# Laser-Interferometric Investigation of Triggering Behavior in CMOS and Smart Power ESD Protection Structures

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We report on noninvasive laser-interferometric thermal and free carrier mapping in electrostatic discharge (ESD) protection devices during a high current stress. The method is based on monitoring the changes in the silicon refractive index due to thermo-optical and plasma-optical effects. We study the homogeneity of bipolar transistor triggering along the device width in CMOS and smart power technology devices. The measured optical phase shift due to temperature and concentration changes is in a good agreement with the results of device simulation.

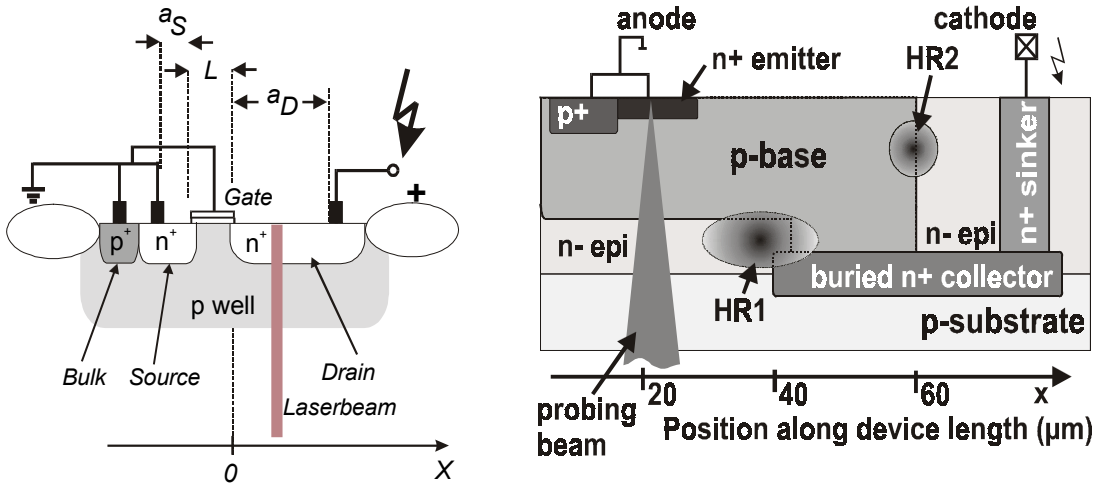
## 1. Introduction

Protection of electronic circuits against electrostatic discharge (ESD) is becoming a more and more important issue with the scaling down of technologies [1] and using the electronics in steadily harsher environment as e.g. in automotive applications [2]. Due to the high energy dissipated during the ESD pulse, the self-heating effect is a dominant failure cause in the ESD protection devices [1]. Due to non-linearities in bipolar conduction, the current flow in the device may be inhomogeneous leading to destructive hot spots. Therefore, thermal mapping is of great importance for hot spot identification and for experimental verification of simulation models [2] – [4]. We have recently developed a laser-interferometric thermal mapping technique for non-invasive investigation of thermal distribution and free carrier concentration changes in ESD protection devices under high current stress [5] – [7]. In this contribution we present the study of triggering homogeneity, thermal and free carrier distribution, and dynamics in CMOS and smart power technology ESD protection devices.

## 2. Results and Discussion

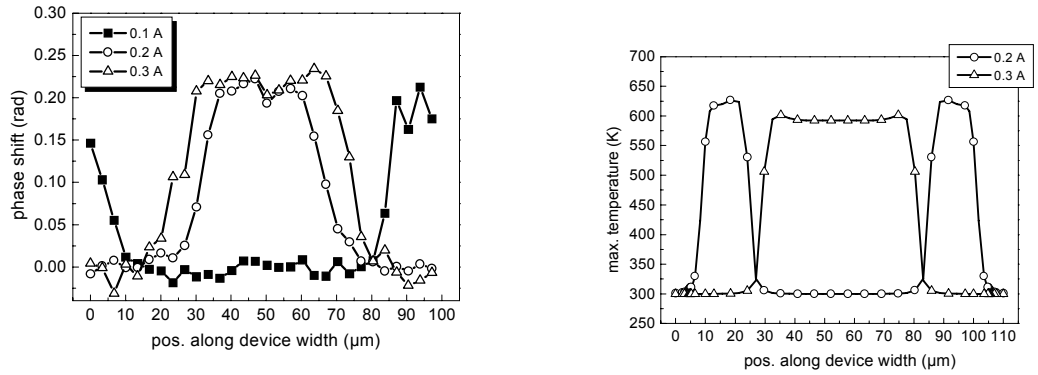
Devices studied are grounded gate- (gg) n-MOSFETs of 0.35 µm process (gate width is 100 µm) [3] and smart power ESD bipolar transistor protection devices [2] (see Fig. 1). The thermal energy distribution and free carrier concentration changes in devices are studied using a heterodyne interferometric technique [5], [6]. The temperature or carrier concentration change during a high current stress causes a modulation of the silicon refractive index which results in a phase shift of an infrared laser beam probing the device from the polished backside. The phase shift is a superposition of thermal and free carrier contributions. They can be distinguished by sign and different time evolution of the phase signal [6]. The devices were stressed by rectangular current pulses using a

transmission line pulser or a DMOS high-current switch. All measurements are performed under the snapback operation where the bipolar conduction occurs in the device.




(a) (b)

Fig. 1: Cross section of (a) gg-n-MOSFET and (b) smart power ESD protection devices. Probing beam is indicated. HR1 and HR2 in (b) indicate the location of regions with dominant heating.

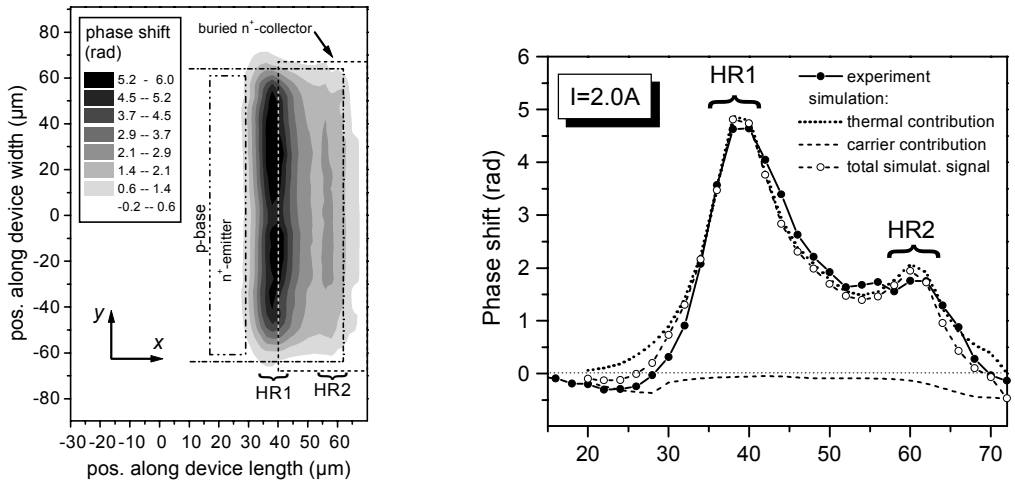



(a) (b)

Fig. 2: (a) Phase shift distribution at the end of 100ns ESD pulse along the width of a gg-n-MOSFET with the stress current as parameter. (b) Simulated current density distribution in the same device.

The trigger homogeneity along the gate width in gg-n-MOS devices is studied at low stress currents. The probe beam is located on position where heat dissipation along the device length is maximal (i.e. at the drain edge of the channel, see Fig. 1(a)). Figure 2(a) shows the measured phase shift distribution along the device width as a function of the stress current. As the holding voltage is nearly current independent, the phase shift represents, in the first approximation, the current density (current per unit of device width). At low stress currents ($I_S$ = 0.1 A) the device triggers preferentially at corners. This is due to a high electric field at the drain/bulk junction curvature at the corners, and consequently higher hole base current density, which promotes the transistor triggering at the

corners. When $I_S$ increases, the triggered place switches to the middle of the device. With a further increase in $I_S$ the triggered width increases, until the device is completely triggered. The change of triggering place from the corner is caused by a lower distributed drain resistance in the device middle, which makes the current conduction in the center energetically more favorable. This trigger behavior can qualitatively be reproduced by an isothermal three-dimensional device simulation using DESSIS$^{ISE}$ (see Fig. 2(b)). At even higher stress currents, when the device is completely triggered, the current conduction along the width is homogeneous until the stress level ($I_S$ > 1 A) where the device fails due to a formation of destructive current filaments [8].




(a) (b)

Fig. 3: 2D distribution (a) and a cross section (b) of phase shift at the end of a current pulse of 170ns duration and $I_S$ = 2A in a smart power ESD protection device (cf. Fig.1(b)).

Because of a larger characteristic feature size in smart power ESD devices, the trigger homogeneity in these devices is studied by performing two-dimensional phase shift mapping in lateral directions. The phase shift distribution along the device length at the end of the stress pulse of $I_S$ = 2 A shows one dominant heat dissipated region (HR 1) and a region with a smaller local temperature maximum (HR 2), see Fig. 3(a). The temperature distribution along the device width is nearly homogeneous, with a slight temperature increase at device corners, probably due to lateral current crowding effect (Fig. 3(a)). Figure 3(b) shows a phase shift distribution along the device length in the middle of the device (y = 0, cf. Fig. 3(a)). The two hot regions HR1 and HR2 can clearly be distinguished. In addition, a region with a negative phase shift can be found under the emitter region. The latter is attributed to a negative phase shift contribution caused by electron injection from the emitter to the base. The electro-thermal two-dimensional device simulation using DESSIS has revealed that the region HR1 (HR2) is related to the heat dissipation due to a vertical current flow from the emitter to the buried layer (due to a subsurface lateral current flow between the p-base and n-sinker), see Fig. 1(b). As the devices at this stress current level trigger homogeneously, the experimental phase shift can be compared to a simulated phase shift. The latter was calculated as a sum of thermal and free carrier contributions, using the integrals of simulated temperature and free carrier distribution along the optical beam path. The agreement between the simulation and experiment is excellent (see Fig. 3(b)). For better distinction of the

free carrier and thermal contributions to the total phase shift, these are also given in the figure.

## 3. Conclusion

The laser interferometric method is a useful characterization tool for study of thermal and free carrier distribution and dynamics in ESD protection devices in ns time domain. An inhomogeneous triggering at low stress currents has been found and explained in gg-n-MOSFET devices. Two hot spots due to a lateral and vertical current path have been revealed in the smart power ESD protection devices. The results are in good agreement with the simulation.

## References

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