Mixed-Signal Circuits on their Way to 0,1µm Technologies

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1. Introduction

Since more than 20 years the semiconductor industry enjoys the benefits of downsizing the device dimensions and thereby increasing functionality and speed of very large-scale integrated circuits. For the first time now there seem to appear some clouds on the horizon. Downscaling integrated circuits below 0.1 µm may face over-proportional production cost due to the increase of process steps and the increase of equipment prices. While digital circuits will follow the well-known scaling laws well below 0.1 µm [1], [2], mixed signal circuits require a differentiated analysis when reaching structure sizes in the order of 0.1 µm and below. The reduced supply voltage affects the dynamic range as well as the noise requirements of analog circuits, and together with threshold voltages not scaling down with the same factor will force a change in circuit topologies. This paper is based on practical experiences with telecommunication circuits designed on technologies between 0.5 µm and 0.13 µm structure size and will describe benefits and challenges of deep sub-micron designs for mixed signal ICs.

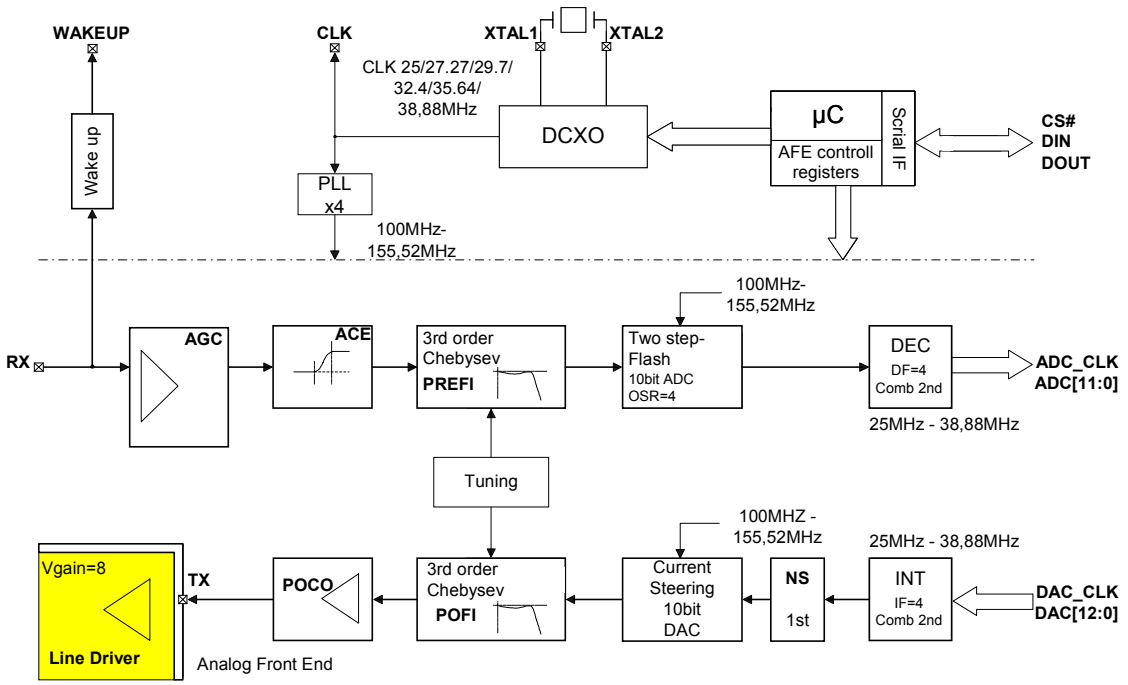
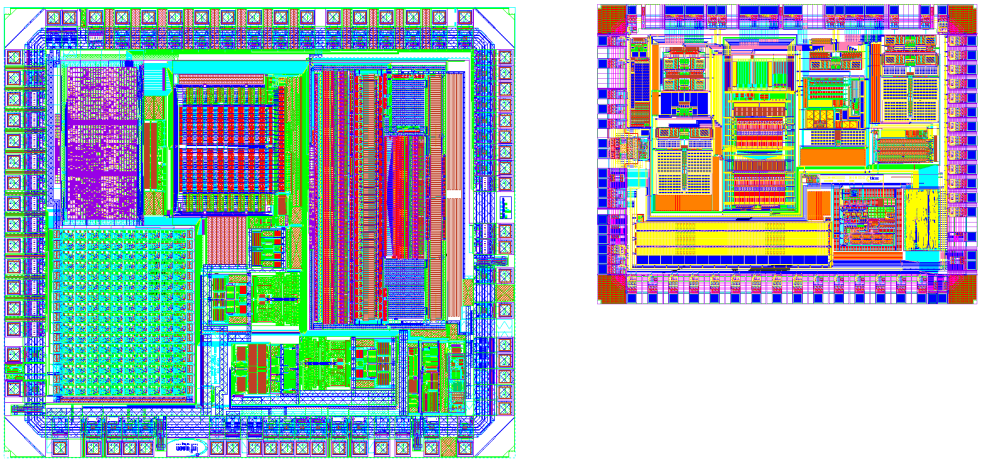


Fig. 1: Block diagram of the analog front-end IC for a VDSL-system for both symmetrical 13 Mbps and asymmetrical 26 Mbps transmission schemes.

2. Requirements Governing Scaling Benefits

In general, scaling down mixed signal circuits in the range from 0.5 µm to 0.18 µm offers a lot of benefits. In particular, the significant increase in bandwidth at constant power levels and the area reduction open up new possibilities in system integration of mixed signal circuits. The scaling of a VDSL analog-front-end IC (Fig. 1) illustrates these benefits. The circuit is part of a new, just unveiled 4-band VDSL solution for both symmetrical 13 Mbps and asymmetrical 26 Mbps spectral band allocation schemes, delivering data for distances of up to 1.5 km over existing telephone copper wire infrastructure.



Technology	0.6 µm BICMOS	0.18 µm CMOS
Supply Voltage	5 V	1.8 / 3.3 V
Area	14,.5 mm^2	7.5 mm^2
Power consumption	710 mW	450 mW
Sampling rate	20 – 33 MSPS	100 – 155 MSPS
Bandwidth	8 MHz	12 MHz

Fig. 2: Result of scaling the VDSL analog front-end IC of Fig. 1.

Figure 2 shows the result of the shrink from a 0.5 µm to a 0.18µm technology: the area was reduced by 50%, and power consumption, by 40%. The increased speed of the transistors allowed to increase the oversampling ratio of the ADC and DAC instead of increasing the moderate resolution of the modules itself. The analog filters and amplifiers also profited from the speed (e.g. the bandwidth of an op-amp increases from 300 MHz to 1 GHz), and there was no problem to enlarge the system bandwidth to 12 MHz required by the new 4-band standard. In conclusion, this example shows that mixed signal circuits with moderate dynamic range or resolution of 11 to 12 bit and higher signal bandwidth are extremely well suited for scaling, and this will continue also to the next generation with 0.13 µm structures and 1.2 V supply.

Somewhat different are the considerations for an ADSL-system [3], [4] that serves for line lengths up to 4 km at an asymmetrical transmission rate of up to 8 Mbps. Here a line referred noise of –140 dBm/Hz, a maximum receive signal of 4 V_{pp} and a signal bandwidth of 1.1 MHz define a dynamic range of 100 dB (Fig. 3). When the allowed signal swing at the input scales down with the structure size of the technology also the noise level in the amplifiers and filters has to be reduced. A simple calculation (Table 1)

shows that due to the noise limitation capacitances in SC circuits increase dramatically with down-scaling. To make it worse modern wafer-processes use low-k dielectrica in order to minimize propagation delay on long and dense interconnects. This in turn increases the chip area consumed by capacitances. In this example, the 0.1 µm generation will need different circuit topologies, e.g. SI instead of SC structures. New structures exploiting the speed advantage of a 0.1 µm process will also be necessary for the 14 bit A/D-converters as shown in Table 2.

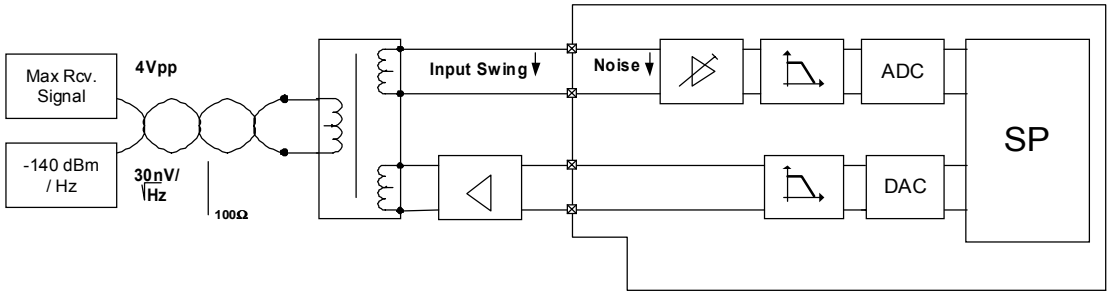


Fig. 3: Schematic input circuit of an ADSL-system. The required dynamic range is 103dB.

Min. Structure Size	Swing	Input Referred Noise	Equivalent R	C (const. RC)
0,5 µm	4 V_{pp}	10 $nV\sqrt{Hz}$	6.7 kΩ	1 pF
0,18 µm	2 V_{pp}	5 $nV\sqrt{Hz}$	1.7 kΩ	4 pF
0,1 µm	1 V_{pp}	2.5 $nV\sqrt{Hz}$	550 Ω	16 pF

Table 1: Equivalent noise resistor and corresponding capacitance calculated for constant bandwidth of an constant dynamic range of the ADSL input circuit shown in Fig. 3.

Min. Structure Size	Swing	ENOB	Quantum Noise	OSR	C_S	f_{CLK}
0.5 µm	4 V_{pp}	13 bit	13 $nV\sqrt{Hz}$	12	150 fF	26 MHz
0.18 µm	2 V_{pp}	13 bit	37 $nV\sqrt{Hz}$	12	2 pF	26 MHz
0.1 µm	1 V_{pp}	13 bit	18 $nV\sqrt{Hz}$	24	4 pF	52 MHz
	New ADC concepts required!			200	0.05 pF	400 MHz
				→ Continuous time ΔΣ-ADC		

Table 2: Change of requirements on the ΔΣ-ADC of the ADSL input circuit (Fig. 3) with downscaling.

Finally the conclusion is that analog processing of signals with a high dynamic range will have to deal with enlarged areas and also significantly higher currents. New circuit

topologies are required, and a careful choice has to be made which circuits can be integrated on a single chip system economically.

3. Circuit Design Considerations

The most severe limitation of analog circuit design in the 0.1 µm region is the fact that V_{th}, the threshold voltage of the MOS-transistors, does not scale linearly with the supply voltage V_{dd}, which will be as low as 1 – 1.2 V. This causes several problems [5]: Amplifier gain will suffer from the lack of cascode stages, and multi stage amplifiers with nested feedback loops might be necessary. Input and output common mode range will overlap only in a small range, thereby reducing the signal swing and so further decreasing the dynamic range. Unfortunately, different requirements for different applications lead to different transistor designs and trade-offs. So currently different threshold voltages and different gate oxide thicknesses are offered within one wafer process, which requires extra masks and lets cost and process-complexity explode.

For true system on chip applications it is consequently desirable to reduce analog circuitry to a minimum and to stick to transistors optimized for digital operation. This was done for a test structure in our newest 0.13 µm process comprising a 10 bit successive approximation ADC, a PLL circuit, a bandgap circuit, and a buffer (Fig. 4). The ADC consists of a switched capacitor array and a comparator circuit and uses only inter-metal capacitors and digital transistors.

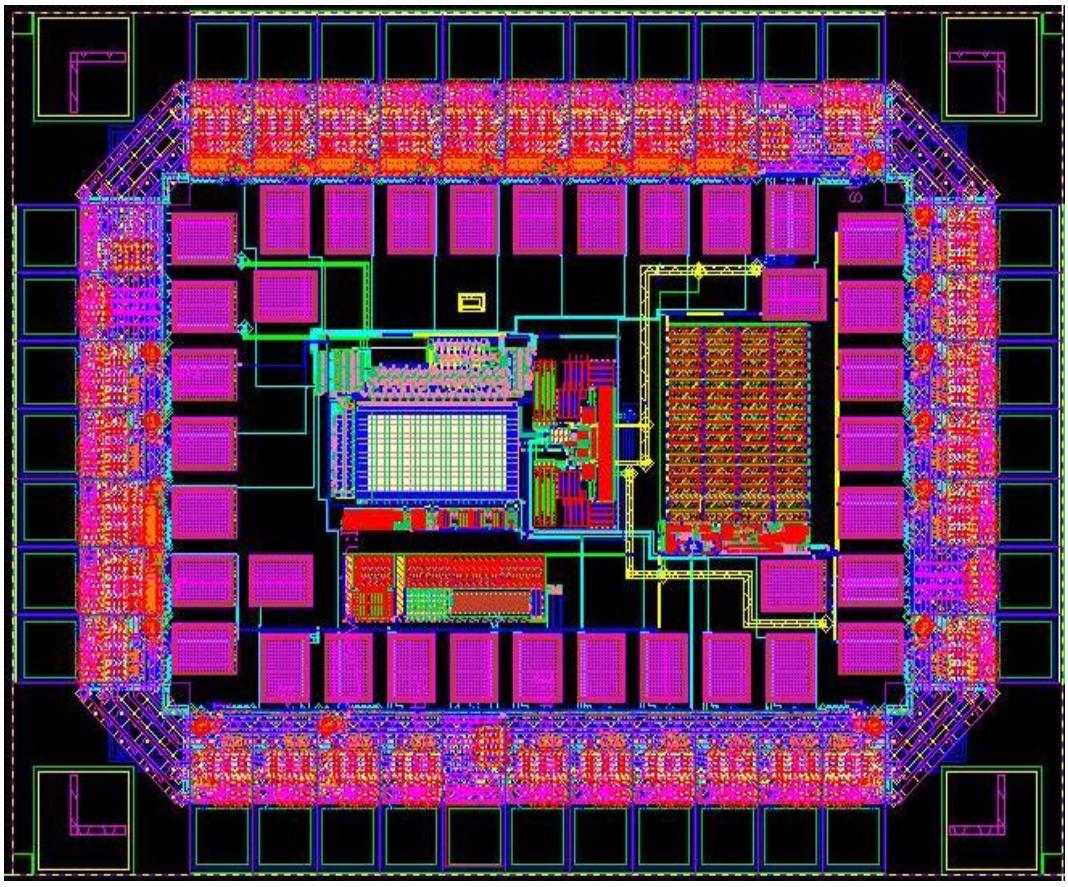


Fig. 4: Layout of a test structure built in a pure digital 0,13µm CMOS process. It contains a 10 Bit SA-ADC, a buffer, a PLL, and a bandgap circuit.

First measurements show an extremely good performance:

Operated at 1.2 V with a sampling frequency of 16 MSPS, the ADC consumes only 2.5 mW and achieves 10 bit THD and 8.5 bit SNR over a signal frequency range of 0 – 8 MHz. The area is 0.082 mm^2.

4. Conclusion

Up to our current mainstream technology with a half pitch of 0,18 µm downscaling of telecommunication ICs delivered the expected increase in performance. When focusing on simple analog structures we expect this trend to continue down to the 0.1 µm region. This was proven by an ADC test structure in our newest 0.13 µm process. For mixed signal circuits requiring a high dynamic range techniques like oversampling or dynamic element matching have to be further developed in order to translate accuracy requirements into speed requirements. In case this is not possible for certain high volume applications we expect to see an increase in process complexity by adding special transistors for mixed signal applications. In general, one-chip solutions for systems on silicon in 0.1 µm processes will represent a challenge to the creativity and ingeniousness of mixed-signal designers.

References

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