Ultrathin Silicon Dioxide: Growth and Characterization

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The technology of ultrathin solid films represents a key issue in microelectronic manufacturing. The continued shrinking of lateral dimensions has to be accompanied by an appropriate reduction of vertical dimensions to control short channel effects. As far as dielectric layers are concerned, silicon dioxide remains in the center of interest. In this work we investigate silicon dioxide layers of a few nanometers thickness grown by thermal oxidation. Electrical characterization of the oxide layers is performed by capacitance-voltage and current-voltage measurements. Comparison of the measured C-V curves with simulated curves shows that the simple MOS-capacitor model used for the simulation is well applicable within the ultrathin regime.

1. Introduction

The formation and characterization of ultrathin dielectric layers is of major importance in microelectronics. Due to the continuing reduction of lateral device dimensions, scaling of the vertical dimensions is required to maintain an appropriate gate control over the channel. In the field of dielectrics silicon dioxide still is the most important material. The gate oxide thickness of MOSFET devices is about to enter the ultrathin layer regime by now. Therefore the electrical properties of ultrathin layers with a thickness of only a few nanometers are of immanent technological interest. These properties are influenced by the growth process itself and post-oxidation processing steps. In this work, ultrathin oxides were thermally grown at intermediate temperatures. The oxidized substrates were integrated into a metal-oxide-semiconductor (MOS) capacitor scheme. Electrical characteristics of ultrathin silicon dioxide were investigated by capacitance-voltage (C-V) and current-voltage (I-V) measurements. The measured C-V characteristics were compared to curves resulting from simulation based on a simple analytical MOS model.

2. Experimental

P-type silicon ($\rho = 14\ \Omega$cm) wafers were oxidized by dry thermal oxidation in pure oxygen after a thorough RCA-clean. To investigate the influence of the oxidation temperature, oxidations were carried out at temperatures from 700 to 800 °C. Oxidation times were adjusted to yield the same oxide thickness (2.8 nm) in each experiment. The oxidized substrates were covered with aluminum by thermal evaporation and patterned using optical lithography and wet etching to form gate electrodes with an area of $1.2\text{x}10^{-4}$ cm^2. Al was sputtered for good backside contacts. The samples were subjected to a pre-metallization anneal at the temperature of the previous oxidation process in an inert atmosphere (N$_2$). The patterned samples were annealed in forming gas (post-metallization anneal) at 400 °C. Annealing times were varied from zero to a maximum of 30 minutes.

A HP 4156B semiconductor parameter analyzer and a HP 4284A LCR meter were used for electrical testing. Oxide thickness was determined from C-V curves at strong accumulation region without any correction and showed good agreement with ellipsometric thickness evaluation.

3. Simulation

In order to simulate the C-V characteristics of a MOS capacitor, the device is modeled as a series connection of a constant capacitance caused by the insulator (C_{Ox}) and the variable capacitance of the semiconductor depletion layer (C_D) [1]. C_D is accessible from (1):

$$C_D = \frac{\partial Q_S}{\partial \psi_S}$$

Q_S....space charge

ψ_S....surface potential

(1)

The space charge is related to the electric field at the surface of the semiconductor ($\mathscr{E}_S$) by (2):

$$Q_S = -\varepsilon_S \mathscr{E}_S$$

ε_S....dielectric constant
    of the semiconductor

(2)

Finally equation (3) describes the ideal relation between the electric field $\mathscr{E}$ and the potential ψ of the material:

$$\mathscr{E}^2 = \left(-\frac{d\psi}{dx}\right)^2 = \left(\frac{2kT}{q}\right)^2 \left(\frac{qp_{p0}\beta}{2\varepsilon_S}\right)\left[\left(e^{-\beta\psi} + \beta\psi - 1\right) + \frac{n_{p0}}{p_{p0}}\left(e^{\beta\psi} - \beta\psi - 1\right)\right]$$

ψ.......potential q.......elementary charge

x........distance from surface p_{p0}...equ. density of holes

k........Boltzmann's constant n_{p0}....equ. density of electrons

T........absolute temperature $\beta = q/kT$

ε_S......dielectric constant of
        the semiconductor

(3)

Knowing the values of C_D and C_{Ox} the overall capacitance and the voltage between gate and bulk is easily computed in dependence of the surface potential ψ_S. The exact position of the calculated curve along the voltage axis is determined from the difference in the work function of the gate metal and the silicon substrate. Since the areas of the stacked capacitors are relatively large, rim induced effects may be neglected in the simulation of the C-V characteristics.

4. Results and Discussion

The variation of the oxidation temperature shows that the C-V characteristic of the gate oxide is drastically improved if the oxidation temperature is increased. Fig. 1 shows the C-V curves of oxide layers grown at 700°C and 800°C respectively. Apart from this both samples underwent the same procedures including pre- and post-metallization anneal. The higher oxidation temperature leads to a well-behaved C-V curve with striking correspondence to the simulated characteristic (dashed line) thereby suggesting that the

simulated curve is valid as a measure of oxide quality. The oxide grown at 700°C on the other hand displays several imperfections like a shifted position along the voltage axis and a nearly constant capacitance from weak to strong accumulation which can be interpreted as a consequence of insulator leakage [2]. The shift of the curve from the ideal position, however, is due to a fixed charge (N_f) of about 1.10^{12} cm^{-2} in the oxide layer. This charge is obviously nearly totally absent when the oxidation is carried out at the higher temperature. Also the post-oxidation annealing procedures were found to be of major influence on the device behavior (Fig. 2).
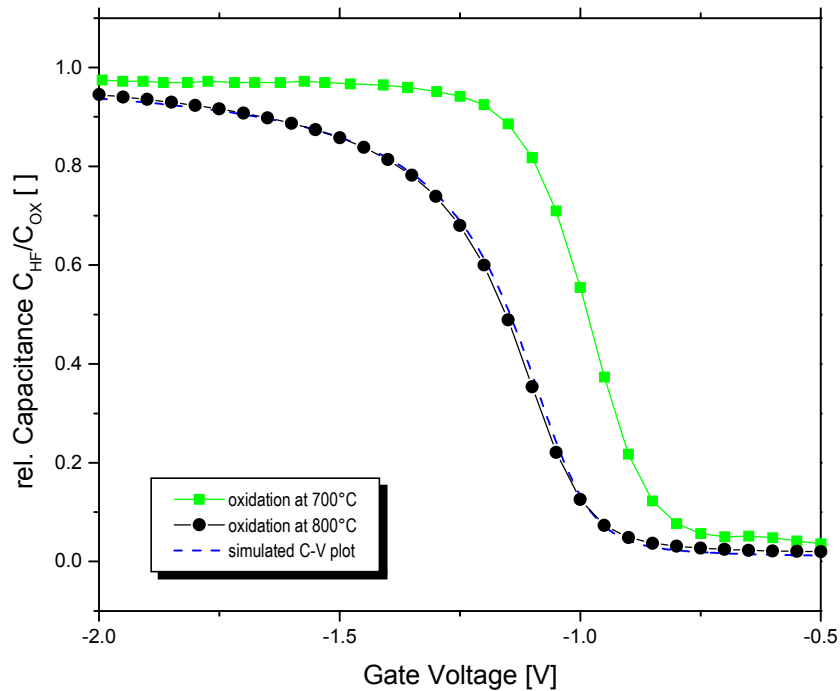

Fig. 1: Typical C-V characteristics showing the effect of different oxidation temperatures.

Without any further temperature treatment after the oxidation, the C-V plot displays a relatively large amount of fixed charge as well as a high density of interface traps which cause the typical stretch-out of the plot (squares). These defects are reduced by a pre-metallization anneal of 30 minutes (circles). Further improvement of the curve to almost the ideal shape of the simulation is achieved by a post-metallization anneal of 10 minutes. Longer heating times are of no desired effect since they in some cases lead to strongly increased gate leakage likely due to metal diffusion through the oxide. Fig. 3 displays a typical current-voltage plot recorded using a sample grown at 800 °C and annealed before and after metallization. The measured current densities are well within the expected range. The much smaller gate currents at positive voltage are due to formation of the depletion layer.
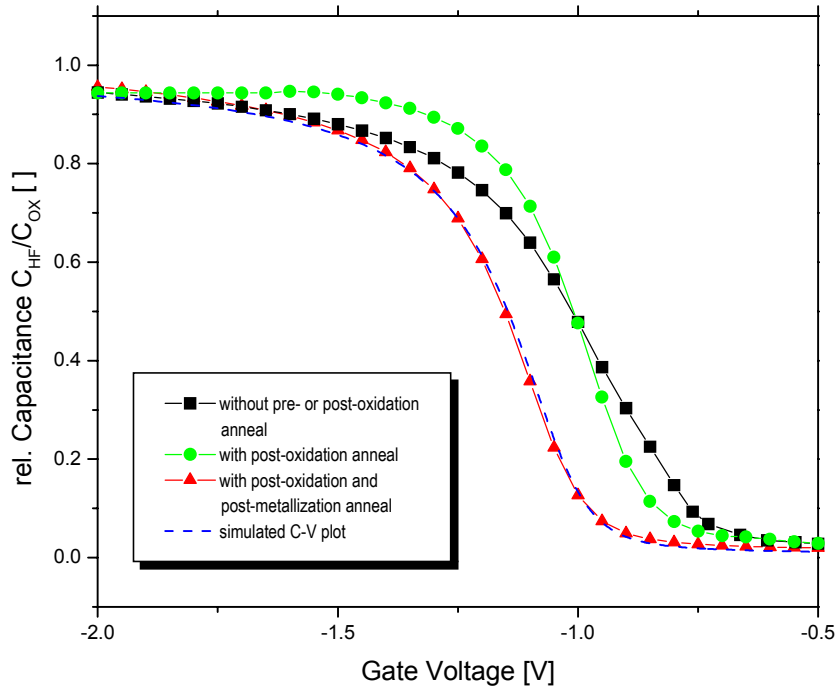
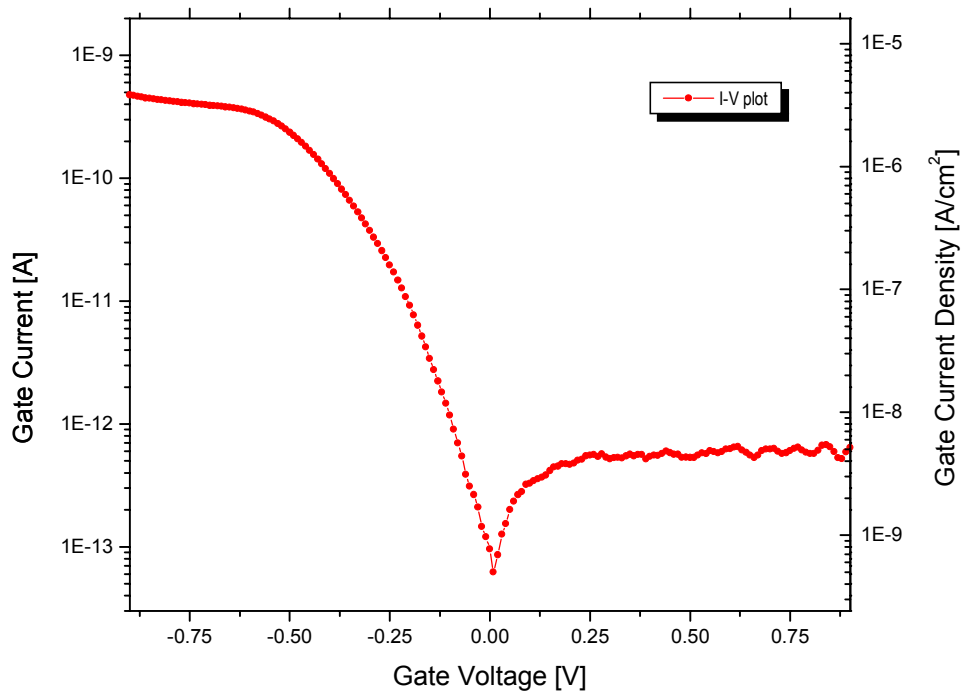Fig. 2: The effect of annealing processes on C-V characteristics.

Fig. 3: I-V curve measured on a fully annealed sample grown at 800°C.

5. Conclusion

Ultrathin silicon dioxide films were thermally grown on p-type silicon at intermediate temperatures ranging from 700 °C to 800 °C and subjected to different pre- and post-metallization annealing steps. Electrical characterizations were performed by capacitance-voltage and current-voltage measurements and compared with simulated curves based on a simple MOS-capacitor model. Excellent agreement of simulation and measurements proved high predictability of electrical behavior and demonstrated applicability to the ultrathin regime. Thus these films are well suited for and have already facilitated pioneering work in demanding applications like scanning capacitance microscopy (SCM) [3].

References

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