Hot Electron Injection Field Effect Transistor

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A new device geometry for a microwave FET with an injection limiting source contact is presented. Through this contact fast electrons are injected into the transistor channel region which leads to a shorter transit time and thereby raised upper frequency limits as compared to a conventional MESFET. Measurement and deembedding methods as well as obtained results are given.

1. Introduction

The purpose of the work reported is to present a new GaAs hot electron injection field effect transistor (HEIFET). In this device the ohmic source contact of a MESFET is replaced by an injection limiting contact in order to inject fast electrons into the channel region. As a consequence the electron transit time through the channel region is reduced, and so the transistors upper frequency limits (f_T and f_{max}) are raised.

2. Experimental

In our HEIFET [1] a hot electron injection contact of the type used in the planar injection limited Gunn diode or "FECTED" [2] replaces the highly doped source contact used in conventional MESFETs. The injection limiting contact which consists of an ohmic contact and an overlapping Schottky gate injects hot and, hence, fast electrons into the FET channel thereby reducing the total transit time throughout the channel. A cross sectional view of the HEIFET is shown in Fig. 1.

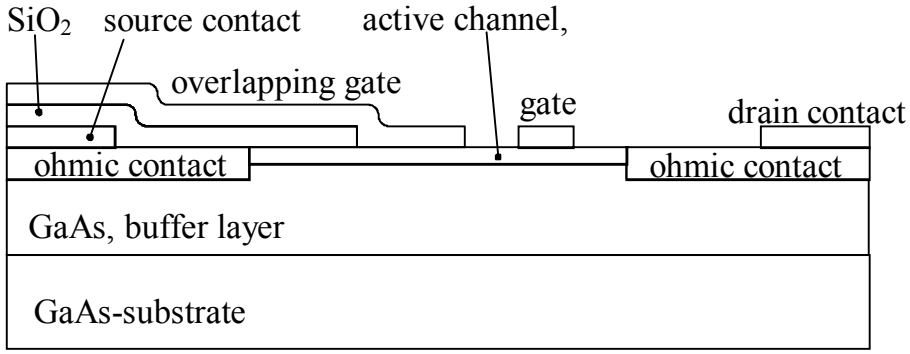

Fig. 1: Cross section of a HEIFET.

In conventional MESFETs the time needed to accelerate electrons leaving the highly doped source region can be as large as a few picoseconds due to the slow energy transfer (energy relaxation) time. This is in our opinion the reason why 0.5 µm gate MESFETs

exhibit a rather low f_T although the time electrons take to traverse a distance of 0.5 µm at saturated velocity (≈10^7 cm/s) is only around 5 ps which is one third of the RF cycle at 60 GHz and which should be short enough to allow efficient operation of a 0.5 µm gate-MESFET at 60 GHz.

3. Measurement Circuit

Our transistors are manufactured by conventional electron beam lithography and lift off techniques in the cleanroom of the Microelectronics Institute. The most critical step in the manufacturing process is the placement of the 0.5 µm gate between the overlapping gate and the ohmic drain contact. In order to need only one gate per transistor an asymmetric layout as shown in figure 1 has been chosen. The transistors are embedded in a coplanar test circuit which allows contacting with a Cascade Microtech waverprober with coplanar HF-tips and so measurement with an HP 8510C vector network analyzer. An overview of the transistor within it's test circuit is given in Fig. 2.

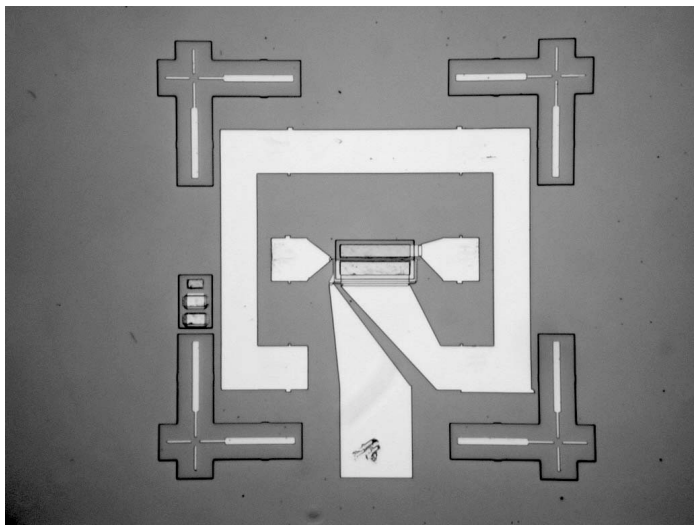

Fig. 2: HEIFET with measurement circuit.

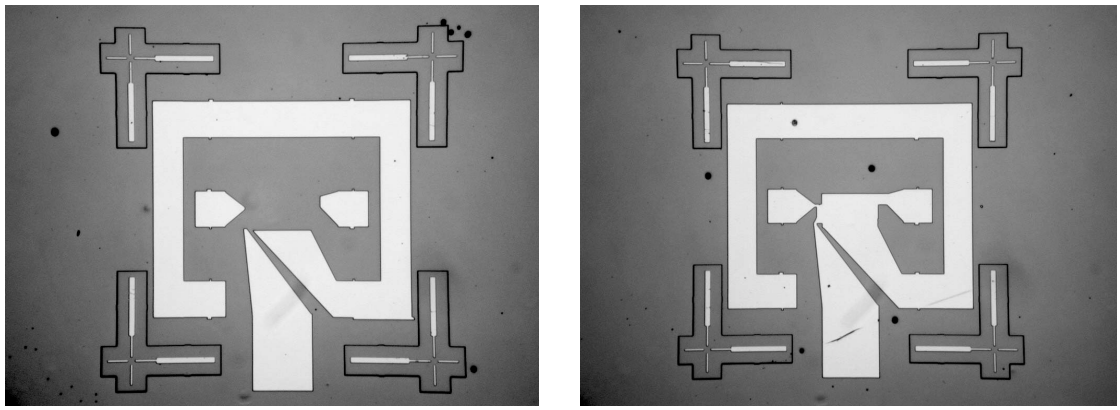

Fig. 3: Open structure (left) and short structure (right) for de-embedding.

4. De-embedding

The only purpose of the test circuit is to enable contacting of the device with coplanar tips during measurement. Since the overall behavior of the transistor is influenced by the test circuit's properties it is necessary to subtract this influence from the measured data. From several available methods to perform this deembedding operation we chose to use one employing separate open and short circuits as shown in Fig. 3 [3].

Following this method the deembedded impedance matrix Z_{TRAN} of the transistor can be calculated by $Z_{TRAN} = \left(Y_{DUT} - Y_{open}\right)^{-1} - \left(Z_{short}^{-1} - Y_{open}\right)^{-1}$. The required values Y_{DUT} for the embedded transistor, Y_{open} for the open structure, and Z_{short} for the short structure can be directly obtained from the measured S-parameters.

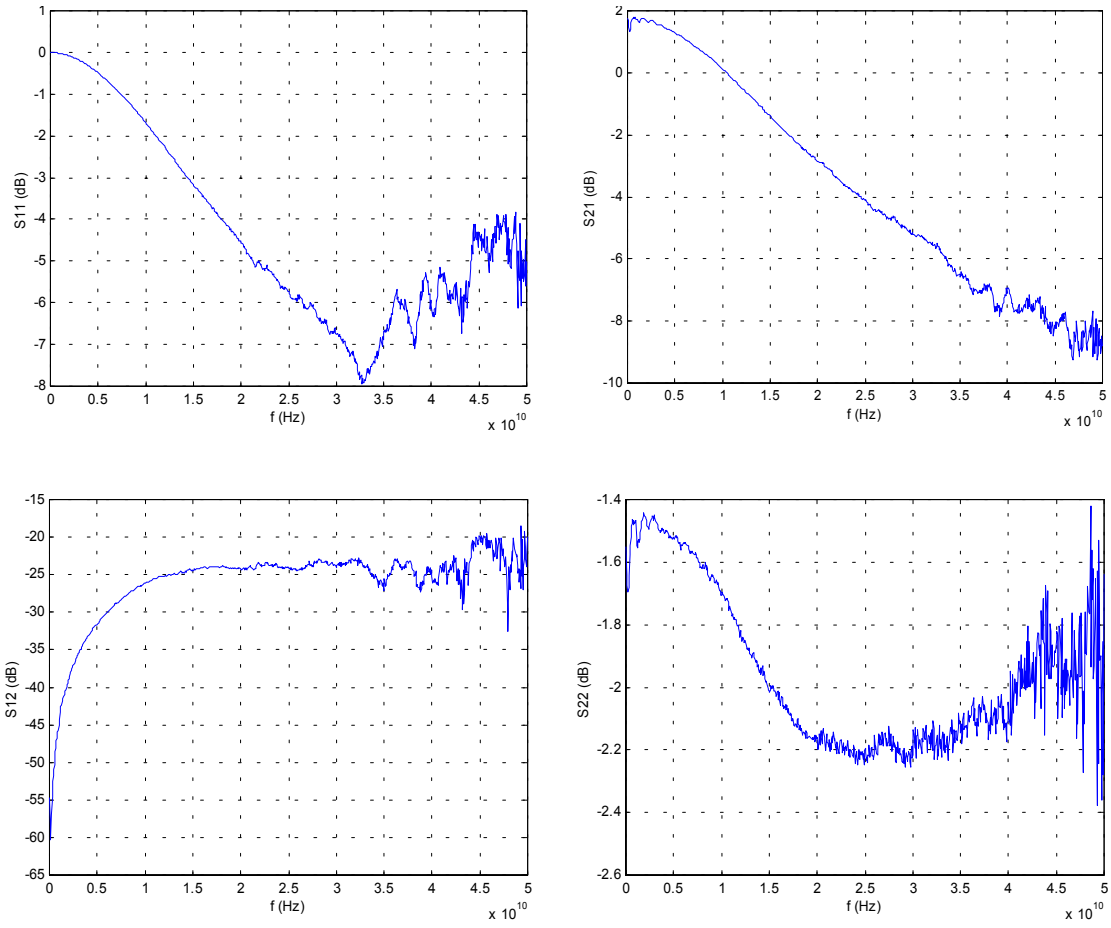

Fig. 4: De-embedded S-parameters of a HEIFET.

5. Results

Using our HP 8510C VNA our transistors have been measured in the frequency range from 45 MHz to 50 GHz. Figure 4 shows the deembedded S-parameters of a HEIFET at a drain voltage of $V_{DS} = 2$ V, gate bias voltage of $V_{GS} = -1.25$ V, and a bias voltage of $V_{BS} = 0.25$ V applied to the overlapping gate. Figure 5 shows the current gain h_{21} calculated from these S-parameters. Therefrom a transit frequency of $f_T = 32$ GHz is deter-

mined for this device. At a frequency of 32 GHz the h_{21} curve departs from its 20 *dB/decade* slope as can be seen in Fig. 5 and continues horizontally. In our opinion this departure from the expected slope is an artifact caused by effects which stem from measuring an asymmetric device with symmetric coplanar tips. Because of the smooth 20 *dB/decade* slope of the curve at lower frequencies we are nevertheless confident that the given value of f_T is reasonable.

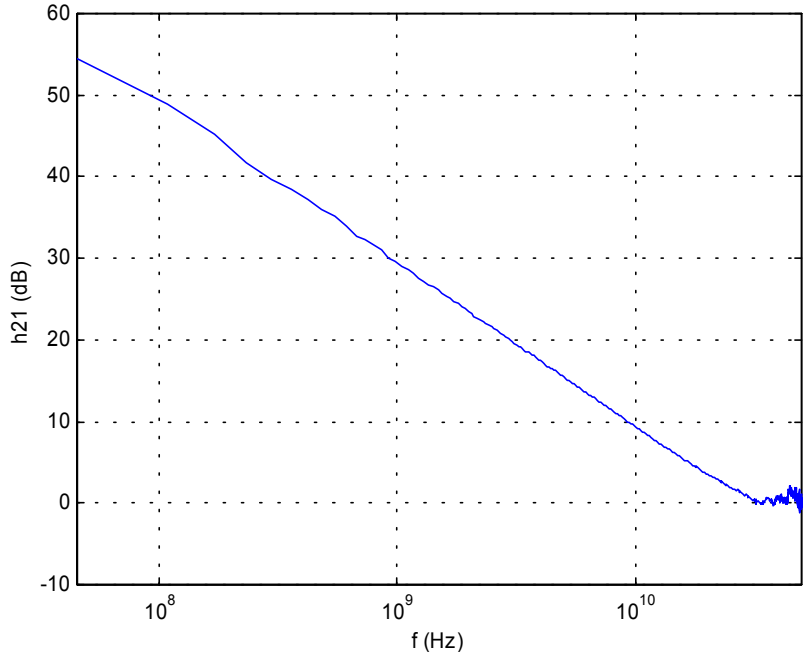

Fig. 5: Deembedded current gain of a HEIFET

6. Conclusion

Despite none of the usual features for improving the upper frequency limit of a FET like gate recess or a mushroom gate have been implemented our transistor shows a transit frequency of 32 GHz which is a good value for a 0.5 µm device. By replacing our current transistor layout with a symmetric one and using an appropriately modified test circuit we hope to extend the range of reliable S-parameter measurement towards higher frequencies. Additionally we hope to raise the f_T of our transistor by optimizing its geometry as well as the parameters of the active channel.

Acknowledgements

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