GMe Forum 2003

Abstracts of the Invited Presentations

Vienna University of Technology
April 10 and 11, 2003

Society for Microelectronics
Vienna, 2003

Society for Microelectronics
c/o Institute of Industrial Electronics and Material Science
Vienna University of Technology
Gusshausstraße 27–29/366
A-1040 Vienna, Austria

Forum Program

Thursday, April 10, 2003

	Opening:
09:00 – 09:30	E. GORNIK (President of the GMe)
	P. SKALICKY (President of the Vienna University of Technology)
	SOI and Waferbonding:
09:30 – 10:15	U. GOESELE, S. CHRISTIANSEN (MPI Halle): "*Strained Si and Wafer-Bonding*"
10:15 – 11:00	G. CELLER (Soitec, Summit, NJ, USA): "*SOI: Developments, Challenges, and Applications*"
11:00 – 11:15	Coffee Break
11:15 – 12:00	P. LINDNER, T. GLINSNER, V. DRAGOI, J. WEIXLBERGER, C. SCHAEFER (EV Group, Schärding): "*Key Enabling Process Technologies for Advanced Semiconductors, MEMS and Nanomanufacturing*"
	Semiconductor Intellectual Property:
12:00 – 12:45	M. KÄSTNER (NewLogic, Lustenau): "*Semiconductor Intellectual Property Industry*"
12:45 – 14:00	Lunch – Catering
	System on a Chip:
14:00 – 14:45	D. DRAXELMAYR, R. PETSCHACHER (Infineon, Villach): "*Mixed-Signal Design for SoCs*"
	Nano-Technology:
14:45 – 15:30	E.J. FANTNER (IMS, Wien): "*Micro@Nano-Fabrication-Austria*"
15:30 – 16:00	Coffee Break
16:00 – 16:45	E. HAMMEL (Electrovac, Klosterneuburg): "*Applications of Micro- and Nano-Technologies*"
16:45 – 17:30	H.G. CRAIGHEAD (Cornell, Ithaca): "*Nanomechanical Systems*"
17:30	Panel Discussion: "*Can Austria Keep Up Internationally in the Area of Nano-Technology?*"

Friday, April 11, 2003

	Organic Electronics:
09:00 – 09:45	G. Leising (AT&S, Leoben): "*Integrated Organic Electronics*"
	Sensors:
09:45 – 10:30	M. Brandl, Ch. Fürböck, F. Schrank, V. Kempe (AMS, Unterpremstätten): "*A Modular MEMS Accelerometer Concept*"
10:30 – 11:00	B. Jakoby (TU Wien): "*Sensors and Interface Electronics for Oil-Condition Monitoring*"
11:00 – 11:15	Coffee Break
	Thermal Imaging:
11:15 – 11:45	D. Pogany (TU Wien): "*Local Thermal and Current Imaging of Power Devices*"
	Opto-Electronics:
11:45 - 12:15	W. Schrenk (TU Wien): "*Quantum Cascade Lasers*"
12:15 - 12:45	T. Fromherz (JKU Linz): "*Light from Silicon: SiGe Quantum Cascade Structures*"
12:45 - 13:15	K. Schmidegg (JKU Linz): "*In-situ Growth Monitoring and On-Line Composition Determination of MOCVD GaN by Spectroscopic Ellipsometry*"
13:15	Snacks and Poster Exhibition

Wafer Bonding and Strained-Layer Silicon

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Wafer bonding refers to a process in which two mirror polished wafers of almost any material are brought into contact and hold together permanently if treated properly. Over the last 20 years wafer bonding has moved from a kind of exotic phenomenon of limited technological interest towards a potential future mainstream technology especially in the context of silicon-on-insulator (SOI) applications. The talk will cover the historical development of wafer bonding and the basic physics and chemistry involved. Different bonding technologies will be touched upon including those which are still in a lab stage like ultra-high vacuum bonding which allows bonding at room temperature with full bonding strength. The talk will mainly deal with silicon but will also mention the bonding of other materials such as III-V compounds. Thinning and layer-splitting technologies will be mentioned shortly. Details of the "smart-cut" approach will be covered in the subsequent talk from SOITEC Company. Various applications of wafer bonding as a generic materials integration approach will be covered including SOI, micromechanics, LEDs and photonic crystals. In a final part the area of strained silicon layers will be discussed which allow an increased electron and hole mobility. In the long run it will be desirable to obtain highly strained silicon layers on insulator (SSOI). Different competing relaxation approaches of SiGe layers and subsequent Si layer growth and layer transfer by wafer bonding will be presented.

SOI: Developments, Challenges, and Applications

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Silicon-on-Insulator (SOI) wafers significantly improve performance of electronic circuits. Initially, the driving force for developing SOI material was to increase radiation hardness of integrated circuits, i.e., improved immunity to single event upsets caused by ionizing particles. More recently, SOI applications entered the mainstream of digital electronics, where they provide increased switching speed of transistors and/or reduced power consumption – this is accomplished primarily because the source and drain capacitance is lowered by having an insulator layer below a MOSFET. As device gate length is scaled below 50 nm, thin SOI layers are becoming essential to maintain proper transistor action by suppressing the short-channel effects. Eventually, planar transistors will need to be replaced with double gates or with vertical transistors – SOI plays an important role in these novel device architectures as well.

The dominant commercial method of fabricating SOI structures is known as the Smart Cut™ process, and it evolved from an invention by M. Bruel [1] at LETI in Grenoble. It utilizes ion implantation as an "atomic scalpel" to cut semiconductor crystals layers. Hydrogen doses $>5\times10^{16}$ cm^{-2} are typically used for splitting of silicon. For the process to work, the implanted surface is bonded to another wafer. At 300–600 °C, depending on material and implant conditions, the pressure of hydrogen that accumulates in the microcavities and microcracks induced by the initial implantation, causes splitting along the implanted zone. The net result is that a thin layer of Si, defined precisely by the implant depth, is transferred from a seed wafer to a handle wafer. Uniform and continuous single crystalline Si films <100nm thick and 700 cm^2 in area (300 mm diameter) can be routinely transferred to new substrates. Such wafers currently serve as substrates for high performance microprocessors, where increased switching speed and reduced power dissipation are important.

The layer transfer process can be applied to a variety of materials. Thin Si films can be transferred to fused silica or glass substrates. SiGe layers and strained Si layers, which enhance mobility of charge carriers, can be transferred to oxidized Si handle wafers. Bonding of single crystalline SiC, InP, and GaAs films to oxidized Si wafers has been demonstrated.

In addition to the purely electronic applications, SOI is used to build MEMS and microphotonic circuits. Challenges in fabrication of advanced SOI wafers and their current and future applications will be reviewed.

Reference:

[1] M. Bruel, Electron. Lett. **31**, 1201 (1995).

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Key Enabling Process Technologies for Advanced Semiconductors, MEMS and Nanomanufacturing

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New technologies like wafer level packaging, MEMS and Nanosystems frequently adopt semiconductor manufacturing processes at an early stage. Specific novel process steps however often develop to become key enabling. The paper will focus on two examples of key enabling process steps: wafer bonding and nano imprint lithography.

Wafer bonding enabled first the economic manufacturing of MEMS devices. Technological reasons for the success of the process in the MEMS community are mainly 3 fold: (a) A bonded wafer stack forms a sealed “first level package” and therefore protects fragile micro machined features from harsh environments occurring during dicing. (b) Allows to encapsulate a controlled ambient (like vacuum) to control a device’s sensitivity and adjust the properties. (c) Stress Isolation: The first level package created at wafer level isolates mechanical stress introduced by the final package (mold or mounting method to board).

In addition, advanced semiconductors found benefit in the bonding technology through: (a) Optical and electrical interconnects (3D interconnects) can be formed at wafer level rather than chip level in order to increase the integration density or the functional density of a device. (b) Creation of chip scale packages at wafer level. (c) New starting materials for advanced semiconductor and MEMS devices (most prominent example is the SOI Wafer). (d) The ability to handle thin and ultra thin wafers for advanced power devices and compound semiconductors.

Examples of devices that utilize above mentioned benefits will be given as well as an overview of wafer bonding methods.

Classical lithography in semiconductor mainstream IC production employs stepper technologies today. Challenges and costs of this technology are steeply increasing at structures below 130 nm. Nano imprinting is a new method for generating pattern in submicron range at reasonable cost. It therefore has the potential for a wide variety of applications in BioMEMS, Biofluidics, Microoptics and Nanotechnology.

The paper will give an overview on emerging Nano Imprint Lithography (NIL) technologies: (a) Hot Embossing (HE) which uses increased temperature to imprint a hard stamp into a polymer. (b) UV Imprinting (UV Molding) which utilizes UV irradiation to cure a polymer between stamp and substrate. (c) Micro Contact Printing (µCP) which transfers a self assembled monolayer (SAM) from a stamp to a substrate surface.

Equipment and tool technology was developed in the past years to support these new emerging imprinting methods.

About EV Group

EV Group (EVG), founded in 1980, is headquartered in Schärding, Austria and has subsidiaries in Phoenix, Arizona, Cranston, Rhode Island and Yokohama, Japan as well as representatives around the world. EVG manufactures a full line of wafer bonders, mask and bond aligners, photoresist coating systems and cleaners for microelectromechanical systems (MEMS) and semiconductor market segments. EVG’s systems are used worldwide in high-volume production environments as well as research and development facilities. For more information visit the EVG web site at www.EVGroup.com, e-mail p.lindner@evgroup.at or call EVG directly at +43 7712 5311-0.

The Silicon Intellectual Property Industry

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In the mid 1990s a new breed of companies emerged: commercial semiconductor intellectual property providers. These SIP firms focus on the development of IP; instead of taking it to production in the form of a complete IC design, they license their technology to IDMs, ASIC vendors, fabless semiconductor manufacturers and to the semiconductor groups of system OEMs who in turn integrate the licensed IP cores into their IC designs. IP companies do not sell chips – they provide technology that will be embedded in their customer's IC designs, hence the term "chipless" company.

The SIP business model can be seen as an extension to the fabless model and to the silicon foundry business model. Silicon foundries enabled fabless companies to capitalize on their design and system expertise without having to invest in a manufacturing facility. Now, the IP companies capitalize on their IC design and system know-how without having to go all the way to IC production.

Commercial intellectual property is the latest phase of the vertical disintegration process of the semiconductor industry. Independent IP providers now challenge one of the last remaining core competencies of semiconductor vendors, the creation of IP and IC designs. Enabled by the availability of third part IP and IC design services, a semiconductor company can be reduced theoretically to a marketing and sales department supported by a logistics group that handles all outsourcing partners.

Mixed-Signal Design for SoCs

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System on Chip (SoC) has become a very popular term in the last years. Although there is no strict definition for it people usually agree that system on chip features

- a complete solution for a specific customers need
- high complexity
- different parts coming from different design worlds, such as digital + analog or RF

Examples which drive the development today are GSM-chips with extensions towards GPRS and UMTS or XDSL systems like ADSL or VDSL. For these high complexity SoCs it is crucial to realize them in cost saving process technologies, which in most cases means to implement them in the latest technology with smallest possible feature sizes. Generally we have to observe that cost reduction is achieved by defining a mainstream CMOS process optimized for digital processing and trying to implement analog or RF function on top of that without generating extra process overhead. We shall present some examples of this:

- A fully embedded 10b 160MS/s two-step ADC in 0.18 µm CMOS
- A sub-psec Jitter PLL for Clock Generation in 0.12 µm Digital CMOS

In the area of automotive chips the challenges are usually different: Instead of getting high complexity in standard CMOS we face the problems of power handling and design robustness against ambient conditions. As examples for this we shall present:

- A Mixed-Signal Hall Sensor IC
- A Robust Smart Power Bandgap Reference Circuit

So currently we see the trend to integrate full systems on the chip going towards ever higher complexity and performance.

However, if we try to look forward for another five to ten years, will this also be the trend of the future? If we look into the requirements for analog and digital circuit design we see some differences that even will become worse in future. We shall discuss some arguments pro and con SoC with respect to the constraints given by process technology, cost and time to market, in order to get some clues what the trends could be.

Micro@Nano-Fabrication-Austria

Ernest J. Fantner
IMS Nanofabrication, Vienna, Austria

Micro@Nano-Fabrication-Austria (MNFA) is a cluster-project within the Austrian Nanoinitiative. It is carried by 19 partners from university, Fachhochschule, non-university centers, Kplus-competence centers and industry. The cluster consists of 33 specific projects which cover 5 topical issues. These are

- Micro@Nano Structuring
- Bio-inspired Materials
- Functionalised Nanomaterials
- Nanodevices
- Sensors & Actuator Systems

The common denominator of all these projects is the use of large-field ion projection optics for 2- and 3-dimensional direct structuring of matter in the micro & nano scale.

The main topic of my talk will be the description of the innovative business creation approach based on the rather unique co-operation between basic research, applied research and commercial product development in the early phase of the Technology Adoption Life Cycle. The resulting competitive advantages in terms of time-to-market, risk-to-market and road-to-market will be discussed. Describing the business life cycle in the environment of a discontinuous innovation by 4 phases, it will be shown how the complementary strengths of basic (university) research and commercial product development can be exploited in the best way. Criteria and specific examples within the MNFA-project will be presented.

An attempt to benchmark this Austrian cluster approach against other concepts within relevant segments of the global micro & nano market will made.

Applications of Micro- and Nanotechnologies

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Carbon nanofibers and nanotubes are promising to revolutionize several fields in material science and are suggested to open the way into nanotechnology. Further market development will depend on material availability at reasonable prices. We have achieved bulk production capacities of high purity carbon nanofibers (CNFs) at low cost by a catalytic chemical vapor deposition (CCVD) process. Reasonably low temperatures and yields of up to several g/m^{2}min at more than 70% carbon gas-to-fiber conversion rates allow considerable cost reductions. Polymer composites have been prepared by shear mixing of CNFs into polymer matrices and extrusion. Another application of our Carbon nanofiber process technology has demonstrated their satisfying field emission properties for large display flat panel devices. We are also studying new carbon fiber composites for hydrogen storage and electronic thermal management applications. Combined with our existing microcooler technology we will reach new horizons in thermal management of high power devices. Microchannel microcoolers have been enabling a breakthrough of semiconductor lasers for industrial applications.

Nanomechanical Systems

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We have created mechanical devices using a variety of materials that we have been studying as sensors and other applications. In most cases, the motion of these devices was detected and in some cases actuated by the application of light. Spatially varying mechanical driving of micromechanical structures was also demonstrated using a scanning probe tip for actuation and an electron beam to detect motion. Sensor applications include immunospecific detection of single bacterial cells and chemical monolayers. Parametric amplification of mechanical motion was demonstrated in a variety of device configurations with optical and electrodynamic drive. High-resolution lithographic processes have been used to create similar resonant mechanical systems with dimensions down to tens of nanometers. Related nanofabrication approaches have also been used to create nanostructures for the mechanical manipulation and sorting of molecules by mechanical and physical properties in a variety of fluid containing system configurations. Mechanical confinement of fluid systems has also been used to enable optical detection and analysis of individual biomolecules.

Integrated Organic Electronics

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and

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The class of organic materials, conjugated polymers, and organic molecules has reached a quite mature and highly accepted status after more than 20 years of intense research and development. The quality and the purity of these new semiconducting materials have been improved by new approaches of chemical synthesis and chemical purification processes and are now demonstrating purity levels which are comparable with state of the art values of inorganic semiconductors. The question of the intrinsic electronic properties of these organic semiconductors is still not answered but the high quality of the available materials made it possible to fabricate electronic devices like field-effect transistors (FET) and optoelectronic devices like organic light-emitting diodes and solar cells. We will report on our research activities targeting the manufacturing of organic field-effect transistors (OFET) with thin films of acenes and other organic semiconductor candidates including results on the growth and characterization of single crystals of acenes. We will outline the current status and the perspectives of these organic electronic devices concerning their performance and integrability into electronic circuits of other platforms, which provides a wide spectrum of applications for new integrated functions.

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A Modular MEMS Accelerometer Concept

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A quasi-monolithic MEMS concept setting up a new family of MEMS-based sensors is presented. The concept combines the advantages of hybrid MEMS with respect to optimal technology choice, and of monolithic integrated MEMS with respect to system integrity, on chip signal conditioning, self-calibration and size.

A sensor signal conditioning circuit and a micro-mechanical sensing element are joined face-to-face by eutectic bonding on wafer level. This sealed system can be used as is, or can be assembled in standard SOIC plastic package. Using this approach, austriamicrosystems AG has developed high performance, low-cost accelerometer sensors.

The accelerometer micro-system consists of the mechanical component die with a single clamped poly-silicon cantilever and an ASIC die with counter-electrodes to measure the distance between cantilever and IC surface. The operation in closed loop mode yields high linearity and large bandwidth.

Specific advantages of the concept are:

1) the modular approach is open for advanced sub-micron technologies,

2) the hermetic seal approach paves the way to new vacuum-on-chip MEMS products.

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austriamicrosystems AG, with headquarter in Unterpremstaetten near Graz (Austria), is one of the world's leading designers and manufacturers of custom specific mixed signal ICs. The company has 940 employees and offices in 14 countries worldwide. Despite the semiconductor downturn austriamicrosystems' sales in 2001 grew by 20% to approximately EUR 147 million.

Sensors and Interface Electronics for Oil Condition Monitoring

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Because of electronic engine control, the engine performance in automobiles has considerably increased, yielding better control of the engine's efficiency and associated exhaust gas emissions. Recently, there has also been increased interest in monitoring the condition of lubricants facilitating proper engine operation. Monitoring the engine oil condition at first instance allows the implementation of increased oil drain intervals. Moreover it provides increased insight into the actual state of the engine, which enables the detection of possibly approaching engine failures but also the monitoring of the performance of engine oils of varying quality. Similar considerations hold for other application where oils are used as lubricants.

The current state of the art in automotive engine oil condition monitoring relies on algorithms aiming for the evaluation of the oil condition. This is achieved by means of processing driving parameters such as elapsed mileage since the last oil change and the number of cold starts. However, this approach merely yields an indirect evaluation of the oil's actual condition. A more direct approach is the implementation of physical sensors in the oil, because their readings are directly related to the actual oil condition.

In this contribution we discuss the suitability of two physical parameters for this purpose: permittivity and viscosity. The latter can be determined using microacoustic viscosity sensors, i.e. piezoelectric devices which can be fabricated using planar microtechnology. However, standard readout concepts for microacoustic sensors are currently either based on bulky and expensive measurement equipment or electronic oscillator circuits. These oscillators malfunction in case of higher viscosities due to the associated higher device damping. In various cases higher viscosities are of primary interest, e.g. for monitoring at low engine temperatures but also for a number of other viscosity sensing applications, e.g. in food industry. For this purpose, we present an alternative measurement approach, which can be implemented in a compact fashion with cost-effective standard components.

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Local Thermal and Current Imaging in Power Devices

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Experimental access to internal parameters of semiconductor devices as carrier concentration, current densities, power dissipation, temperature, etc. is of great interest for the understanding of device physics and for device optimization. Monitoring of the temperature is especially important for power and electrostatic discharge (ESD) protection devices (PDs), where the self-heating effect is a main cause of device failure. These devices operate at high current and power densities where the internal device behavior predicted by device simulation has a limited degree of confidence, due to lack of calibrated physical models at high temperatures. As the self-heating phenomena in these devices occur in ns to µm time scale, the experimental verification of the simulation results necessitates ns time resolution.

In the backside transient interferometric mapping (TIM) technique, an infrared laser beam (λ = 1.3 µm) probes the temperature- or free carrier-induced changes in the semiconductor refractive index inside a device. The resulting phase shift is detected interferometrically, using a scanning or 2D holographic interferometry method (ns time and µm space resolution). The devices are stressed with high current pulses of 10 ns and 100 ns duration, representing the time scale of the charge device model (CDM) and human body model (HBM) ESD stress, respectively.

This contribution is focused on the application of the TIM method for the study of ESD phenomena in smart power technology ESD protection devices and power DMOS transistors. Hot spots, current instabilities and moving current filaments are investigated. The spatio-temporal distribution of current and temperature is correlated with the time evolution of electrical characteristics. The comparison between the measured and simulated phase distributions is used for the verification of device simulation models in HBM and CDM time domains. As well, failure mechanisms in ESD protection devices are investigated by monitoring the hot spot dynamics during a single destructive pulse.

Quantum Cascade Lasers

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Quantum cascade lasers (QCLs) are powerful light emitters in the mid infrared and, most recently also in the far infrared. The light generation is based on intersubband transitions, usually within the conduction band. The strong light emission in the mid infrared spectral region is interesting for chemical sensing and a potential application for far infrared emission is astronomy and tomography in medicine. Recently, continuous wave operation at room temperature of InP based QCLs has been demonstrated.

In this work, we intent to present our latest results on the improvement of GaAs/AlGaAs QCLs. The emission wavelength of the mid infrared lasers covers now a range from 8.7 µm up to 23 µm. The optical waveguide for 23 µm is a surface plasmon waveguide whereas for wavelength below 20 µm a double plasmon enhanced waveguide is used for vertical light confinement. The highest working temperature of a GaAs/AlGaAs QCL in pulsed mode operation is increased close to 100 °C and the average power of the 11 µm wavelength emission is above 1 mW at room temperature. Accelerated aging tests showed an estimated lifetime of 80 years.

We have also fabricated narrow (w = 10, 20 µm) Fabry Perot and distributed feedback lasers. Distributed feedback lasers own a spectral single mode emission, which make them suitable for the measurement of narrow absorption lines, typical for gases. The threshold current density does not show a strong dependency on the laser width, which is a result of the strong lateral light confinement of the deep etched ridge lasers. By reducing the width of a laser, the operation current is reduced, which helps to cut the costs of the electronics and the laser cooler.

Light from Silicon: SiGe Quantum Cascade Structures

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Recently, electroluminescence in the far-infrared (FIR) at THz frequencies [1] as well as in mid-infrared (MIR) spectral region [2], [3] has been observed for SiGe quantum cascade structures. Both the improvement of low temperature SiGe molecular beam epitaxy as well as the growth on relaxed, high quality SiGe buffer (pseudo-substrates) have enabled the recent progress in the development SiGe cascades: Due to the large lattice mismatch of Si and Ge, the layers of a SiGe cascade structure are highly strained. In order to suppress the relaxation of the strain via the formation of dislocations during growth on Si substrates, the samples have to be grown at low temperatures around 300 °C far in the meta-stable growth regime. Alternatively, by growing strain-symmetrized Si/SiGe layer sequences on SiGe pseudo-substrates, stable cascade structures with a virtually unlimited number of periods can be grown.

In contrast to the III-V system, where unipolar quantum cascade structures are usually formed in the conduction band, in the Si/SiGe system up to now most of the work related to cascade structures has been performed for valence band quantum wells. However, for growth on SiGe pseudosubstrates, also in the conduction band deep quantum wells can be formed. The recent experimental results presented for example in [1] – [3] are summarized and compared to band structure calculations. In these calculations, the heavy hole (HH), light hole (LH) and split off (SO) valence bands and their coupling due to the biaxial strain and finite inplane wavevectors are included by a Luttinger-Kohn-type $\mathbf{k}\cdot\mathbf{p}$ envelope function approach. Alternative designs for SiGe cascade structures will be discussed.

References:

[1] S. A. Lynch et al., Appl. Phys. Lett. **81**, 1543 (2002).

[2] G. Dehlinger et al., Science **290**, 2277 (2000).

[3] I. Borman et al., Appl. Phys. Lett. **80**, 2260 (2002).

In-situ Growth Monitoring and On-Line Composition Determination of MOCVD GaN by Spectroscopic Ellipsometry

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Group III nitrides have attracted tremendous R&D effort in the past few years resulting in the commercialization of optoelectronic devices operating in the blue and ultraviolet spectral range. Other fields of application include high mobility transistor devices (HEMT's), UV detectors and laser diodes for tomorrow's range of optical storage products. The fabrication of GaN layers is mostly done by Metalorganic Chemical Vapor Deposition (MOCVD), which provides high growth rates and throughput in a non-UHV environment. The range of real-time diagnostic tools for MOCVD reactors is however quite limited, as electron diffraction techniques like RHEED (reflection high energy electron diffraction) cannot be used at atmospheric pressure. Optical methods like spectroscopic ellipsometry (SE) or reflection difference spectroscopy (RDS) have been successfully employed for in-situ monitoring of III-V and II-VI compounds. We present a concept of optical growth monitoring for GaN and its related ternary compounds AlGaN and InGaN. A special reactor was designed to accommodate both a reflectometer and a spectroscopic ellipsometer operating in the visible and UV spectral range (1.5 - 5.2 eV). First efforts were dedicated towards the monitoring of standard growth procedures for hexagonal GaN on sapphire (0001) substrates. It can be shown that SE provides similar results to commercially available reflectometry setups but with an improved signal to noise ratio and a higher level of detail during critical steps of nucleation layer growth and annealing. Since there is very little published data of optical constants of the nitrides at higher temperatures, measurements of the dielectric function were carried out from room temperature to growth temperature (~1050 °C). This data was taken as a basis for the on-line composition determination of ternary AlGaN and InGaN layers. We use the virtual interface approximation together with external x-ray diffraction measurements to calculate Al and In contents of the growing layer. We also show possible applications to the growth of GaN/AlGaN superlattices and graded composition layers. While Al content monitoring is quite straightforward and produces good results, In content determination is difficult due to the miscibility gap in the GaN – InN system.

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