Study of Internal Behavior of BCD ESD Protection Devices under TLP and Very-Fast TLP Stress

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The internal behavior of BCD npn electrostatic discharge (ESD) protection devices is analyzed experimentally and by simulation. The device internal thermal and free carrier density distributions during TLP and vf-TLP stresses are studied by a backside transient interferometric mapping technique. Two current paths, one through a lateral npn transistor and one through a vertical npn transistor, are identified. The current flow along the width of the devices is homogeneous. This explains their high ESD ruggedness.

Introduction

The automotive industry requires protection against both the human body model (HBM) and the charged device model (CDM) electrostatic discharge stresses [1, 2]. Monitoring of the internal thermal behavior in such devices is significant for the understanding of device reliability and failure mechanisms [3, 4].

The transient interferometric mapping (TIM) technique is a powerful tool for the investigation of internal device behavior and provides information on thermal and free-carrier concentration dynamics and spatial distribution during an ESD event.

In this paper we investigate the internal device behavior of a bipolar-CMOS-DMOS (BCD) technology ESD protection device under 100 ns TLP and 10 ns vf-TLP stresses.

Device and Measurement Technique

Lateral npn ESD protection devices implemented in an 0.8 µm smart power process (BCD4) are studied. A simplified cross section of the device is shown in Fig. 1. The emitter/body contact was grounded and positive polarity pulses were applied to the collector contact during the investigations.

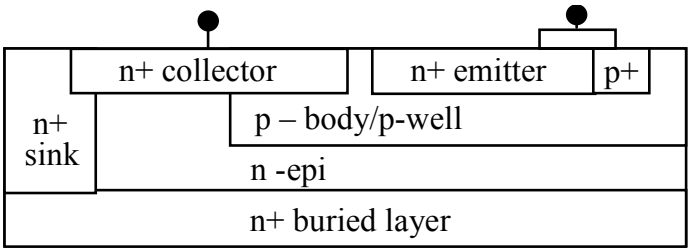

Fig. 1: Simplified cross sections of the studied device.

The high current IV characteristics were measured using 100 ns TLP and 10 ns vf-TLP pulsers.

The backside TIM is carried out by a scanning heterodyne interferometer setup [5]. An infrared laser beam of 1.3 µm wavelength is focused from the backside on a device and scans the device. The temperature and free-carrier induced phase shift of the reflected beam is then interferometrically detected. If the thermal effect dominates the measured phase shift $\Delta\varphi$ can be directly related to the two-dimensional thermal energy density E_{2D} in the device via the relation: $E_{2D}(x,y,t) = 0.88\ \Delta\varphi(x,y,t)$ (nJ/µm^2, rad) [6]. The phase shift is measured with 1.5 µm space and 3 ns time resolution.

Experimental Results

Figure 2 shows the high current IV characteristics of the device of width 100 µm measured by 100 ns TLP and 10 ns vf-TLP. The IV curve obtained by TLP bends from the IV obtained by vf-TLP at currents above 2 A, i.e., the differential resistance (R_{diff}) is higher for TLP stress. This can be attributed to a self-heating effect. The R_{diff} of the device at current levels below 2 A is the same for both TLP and vf-TLP types of stress. The $1/R_{diff}$ scales nearly linearly as a function of the device width in this range as can be seen in Fig. 3.

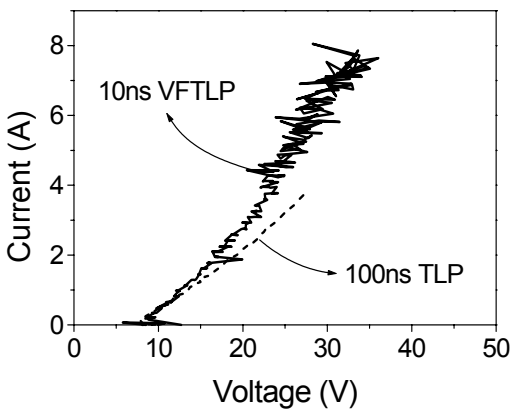

Fig. 2: High current IV characteristics of the device of width 100 µm measured by 10 ns vf-TLP and 100 ns TLP (after [4]).

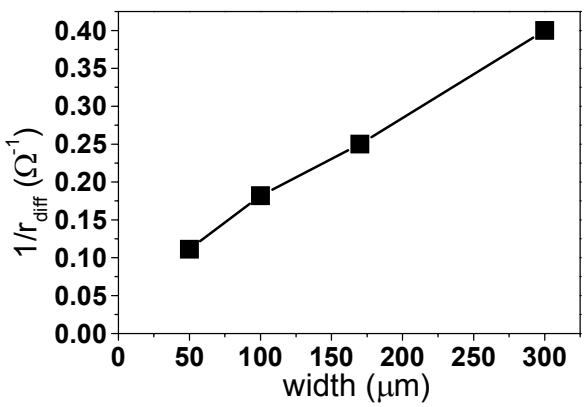

Fig. 3: Inverse differential resistance $1/R_{diff}$ as a function of device width (after [4]).

The ESD ruggedness of the device is high. The 170 µm wide device can sustain 4 A of TLP and 18 A of vf-TLP stress levels. These are the measurement setup limits.

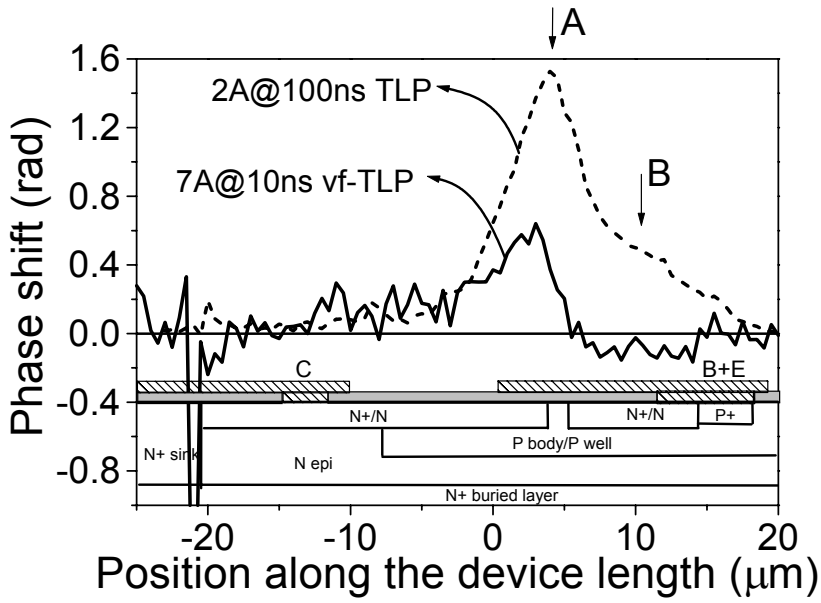

Fig. 4: Phase shift distribution along the device length measured at the pulse end of stresses of 2 A @ 100 ns (TLP) and 7 A @ 10 ns (vf-TLP). Aligned simplified cross section is also indicated (after [4]).

Figure 4 shows the phase shift distribution along the device length at the pulse end of two stress conditions: 100 ns TLP pulse with amplitude of 2 A and 10 ns vf-TLP pulses with amplitude of 7 A. An aligned simplified cross section of the device is also shown in Fig. 4. A dominant positive phase shift peak is located at the collector edge of the lateral npn transistor during both TLP and vf-TLP stresses (see A in Fig. 4). This peak arises from the heat dissipation in the reverse biased n^+-collector/p-body pn junction, which undergoes impact ionization. Another important area is located at the position of the n^+-emitter (see B in Fig. 4). The phase shift at the end of short vf-TLP stress is negative there. It arises from the increased free carrier concentration due to injection in the forward biased n^+-emitter/p-body junction, when the npn transistor is turned on. One can therefore expect also a positive phase shift due to heating related to the activity of a vertical npn transistor being present under the n^+-emitter. However, the temperature rise at pulse duration of 10 ns is insufficient to make the total phase signal positive. A positive thermal side-hump related to the heating in the vertical npn transistor can only be observed under longer pulses, as it can be seen on the phase shift profile measured at the end of a 100 ns long TLP stress pulse (see B in Fig. 4).

The activity of the vertical npn transistor depends on the stress current level. The phase shift distributions along the device length at three different TLP stress current levels are shown in Fig. 5. Let us concentrate on side hump (peak B in Fig. 5). It can be observed only at higher stress levels (I > 2 A). The phase shift peak B is more pronounced at the device corners, compared to the middle of the device. This can be seen on the measurements at I = 4 A, where the phase shift distribution is taken in the device middle (curve “M” in Fig. 5) and at one corner of the device (curve “C” in Fig. 5).

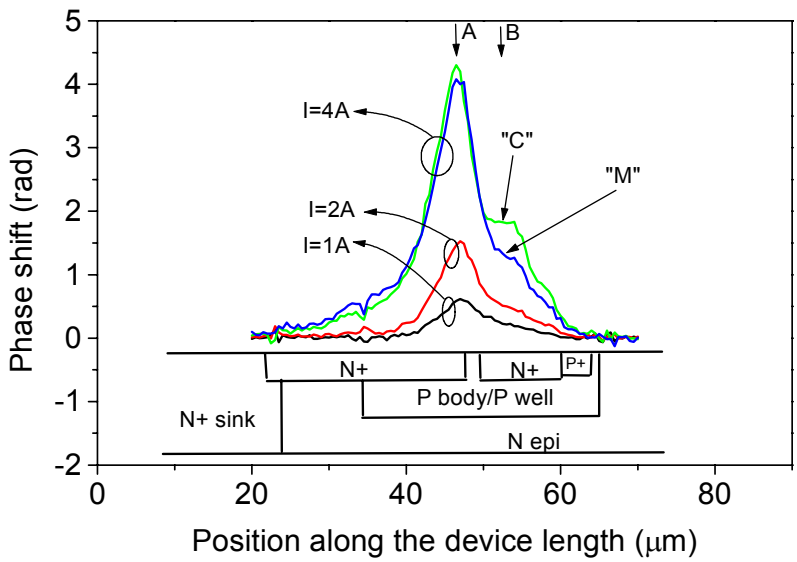

Fig. 5: Phase shift distribution along the device length as a function of TLP stress current. The inset shows a simplified device cross section (after [3]).

Homogeneity of the current flow along the width of the devices stressed by 10 ns vf-TLP pulses was also investigated. Figure 6 shows the phase shift distribution along the dominant hot spot (peak A in Fig. 4) in the devices of different widths stressed by the same current per device width. The optical mapping reveals very homogeneous current flow thus explaining linear scaling of the inverse differential resistance $1/R_{diff}$ as a function of the device width (see Fig. 3) and the high ESD ruggedness of the devices.

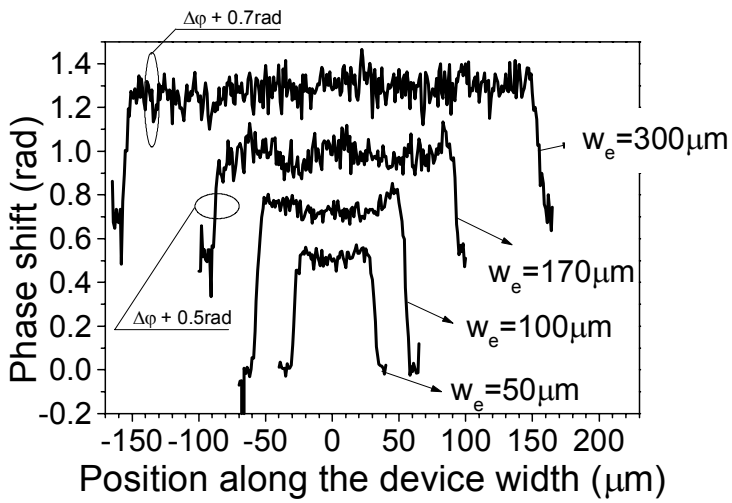

Fig. 6: Phase shift distribution at the end of stress 10 ns vf-TLP along the device width. The current density (current/width) was the same for all devices (after [4]).

Figure 7 shows the simulated heat dissipation in the device at t = 100 ns for the stress current pulse of 2.5 A. The main heat dissipation region is located at the lateral n^+-collector/p-body junction. This agrees with the experiment, because the dominant phase shift peak was observed at this place (see A in Fig. 4). The heat dissipating re-

gion is also observed at the n-epi/p-body junction under the n^+-emitter, which explains the existence of the side-hump observed experimentally at the end of 100 ns TLP pulses in this structure (see B in Fig. 4). This is the second region where the impact ionization takes place.

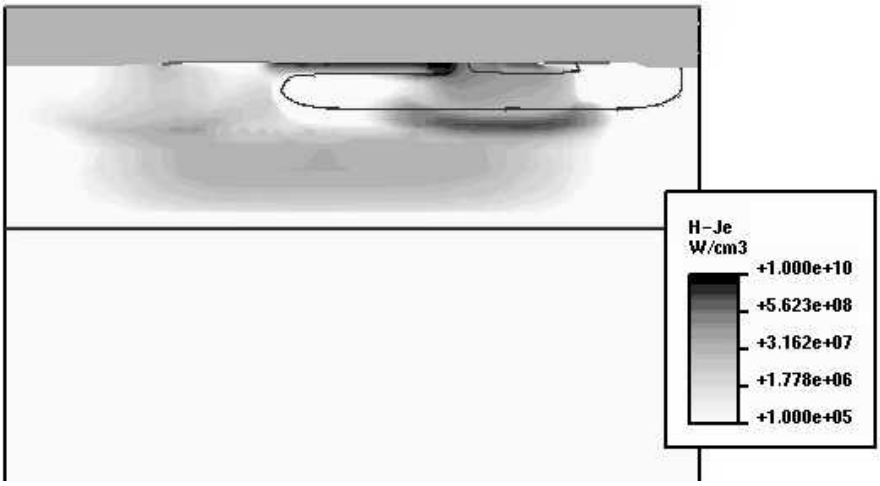

Fig. 7: Simulated heat dissipation due to electron current flow in the device at the end of 2.5 A @ 100 ns stress (after [4]).

Conclusions

The internal behavior of BCD ESD protection devices under TLP and vf-TLP stress was studied and compared. The device operation is dominated by the action of the lateral npn transistor. The n^+-collector/p-base junction of this transistor where impact ionization takes place was identified as the main heat-dissipating source. The activity of the vertical npn transistor is also identified in the device. The optical mapping along the device width has revealed homogeneous current flow. This is consistent with the scaling of the inverse differential resistance of the devices with their width. Thanks to the homogeneous current flow, devices also exhibit excellent ESD ruggedness in both HBM and CDM time domains.

Acknowledgements

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