SOI: Developments, Challenges, and Applications

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Silicon-on-Insulator (SOI) wafers significantly improve performance of electronic circuits. Initially, the driving force for developing SOI material was to increase radiation hardness of integrated circuits, i.e., improved immunity to single event upsets caused by ionizing particles. More recently, SOI applications entered the mainstream of digital electronics, where they provide increased switching speed of transistors and/or reduced power consumption – this is accomplished primarily because the source and drain capacitance is lowered by having an insulator layer below a MOSFET. As device gate length is scaled below 50 nm, thin SOI layers are becoming essential to maintain proper transistor action by suppressing the short-channel effects. Eventually, planar transistors will need to be replaced with double gates or with vertical transistors – SOI plays an important role in these novel device architectures as well.

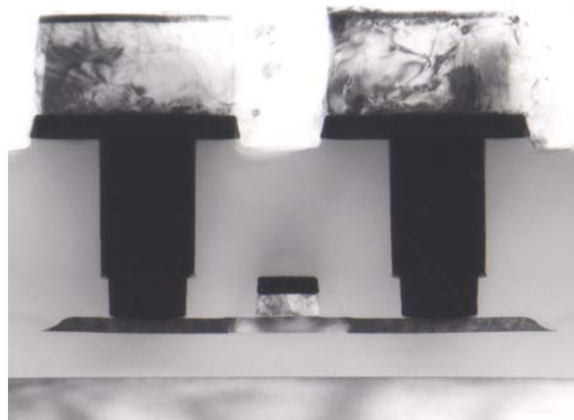

Fig. 1: A low magnification TEM cross section of a transistor made in SOI. The gate is 250 nm long and the buried oxide is 200 nm thick. W plugs make contacts to the source and drain (From Celler and Cristoloveanu [1]).

The dominant commercial method of fabricating SOI structures is known as the Smart Cut™ process, and it evolved from an invention by M. Bruel at LETI in Grenoble [2]. It utilizes ion implantation as an “atomic scalpel” to cut semiconductor crystals layers. Hydrogen doses $>5\times10^{16}$ cm^{-2} are typically used for splitting of silicon. For manufacturing SOI structures, the implanted surface is bonded to another wafer. As a function of temperature, depending on material and implant conditions, the pressure of hydrogen that accumulates in the microcavities and microcracks induced by the initial implantation eases splitting along the implanted zone. The net result is that a thin layer of Si, defined precisely by the implant depth, is transferred from a seed wafer to a handle wafer.

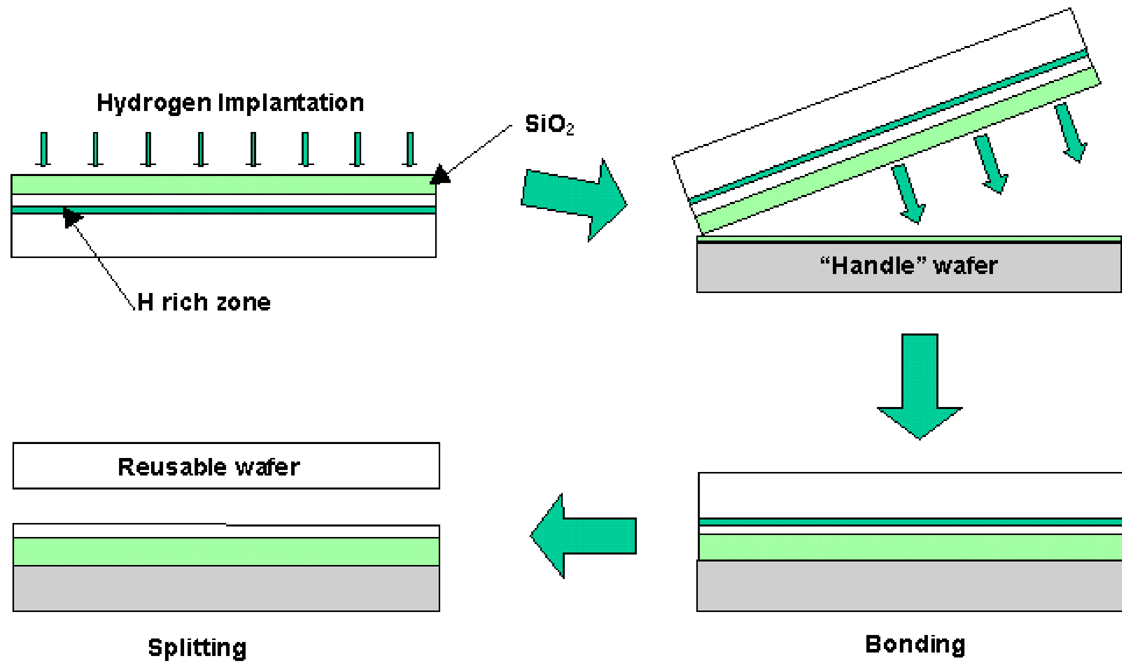

Fig. 2: A schematic representation of the Smart Cut™ process.

The Arrhenius plot in Fig. 3 shows the temperature dependence for thermally induced exfoliation [3]. At high temperatures, the activation energy for splitting is 0.5 eV and this energy is believed to be associated with diffusion of free atomic hydrogen in silicon (~0.48 eV). At low temperatures, the splitting activation energy is about 2.2 eV: hydrogen diffusion is still expected to occur, but this time it is linked to trapping-detrapping phenomena.

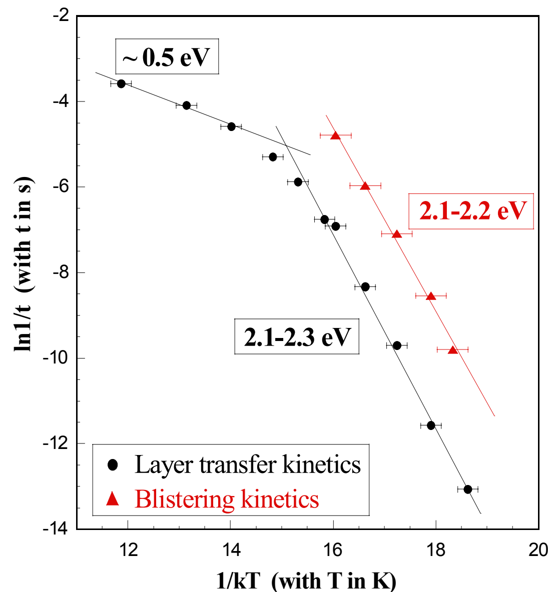

Fig. 3: Time necessary to transfer a thin layer or to obtain blistering in the absence of a stiffener, as a function of the annealing time (From Aspar and Auberton-Hervé [3]).

The Smart Cut™ process is a good example of a transition from an invention to technology, from fundamental scientific ideas based on the understanding of physics and materials to a major industrial activity that employs hundreds of people. Currently, uniform and continuous single crystalline Si films thinner than 100 nm are routinely transferred between 300 mm wafers. Such SOI wafers serve as substrates for high performance microprocessors that can be found not only in large computer servers but also in desktop systems, where they offer increased switching speed and reduced power dissipation.

The progression of CMOS technology nodes to smaller dimensions imposes a demand on scaling down of the SOI film thickness. Soitec roadmap for ultra-thin SOI wafers is shown in Table I [4]. The simultaneous requirements of thinner Si films and better thickness uniformity are a major technological challenge that necessitates steady improvements in surface finishing. Recent data demonstrated that 300 mm wafers with 20±2 nm (±3σ) Si films are feasible in a production environment [4].

Time line	**2000**	**2001**	**2002**	**2003-04**	**2004-05**
Process generation	**PD**	**FD**	**UT1**	**UT2**	**XUT**
Silicon Layer Thickness (Å)	**1000**	**500-700**	**200-700**	**200-300**	**200**
Si unif 6σ (Å)	**150**	**100**	**70**	**30**	**10**
Si unif 6σ; all wafers all sites (%)	**± 7 %**	**± 7 %**	**± 6 %**	**± 5 %**	**± 2.5 %**
Roughness AFM(RMS) • **1×1 µm** • **10×10 µm**	**1 Å** **1.5 Å**	**1 Å** **1.5 Å**	**1.5 Å** **3 Å**	**2 Å** **4 Å**	**2 Å** **5 Å**
Box Layer Thickness (Å)	**1500-2000**	**1000-1500**	**1000-1500**	**800-1500**	**800-1500**
Box Layer TTV	**± 4%**	**± 4%**	**± 3%**	**± 3%**	**± 3%**

Table I: Soitec roadmap for ultra-thin SOI wafers

The layer transfer made possible by the Smart Cut process can be applied to a variety of materials. Thin Si films can be transferred to fused silica (SOQ for Si-on-quartz) or glass substrates. Si devices on transparent insulating wafers have important electronic and photonic applications. Strained-Si-on-insulator (SSOI) combines benefits of SOI with enhanced mobility of charge carriers [5]. Strained Si is usually grown as a thin pseudomorphic layer on a virtual SiGe substrate and then a suitable layer can be transferred to an oxidized Si handle wafer. Bonding of single crystalline SiC, InP, and GaAs films to oxidized Si wafers has also been demonstrated.

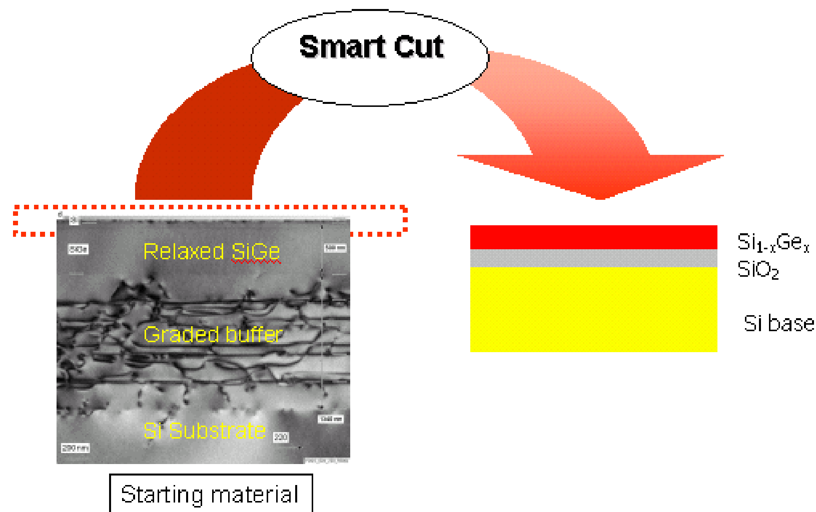

Fig. 4: An example of a relaxed SiGe film that is ready for transfer to an oxidized Si wafer in order to form SiGe-on-insulator (From Ghyselen *et al.* [6]).

In summary, the Smart Cut™ process makes possible production of large quantities of 200 and 300 mm SOI wafers that are used for high performance electronic circuits. Other applications that are emerging are SiGe-on-insulator, SSOI, SOQ, and the transfer of compound semiconductor layers to other substrates.

Acknowledgments

I would like to acknowledge many colleagues at Soitec who made this article possible, and in particular B. Ghyselen, C. Maleville, and C. Mazure.

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