Mixed-Signal Design for SoCs

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Introduction

System on Chip (SoC) has become a very popular term in the last years. Although there is no strict definition for it people usually agree that system on chip features

- a complete solution for a specific customers need
- high complexity
- different parts coming from different design worlds, such as digital + analog or RF.
- These three requirements also give some indication what the challenges or difficulties in SOC design are.

The first term largely applies for system know-how of the IC manufacturer. Providing system solutions usually does not mean to just do a chip design where the customer tells what it should look like and how to implement it. Providing system solutions means to take a greater part of the value chain: The chip provider has to understand the customers' need and actively participate in coming up with solution proposals. This incorporates not just electronic design but also application know-how as well as architectural and software considerations.

The second term is largely related to manufacturing skills. Of course we need high engineering capabilities in order to be able to design the system. But on top of that we also have to deliver at low cost. For competitiveness in this area – at least for digital chip area – we have to go to very advanced process technologies. Fig. 1 shows the development of DRAM complexity over time whereas Fig. 2 shows the price decline over time.

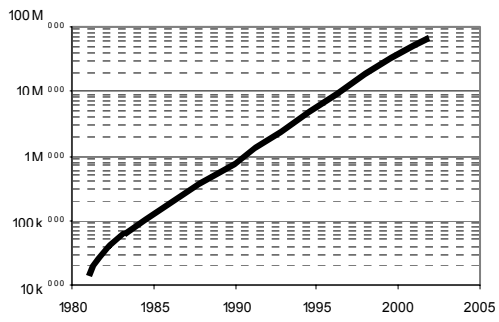

Fig. 1: DRAM: Complexity increase over time

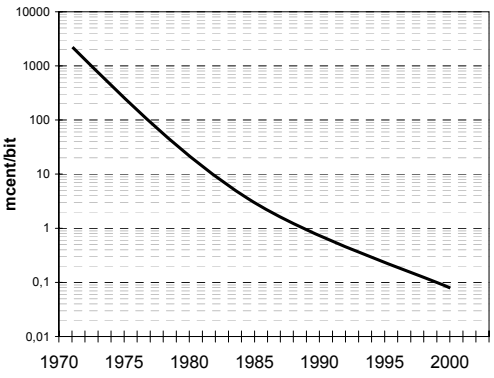

Fig. 2: DRAM: Price [milli-cent per bit] decline over time

The message is very clear: In not even 30 years we have a price decline of 10.000 (ten thousand) for a given function, which in this case is one bit of memory capability. The

reason for this is undoubtedly the rapid development in process technology, which allows the integration of an exponentially growing amount of transistors at a moderate increase in manufacturing cost. On the other hand this figure also means a cost disadvantage in taking a somewhat old-fashioned technology, at least for heavy mass production.

The third term relates to engineering skills. A major impact on the competitiveness of the system comes from architectural considerations: Analog versus digital, serial versus parallel processing quite often is a nontrivial choice. Another challenge stems from the fact that design methodologies for different worlds like analog and digital are quite incompatible. In order to cope with the increasing complexity we try to model the chip at always higher abstraction levels. But analog design still relies on SPICE-type simulators. There are lots of efforts also in the EDA-industry to fill that gap but it seems that design complexity is growing faster than the processing capability of design and simulation tools. Therefore major success factors are design style and design methodology.

Design Examples of MS-SoCs

As the issue of this paper is to demonstrate recent MS-designs, we will now focus more on the analog side being part of some more complex MS-chip. For communication ICs this implies noise immunity as well as advanced signal processing speeds. Noise immunity is important for suppressing digitally induced switch noise, whereas the speed requirement comes from always increasing bandwidths. Typical examples for this are the cellular phone business, where the GSM-standard has been developed over GPRS towards UMTS, or the development from ISDN via ADSL towards VDSL in wireline communication. A typical example for a high speed ADC targeted as a key component in a VDSL system [1] is shown in [2]. Another example for an ADSL system can be found in [3]. In order to get the desired performance out of the converters we need high-quality clock sources (e.g., [4]).

In the area of automotive chips the challenges are usually different: Instead of getting high complexity in standard CMOS we face the problems of power handling and design robustness against ambient conditions. [5] shows an example for a mixed signal hall-sensor IC, where the internal self-calibration algorithm guarantees superior sensing accuracy. [6] is an example of a highly robust analog module. In the following a short summary about key challenges and features of selected blocks will be presented.

A 1.8 V 450 mW VDSL 4-Band Analog Front End IC in 0.18 µm CMOS

A highly integrated analog front-end (AFE) chip was designed in a 0.18 µm CMOS process using 1.8 Volts supplies only. All the receiver and transmitter functionality is included in a single chip. The receiver dynamic range requirement is achieved by the use of a 32 dB programmable gain amplifier (PGA) followed by an 11 bit ADC. The prefilter (PREFI) removes high frequency signals which would cause aliasing in the sampling operation of the ADC. For partial compensation of the line attenuation at high frequencies an analog channel equalizer (ACE) is implemented. Transmit functionality is provided by the 12 bit DAC, a reconstruction filter (POFI), and a programmable gain amplifier (POCO). On chip clock generation is performed with a digitally controlled crystal oscillator and a PLL. In sleep mode, only the clock generation and the wake up circuit are active, consuming 40 mWatts of power. The AFE is designed with fully differential circuits taking a chip area of 7.5 mm².

A Fully Embedded 10 b 160 MS/s Two-Step ADC in 0.18 µm CMOS

For broadband wireline and wireless communication systems Nyquist-analog/digital converters with a resolution of 10 bits, sampling rates in excess of 100 MS/s and signal bandwidths up to 50 MHz are needed. Especially in portable applications, low power consumption is an additional constraint. The two-step subranging approach offers both low latency and small chip area as compared to pipeline-converters of the same resolution, together with low power consumption. Since in highly integrated system-on-chip (SoC) solutions the number of available pins for the analog part is severely limited, a fully embedded solution is required including on-chip reference generation and adequate input signal buffering.

The 10 bit ADC with 160 MHz sampling rate was designed in 0.18 µm CMOS. It has a silicon area of 1 mm² and a total power consumption of 190 mW. Target applications include VDSL, Cable modem and DVB-T system solutions using COFDM modulation.

A 14-Bit Delta-Sigma Modulator for ADSL-CO Applications in 0.18 µm CMOS

A high-resolution multi-bit Sigma-Delta ADC implemented in a 0.18 µm CMOS technology is introduced. Active blocks are composed of regular threshold voltage devices only. The circuit is targeted for an ADSL Central-Office (CO) application. An area- and power-efficient realization of a 2^{nd}-order, single-loop, 3-bit modulator with high oversampling ratio (OSR=96) was developed. The $\Sigma\Delta$ - modulator features an 85 dB dynamic range over a 300 kHz signal bandwidth. The measured power consumption of the ADC core is 15 mW only.

New technologies require several cascaded transistor stages to provide sufficient DC gain and high output voltage swing such as a two stage Miller OpAmp. A two stage Miller OpAmp consumes relatively high power drain in the 2^{nd} transistor stage for providing appropriate phase margin and sufficient internal slew rate. However, SC integrators do not require high dynamic performance during the sampling phase. This allowed us to reduce the bias current to 1/3 of the integration phase value. The dynamic biasing technique of both integrators is driven by the rhythm of the clock signal and so uncorrelated to the signal. This solution offers the possibility to reduce the rms value of current consumption of about 30%.

A Sub-psec Jitter PLL for Clock Generation in 0.12 µm Digital CMOS

In today's chip architectures a clean clock source very often is a basic requirement. A very low phase noise and thus integrated jitter clock is a prerequisite for high-speed transceiver circuits, or sampling applications using high performance AD and DA converters. For such low jitter PLLs it is essential not only to use a low jitter VCO (like LC-VCO). One must optimize every block to get low phase noise over the full frequency span. The PLL loop is a classical charge pump PLL and is fully integrated. To minimize supply and substrate noise injection all clock and analog signal paths are differential. The phase frequency detector has been built with differential PPCL NAND gates. The combination of a fully differential charge pump with an active differential loop filter leads to reduced spurious tones at the PLL output and low ohmic outputs to drive the LC-VCO varactors. The associated common mode feedback loops present also some design and stability challenges. In order to meet the specifications for 2.488 GHz and 3.11 GHz output frequencies, two LC-VCOs have been implemented on chip. They are separated from each other and operated alternatively. The LC-VCOs are fully integrated and their differential tuning is obtained with NMOS and PMOS varactors. The fast prescalers are implemented in CML logic, in order to have reduced noise injection in the power supply lines.

A Mixed-Signal Hall Sensor IC with Direction Detection

Magnetic Sensors based on the Hall effect have been well established for automotive applications like sensing of rotating target wheels, e.g. for crankshaft, camshaft, gearbox or wheel speed detection. For reliable operation magnetic differential fields ranging from ±100 mT down to approx. ±1 mT (which corresponds to a hall voltage of about 100 µV) superimposed by homogenous bias fields up to several ±100 mT have to be resolved in an automotive environment. The sensor can be supplied directly by the 12V board net. Major requests are:

- Tj=-50°C up to 210°C
- Supplies between 4.5V and approx. 24V
- Immunity against supply ripple and radiated energy
- Insensitivity to bias field and amplitude modulations
- Fast signal detection at start up or supply interruption

An additional challenge is caused by the current interface: The chip modulates its own supply current to signal “high” or “low” logic states. This leads to thermal transients propagating through the chip influencing biasing conditions as well as differential pairs and the highly sensitive hall probes. Therefore we had to establish a layout floor plan which takes into account noise separation as well as thermal interaction. For getting the desired sensing accuracy we have defined a mixed-signal architecture which contains a straight forward analog signal path for analog robustness. Accuracy and start-up considerations are tackled in the digital domain. The self-calibration algorithm forms a negative feedback loop which measures the analog signal quality and adjusts system parameters like offset via D/A-converters accordingly.

A Robust Smart Power Bandgap Reference Circuit for Use in an Automotive Environment

Bandgap reference circuits represent a key block in most smart power circuits. For automotive use, their functionality and accuracy under harsh environmental conditions is crucial for the IC’s performance.

One issue is the extremely high operating temperature which can, under failure conditions, reach 220 °C or more. Since the bandgap function is needed for a controlled shut-down, safe and reliable operation has to be guaranteed also at these temperatures. In addition, especially automotive power handling circuits suffer from minority carrier injection into the substrate due to over- or undershoots. They represent collector currents into any junction embedded into the substrate and can cause disturbances in sensitive analog circuits, e.g., the bandgap reference.

To overcome the problems of minority-carrier (i.e., electron) injection into the substrate and the issue of high-temperature junction-leakage currents, we have developed a new topology for the bandgap reference circuit. In this topology, all n-wells which are potential collectors of the parasitic n-p-n transistor are supplied by a low-impedance path to ensure that parasitic currents at these nodes will not affect the circuit’s performance. Since the largest junction-leakage currents at high temperatures also occur at these nodes, the new topology also shows excellent performance at very high junction temperatures.

Measurements show that parasitic currents do not disturb the functionality of the new bandgap reference which operates accurately up to 260°C.

Future Trends

Whereas the previous examples demonstrate the state of the art we will now try to extrapolate today's findings into the future. A well-suited instrument for this is the ITRS (International Technology Roadmap for Semiconductors) [7]. What we have seen in the past is the shrinking of feature sizes in general. This leads to higher speed, and lower power dissipation and cost per function. Process technology developments were mainly driven by the requirements of digital chips, and the analog circuits had to adapt to that. But to be honest – with the addition of linear resistors and capacitors most of the so defined processes were quite suitable to analog circuit design as well. Will this prolong in future?

The first thing we can note from the ITRS is that the development of digital process technologies will not be as smooth as in the past. We see that even for logic we can find three different roadmaps. One for "High performance logic", one for "Low operating power", and one for "Low standby power". As time passes, these three branches are predicted to diverge even further. In the year 2001 the roadmap sees at least the same supply voltage for all of them, which is 1.2 V. In the year 2007 the nominal supply voltages show a spread between 0.7 V and 1.1 V. At first sight it seems astonishing that the lower power we want to achieve the higher the supply voltage is. This is in some contradiction to the well-known practice that supply reduction helps in saving power. In order to understand this we have to go to a different viewpoint. If we look into the "High performance logic"-table again we see that the subthreshold leakage current goes from 10 nA/µm width in 2001 to 1 µA/µm in 2007. Having a full chip of such leaky devices leads to an unacceptable high leakage level in many applications. Assuming e.g. 10 mio. gates with 1 µA leakage each we end up at 10 A leakage current. And this is for room temperature with a significant increase towards higher temperatures. So we learn that many applications in future are just power-limited. With a given subthreshold slope of approx. 85 mV/decade the only way to reduce this leakage current is to increase the threshold voltage. This, however, leads to slower transistors. In order to speed them up we have to use a larger gate overdrive which leads to a larger supply voltage. This again leads to higher switching power dissipation. So this scenario makes only sense when most of the power is coming from static leakage power and it is of primary importance to reduce this. At the bottom line we find out that if we want do optimize for low power consumption we have to balance static against dynamic power dissipation and the optimization result depends on factors like the activity of the circuit and the acceptable delay time. Depending on this we find optimums requiring different transistor parameters causing different process flows.

Another trend we see is that useful analog supply voltages divert more and more from digital supply voltages. The "Mixed-signal device technology roadmap" shows a typical analog supply voltage of 1.8 – 2.5 V in the year 2007. Since the digital supply voltage tends to go down whereas the analog supply voltage stays more or less constant the gap between analog and digital gets even bigger. In addition to that even for plain digital circuits we see that the cost per wafer further goes up due to increasing process complexity and increasing equipment cost. As long as analog functions can live with the options provided by the digital process this will be ok for analog. So, if analog circuit parts can be designed with the digital core devices, eventually using digital I/O devices for getting higher supply voltages, this does not add extra cost. However, if analog circuits are requiring transistors for their own, it is quite likely that this will be just a cost overhead as compared to multi-chip solutions. It should be noted that the big success of SoCs was not due to the elegance of this approach, it was mainly because it also was a cost optimum. So the future of SoCs will greatly depend on the ability of system architects and analog designers if they continuously will manage to deal with processes mainly defined for digital use.

References

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