

Wafer Bonding and Strained-Layer Silicon

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Wafer bonding refers to a process in which two mirror polished wafers of almost any material are brought into contact and hold together permanently if treated properly. Over the last 20 years wafer bonding has moved from a kind of exotic phenomenon of limited technological interest towards a potential future mainstream technology especially in the context of silicon-on-insulator (SOI) applications. The talk will cover the historical development of wafer bonding and the basic physics and chemistry involved. Different bonding technologies will be touched upon including those which are still in a lab stage like ultra-high vacuum bonding which allows bonding at room temperature with full bonding strength. The talk will mainly deal with silicon but will also mention the bonding of other materials such as III-V compounds. Thinning and layer-splitting technologies will be mentioned shortly. Details of the “smart-cut” approach will be covered in the subsequent talk from SOITEC Company. Various applications of wafer bonding as a generic materials integration approach will be covered including SOI, micromechanics, LEDs and photonic crystals. In a final part the area of strained silicon layers will be discussed which allow an increased electron and hole mobility. In the long run it will be desirable to obtain highly strained silicon layers on insulator (SSOI). Different competing relaxation approaches of SiGe layers and subsequent Si layer growth and layer transfer by wafer bonding will be presented.