GMe Forum 2003

PROCEEDINGS OF THE SEMINAR
AT THE VIENNA UNIVERSITY OF TECHNOLOGY

ORGANIZED BY THE SOCIETY FOR MICROELECTRONICS
(GESELLSCHAFT FÜR MIKROELEKTRONIK – GMe)

April 10 – 11, 2003

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April 10 – 11, 2003

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Preface

In spring 1977, the first Austrian microelectronics technology seminar took place in Grossarl, Salzburg, under the title "*Technologie in der Mikroelektronik*" ("*Technology in Microelectronics*"), primarily intended as a workshop for Austrian university researchers in this field. A long series of biennial seminars in Grossarl followed, the first of which were organized by a group of institutes at the Vienna University of Technology. Later, after the Society for Microelectronics (*Gesellschaft für Mikroelektronik*; GMe) had been founded in the mid-1980s, the GMe coordinated the seminars. This sequence of seminars continued in 1999 at a new venue, Bad Hofgastein, and with a new title, "*Current Developments of Microelectronics*". With the change of the seminar venue from Grossarl to Bad Hofgastein the scope of the seminar shifted: Great efforts had been made particularly during the 1990s to invite guest speakers from industry or foreign universities, however, the audience consisted practically exclusively of university researchers. Beginning with the 1999 seminar in Bad Hofgastein, the seminar was designed to appeal to a more application-oriented audience. This trend continued in 2001 when the organizers decided to hold the seminar at a more central place, i.e., at the Vienna University of Technology, thereby facilitating the participation of representatives of foreign and Austrian industry and government. To reflect more clearly the new target of the seminar, its title was changed to "*GMe Forum*". Most of the oral presentations are now review papers presented by top-level speakers from international industry and research facilities. The institutions supported by the GMe also present their results, partly as oral presentations but mostly as posters.

The main goal of the Society for Microelectronics (GMe) is to promote microelectronics research and technology at Austrian universities and to establish links to the Austrian industry. The GMe is essentially financed by the government and supports relevant microelectronics activities at Austrian universities. The relatively small budget of the GMe prohibits the full sponsoring of research projects. Nevertheless, the GMe supplements other research funding sources by providing contributions for creating and maintaining laboratory infrastructure. In addition to backing other technological activities in the fields of design, sensors, and optoelectronics, the main goal of the GMe in recent years was the support of the two clean room centers at the Vienna University of Technology and at the Johannes Kepler University Linz, respectively, where internationally competitive technological equipment has been made available to researchers and students.

We hope that the proceedings will promote the impact of the *GMe Forum 2003*, and that they may contribute to an even better international cooperation of the Austrian microelectronics researchers.

o.Univ.Prof. Dr. Erich GORNIK
President of the GMe

Ao.Univ.Prof. Dr. Karl RIEDLING
Secretary General of the GMe

Forum Program

Thursday, April 10, 2003

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	P. SKALICKY (President of the Vienna University of Technology)
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Friday, April 11, 2003

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Insulating Films:

Transport Phenomena:

Sensors:

ESD Protection Devices:

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Contents

SOI and Waferbonding

Wafer Bonding and Strained-Layer Silicon

U. Goesele and S. Christiansen
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Wafer bonding refers to a process in which two mirror polished wafers of almost any material are brought into contact and hold together permanently if treated properly. Over the last 20 years wafer bonding has moved from a kind of exotic phenomenon of limited technological interest towards a potential future mainstream technology especially in the context of silicon-on-insulator (SOI) applications. The talk will cover the historical development of wafer bonding and the basic physics and chemistry involved. Different bonding technologies will be touched upon including those which are still in a lab stage like ultra-high vacuum bonding which allows bonding at room temperature with full bonding strength. The talk will mainly deal with silicon but will also mention the bonding of other materials such as III-V compounds. Thinning and layer-splitting technologies will be mentioned shortly. Details of the “smart-cut” approach will be covered in the subsequent talk from SOITEC Company. Various applications of wafer bonding as a generic materials integration approach will be covered including SOI, micromechanics, LEDs and photonic crystals. In a final part the area of strained silicon layers will be discussed which allow an increased electron and hole mobility. In the long run it will be desirable to obtain highly strained silicon layers on insulator (SSOI). Different competing relaxation approaches of SiGe layers and subsequent Si layer growth and layer transfer by wafer bonding will be presented.

SOI: Developments, Challenges, and Applications

G.K. Celler

Soitec USA, 2 Centennial Drive, Peabody, MA 01960, USA

Silicon-on-Insulator (SOI) wafers significantly improve performance of electronic circuits. Initially, the driving force for developing SOI material was to increase radiation hardness of integrated circuits, i.e., improved immunity to single event upsets caused by ionizing particles. More recently, SOI applications entered the mainstream of digital electronics, where they provide increased switching speed of transistors and/or reduced power consumption – this is accomplished primarily because the source and drain capacitance is lowered by having an insulator layer below a MOSFET. As device gate length is scaled below 50 nm, thin SOI layers are becoming essential to maintain proper transistor action by suppressing the short-channel effects. Eventually, planar transistors will need to be replaced with double gates or with vertical transistors – SOI plays an important role in these novel device architectures as well.

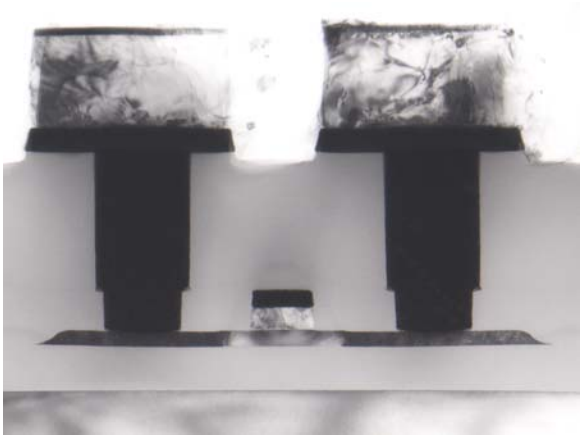

Fig. 1: A low magnification TEM cross section of a transistor made in SOI. The gate is 250 nm long and the buried oxide is 200 nm thick. W plugs make contacts to the source and drain (From Celler and Cristoloveanu [1]).

The dominant commercial method of fabricating SOI structures is known as the Smart Cut™ process, and it evolved from an invention by M. Bruel at LETI in Grenoble [2]. It utilizes ion implantation as an “atomic scalpel” to cut semiconductor crystals layers. Hydrogen doses >5×10^{16} cm^{-2} are typically used for splitting of silicon. For manufacturing SOI structures, the implanted surface is bonded to another wafer. As a function of temperature, depending on material and implant conditions, the pressure of hydrogen that accumulates in the microcavities and microcracks induced by the initial implantation eases splitting along the implanted zone. The net result is that a thin layer of Si, defined precisely by the implant depth, is transferred from a seed wafer to a handle wafer.

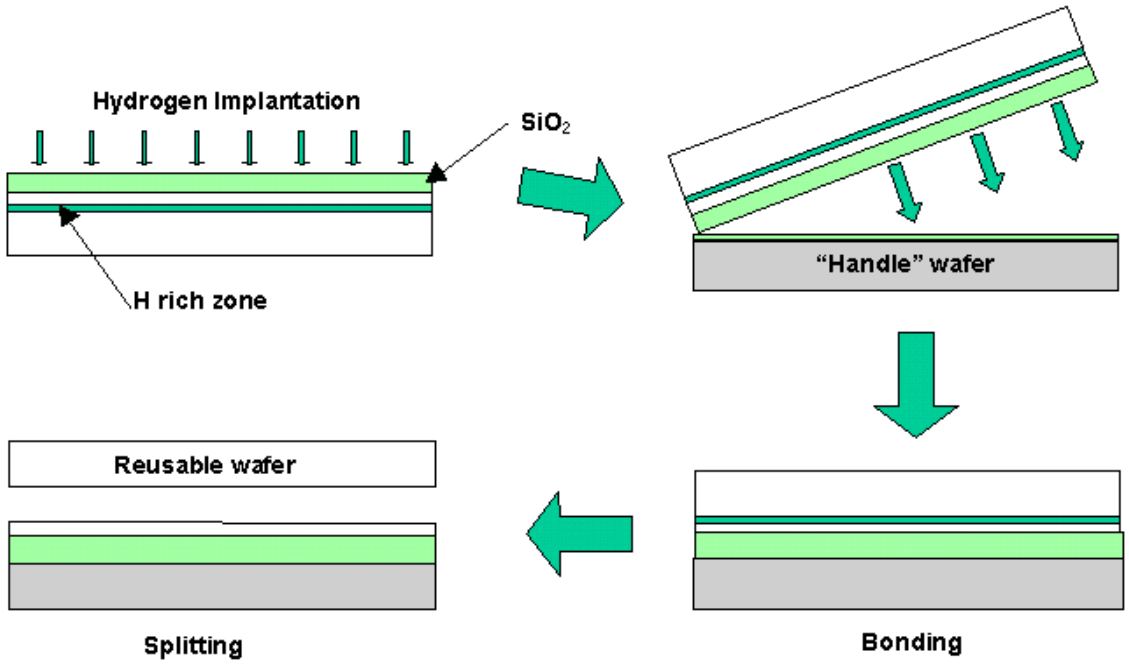

Fig. 2: A schematic representation of the Smart Cut™ process.

The Arrhenius plot in Fig. 3 shows the temperature dependence for thermally induced exfoliation [3]. At high temperatures, the activation energy for splitting is 0.5 eV and this energy is believed to be associated with diffusion of free atomic hydrogen in silicon (~0.48 eV). At low temperatures, the splitting activation energy is about 2.2 eV: hydrogen diffusion is still expected to occur, but this time it is linked to trapping-detrapping phenomena.

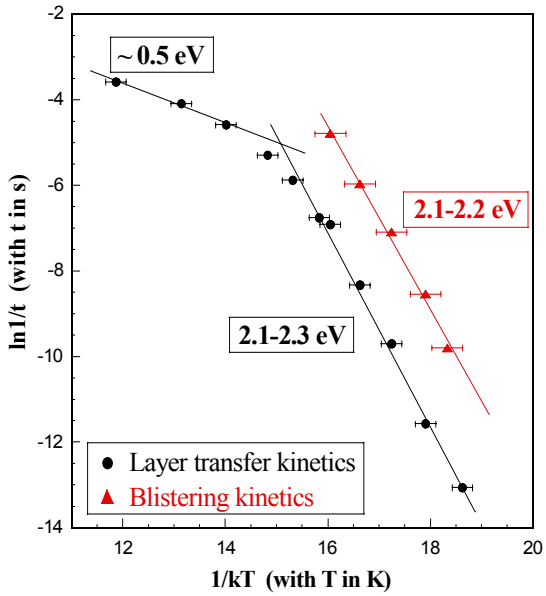

Fig. 3: Time necessary to transfer a thin layer or to obtain blistering in the absence of a stiffener, as a function of the annealing time (From Aspar and Auberton-Hervé [3]).

The Smart Cut™ process is a good example of a transition from an invention to technology, from fundamental scientific ideas based on the understanding of physics and materials to a major industrial activity that employs hundreds of people. Currently, uniform and continuous single crystalline Si films thinner than 100 nm are routinely transferred between 300 mm wafers. Such SOI wafers serve as substrates for high performance microprocessors that can be found not only in large computer servers but also in desktop systems, where they offer increased switching speed and reduced power dissipation.

The progression of CMOS technology nodes to smaller dimensions imposes a demand on scaling down of the SOI film thickness. Soitec roadmap for ultra-thin SOI wafers is shown in Table I [4]. The simultaneous requirements of thinner Si films and better thickness uniformity are a major technological challenge that necessitates steady improvements in surface finishing. Recent data demonstrated that 300 mm wafers with 20±2 nm (±3σ) Si films are feasible in a production environment [4].

Time line	**2000**	**2001**	**2002**	**2003-04**	**2004-05**
Process generation	**PD**	**FD**	**UT1**	**UT2**	**XUT**
Silicon Layer Thickness (Å)	**1000**	**500-700**	**200-700**	**200-300**	**200**
Si unif 6σ (Å)	**150**	**100**	**70**	**30**	**10**
Si unif 6σ; all wafers all sites (%)	**± 7 %**	**± 7 %**	**± 6 %**	**± 5 %**	**± 2.5 %**
Roughness AFM(RMS) • **1×1 µm** • **10×10 µm**	**1 Å** **1.5 Å**	**1 Å** **1.5 Å**	**1.5 Å** **3 Å**	**2 Å** **4 Å**	**2 Å** **5 Å**
Box Layer Thickness (Å)	**1500-2000**	**1000-1500**	**1000-1500**	**800-1500**	**800-1500**
Box Layer TTV	**± 4%**	**± 4%**	**± 3%**	**± 3%**	**± 3%**

Table I: Soitec roadmap for ultra-thin SOI wafers

The layer transfer made possible by the Smart Cut process can be applied to a variety of materials. Thin Si films can be transferred to fused silica (SOQ for Si-on-quartz) or glass substrates. Si devices on transparent insulating wafers have important electronic and photonic applications. Strained-Si-on-insulator (SSOI) combines benefits of SOI with enhanced mobility of charge carriers [5]. Strained Si is usually grown as a thin pseudomorphic layer on a virtual SiGe substrate and then a suitable layer can be transferred to an oxidized Si handle wafer. Bonding of single crystalline SiC, InP, and GaAs films to oxidized Si wafers has also been demonstrated.

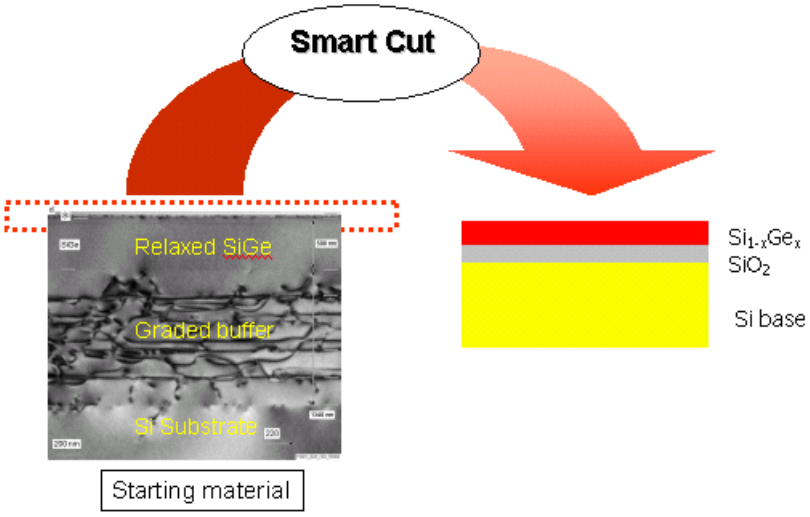

Fig. 4: An example of a relaxed SiGe film that is ready for transfer to an oxidized Si wafer in order to form SiGe-on-insulator (From Ghyselen *et al.* [6]).

In summary, the Smart Cut™ process makes possible production of large quantities of 200 and 300 mm SOI wafers that are used for high performance electronic circuits. Other applications that are emerging are SiGe-on-insulator, SSOI, SOQ, and the transfer of compound semiconductor layers to other substrates.

Acknowledgments

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Key Enabling Process Technologies for Advanced Semiconductors, MEMS and Nanomanufacturing

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New technologies like wafer level packaging, MEMS and Nanosystems frequently adopt semiconductor manufacturing processes at an early stage. Specific novel process steps however often develop to become key enabling. The paper will focus on two examples of key enabling process steps: wafer bonding and nano imprint lithography.

Wafer bonding enabled first the economic manufacturing of MEMS devices. Technological reasons for the success of the process in the MEMS community are mainly threefold:

- A bonded wafer stack forms a sealed “first level package” and therefore protects fragile micro machined features from harsh environments occurring during dicing.
- Allows to encapsulate a controlled ambient (like vacuum) to control a device’s sensitivity and adjust the properties.
- Stress Isolation: The first level package created at wafer level isolates mechanical stress introduced by the final package (mold or mounting method to board).

In addition, advanced semiconductors found benefit in the bonding technology through:

- Optical and electrical interconnects (3D interconnects) can be formed at wafer level rather than chip level in order to increase the integration density or the functional density of a device.
- Creation of chip scale packages at wafer level.
- New starting materials for advanced semiconductor and MEMS devices (most prominent example is the SOI Wafer).
- The ability to handle thin and ultra thin wafers for advanced power devices and compound semiconductors.

Examples of devices that utilize above mentioned benefits will be given as well as an overview of wafer bonding methods.

Classical lithography in semiconductor mainstream IC production employs stepper technologies today. Challenges and costs of this technology are steeply increasing at structures below 130 nm. Nano imprinting is a new method for generating pattern in submicron range at reasonable cost. It therefore has the potential for a wide variety of applications in BioMEMS, Biofluidics, Microoptics and Nanotechnology.

The paper will give an overview on emerging Nano Imprint Lithography (NIL) technologies:

- Hot Embossing (HE) which uses increased temperature to imprint a hard stamp into a polymer.

- UV Imprinting (UV Molding) which utilizes UV irradiation to cure a polymer between stamp and substrate.
- Micro Contact Printing (µCP) which transfers a self assembled monolayer (SAM) from a stamp to a substrate surface.

Equipment and tool technology was developed in the past years to support these new emerging imprinting methods.

About EV Group

EV Group (EVG), founded in 1980, is headquartered in Schärding, Austria and has subsidiaries in Phoenix, Arizona, Cranston, Rhode Island and Yokohama, Japan as well as representatives around the world. EVG manufactures a full line of wafer bonders, mask and bond aligners, photoresist coating systems and cleaners for microelectromechanical systems (MEMS) and semiconductor market segments. EVG's systems are used worldwide in high-volume production environments as well as research and development facilities. For more information visit the EVG web site at www.EVGroup.com, e-mail p.lindner@evgroup.at, or call EVG directly at +43 7712 5311-0.

Semiconductor Intellectual Property

The Silicon Intellectual Property Industry

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In the mid 1990s a new breed of companies emerged: commercial semiconductor intellectual property providers. These SIP firms focus on the development of IP; instead of taking it to production in the form of a complete IC design, they license their technology to IDMs, ASIC vendors, fabless semiconductor manufacturers and to the semiconductor groups of system OEMs who in turn integrate the licensed IP cores into their IC designs. IP companies do not sell chips – they provide technology that will be embedded in their customer's IC designs, hence the term "chipless" company.

The SIP business model can be seen as an extension to the fabless model and to the silicon foundry business model. Silicon foundries enabled fabless companies to capitalize on their design and system expertise without having to invest in a manufacturing facility. Now, the IP companies capitalize on their IC design and system know-how without having to go all the way to IC production.

Commercial intellectual property is the latest phase of the vertical disintegration process of the semiconductor industry. Independent IP providers now challenge one of the last remaining core competencies of semiconductor vendors, the creation of IP and IC designs. Enabled by the availability of third part IP and IC design services, a semiconductor company can be reduced theoretically to a marketing and sales department supported by a logistics group that handles all outsourcing partners.

System on a Chip

Mixed-Signal Design for SoCs

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Introduction

System on Chip (SoC) has become a very popular term in the last years. Although there is no strict definition for it people usually agree that system on chip features

- a complete solution for a specific customers need
- high complexity
- different parts coming from different design worlds, such as digital + analog or RF.
- These three requirements also give some indication what the challenges or difficulties in SOC design are.

The first term largely applies for system know-how of the IC manufacturer. Providing system solutions usually does not mean to just do a chip design where the customer tells what it should look like and how to implement it. Providing system solutions means to take a greater part of the value chain: The chip provider has to understand the customers' need and actively participate in coming up with solution proposals. This incorporates not just electronic design but also application know-how as well as architectural and software considerations.

The second term is largely related to manufacturing skills. Of course we need high engineering capabilities in order to be able to design the system. But on top of that we also have to deliver at low cost. For competitiveness in this area – at least for digital chip area – we have to go to very advanced process technologies. Fig. 1 shows the development of DRAM complexity over time whereas Fig. 2 shows the price decline over time.

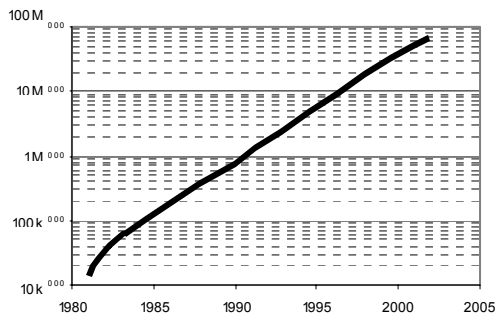

Fig. 1: DRAM: Complexity increase over time

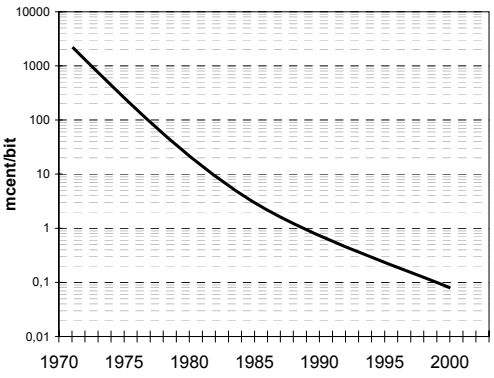

Fig. 2: DRAM: Price [milli-cent per bit] decline over time

The message is very clear: In not even 30 years we have a price decline of 10.000 (ten thousand) for a given function, which in this case is one bit of memory capability. The

reason for this is undoubtedly the rapid development in process technology, which allows the integration of an exponentially growing amount of transistors at a moderate increase in manufacturing cost. On the other hand this figure also means a cost disadvantage in taking a somewhat old-fashioned technology, at least for heavy mass production.

The third term relates to engineering skills. A major impact on the competitiveness of the system comes from architectural considerations: Analog versus digital, serial versus parallel processing quite often is a nontrivial choice. Another challenge stems from the fact that design methodologies for different worlds like analog and digital are quite incompatible. In order to cope with the increasing complexity we try to model the chip at always higher abstraction levels. But analog design still relies on SPICE-type simulators. There are lots of efforts also in the EDA-industry to fill that gap but it seems that design complexity is growing faster than the processing capability of design and simulation tools. Therefore major success factors are design style and design methodology.

Design Examples of MS-SoCs

As the issue of this paper is to demonstrate recent MS-designs, we will now focus more on the analog side being part of some more complex MS-chip. For communication ICs this implies noise immunity as well as advanced signal processing speeds. Noise immunity is important for suppressing digitally induced switch noise, whereas the speed requirement comes from always increasing bandwidths. Typical examples for this are the cellular phone business, where the GSM-standard has been developed over GPRS towards UMTS, or the development from ISDN via ADSL towards VDSL in wireline communication. A typical example for a high speed ADC targeted as a key component in a VDSL system [1] is shown in [2]. Another example for an ADSL system can be found in [3]. In order to get the desired performance out of the converters we need high-quality clock sources (e.g., [4]).

In the area of automotive chips the challenges are usually different: Instead of getting high complexity in standard CMOS we face the problems of power handling and design robustness against ambient conditions. [5] shows an example for a mixed signal hall-sensor IC, where the internal self-calibration algorithm guarantees superior sensing accuracy. [6] is an example of a highly robust analog module. In the following a short summary about key challenges and features of selected blocks will be presented.

A 1.8 V 450 mW VDSL 4-Band Analog Front End IC in 0.18 µm CMOS

A highly integrated analog front-end (AFE) chip was designed in a 0.18 µm CMOS process using 1.8 Volts supplies only. All the receiver and transmitter functionality is included in a single chip. The receiver dynamic range requirement is achieved by the use of a 32 dB programmable gain amplifier (PGA) followed by an 11 bit ADC. The prefilter (PREFI) removes high frequency signals which would cause aliasing in the sampling operation of the ADC. For partial compensation of the line attenuation at high frequencies an analog channel equalizer (ACE) is implemented. Transmit functionality is provided by the 12 bit DAC, a reconstruction filter (POFI), and a programmable gain amplifier (POCO). On chip clock generation is performed with a digitally controlled crystal oscillator and a PLL. In sleep mode, only the clock generation and the wake up circuit are active, consuming 40 mWatts of power. The AFE is designed with fully differential circuits taking a chip area of 7.5 mm².

A Fully Embedded 10 b 160 MS/s Two-Step ADC in 0.18 µm CMOS

For broadband wireline and wireless communication systems Nyquist-analog/digital converters with a resolution of 10 bits, sampling rates in excess of 100 MS/s and signal bandwidths up to 50 MHz are needed. Especially in portable applications, low power consumption is an additional constraint. The two-step subranging approach offers both low latency and small chip area as compared to pipeline-converters of the same resolution, together with low power consumption. Since in highly integrated system-on-chip (SoC) solutions the number of available pins for the analog part is severely limited, a fully embedded solution is required including on-chip reference generation and adequate input signal buffering.

The 10 bit ADC with 160 MHz sampling rate was designed in 0.18 µm CMOS. It has a silicon area of 1 mm² and a total power consumption of 190 mW. Target applications include VDSL, Cable modem and DVB-T system solutions using COFDM modulation.

A 14-Bit Delta-Sigma Modulator for ADSL-CO Applications in 0.18 µm CMOS

A high-resolution multi-bit Sigma-Delta ADC implemented in a 0.18 µm CMOS technology is introduced. Active blocks are composed of regular threshold voltage devices only. The circuit is targeted for an ADSL Central-Office (CO) application. An area- and power-efficient realization of a 2^{nd}-order, single-loop, 3-bit modulator with high oversampling ratio (OSR=96) was developed. The $\Sigma\Delta$ - modulator features an 85 dB dynamic range over a 300 kHz signal bandwidth. The measured power consumption of the ADC core is 15 mW only.

New technologies require several cascaded transistor stages to provide sufficient DC gain and high output voltage swing such as a two stage Miller OpAmp. A two stage Miller OpAmp consumes relatively high power drain in the 2^{nd} transistor stage for providing appropriate phase margin and sufficient internal slew rate. However, SC integrators do not require high dynamic performance during the sampling phase. This allowed us to reduce the bias current to 1/3 of the integration phase value. The dynamic biasing technique of both integrators is driven by the rhythm of the clock signal and so uncorrelated to the signal. This solution offers the possibility to reduce the rms value of current consumption of about 30%.

A Sub-psec Jitter PLL for Clock Generation in 0.12 µm Digital CMOS

In today's chip architectures a clean clock source very often is a basic requirement. A very low phase noise and thus integrated jitter clock is a prerequisite for high-speed transceiver circuits, or sampling applications using high performance AD and DA converters. For such low jitter PLLs it is essential not only to use a low jitter VCO (like LC-VCO). One must optimize every block to get low phase noise over the full frequency span. The PLL loop is a classical charge pump PLL and is fully integrated. To minimize supply and substrate noise injection all clock and analog signal paths are differential. The phase frequency detector has been built with differential PPCL NAND gates. The combination of a fully differential charge pump with an active differential loop filter leads to reduced spurious tones at the PLL output and low ohmic outputs to drive the LC-VCO varactors. The associated common mode feedback loops present also some design and stability challenges. In order to meet the specifications for 2.488 GHz and 3.11 GHz output frequencies, two LC-VCOs have been implemented on chip. They are separated from each other and operated alternatively. The LC-VCOs are fully integrated and their differential tuning is obtained with NMOS and PMOS varactors. The fast prescalers are implemented in CML logic, in order to have reduced noise injection in the power supply lines.

A Mixed-Signal Hall Sensor IC with Direction Detection

Magnetic Sensors based on the Hall effect have been well established for automotive applications like sensing of rotating target wheels, e.g. for crankshaft, camshaft, gearbox or wheel speed detection. For reliable operation magnetic differential fields ranging from ±100 mT down to approx. ±1 mT (which corresponds to a hall voltage of about 100 µV) superimposed by homogenous bias fields up to several ±100 mT have to be resolved in an automotive environment. The sensor can be supplied directly by the 12V board net. Major requests are:

- Tj=-50°C up to 210°C
- Supplies between 4.5V and approx. 24V
- Immunity against supply ripple and radiated energy
- Insensitivity to bias field and amplitude modulations
- Fast signal detection at start up or supply interruption

An additional challenge is caused by the current interface: The chip modulates its own supply current to signal “high” or “low” logic states. This leads to thermal transients propagating through the chip influencing biasing conditions as well as differential pairs and the highly sensitive hall probes. Therefore we had to establish a layout floor plan which takes into account noise separation as well as thermal interaction. For getting the desired sensing accuracy we have defined a mixed-signal architecture which contains a straight forward analog signal path for analog robustness. Accuracy and start-up considerations are tackled in the digital domain. The self-calibration algorithm forms a negative feedback loop which measures the analog signal quality and adjusts system parameters like offset via D/A-converters accordingly.

A Robust Smart Power Bandgap Reference Circuit for Use in an Automotive Environment

Bandgap reference circuits represent a key block in most smart power circuits. For automotive use, their functionality and accuracy under harsh environmental conditions is crucial for the IC’s performance.

One issue is the extremely high operating temperature which can, under failure conditions, reach 220 °C or more. Since the bandgap function is needed for a controlled shut-down, safe and reliable operation has to be guaranteed also at these temperatures. In addition, especially automotive power handling circuits suffer from minority carrier injection into the substrate due to over- or undershoots. They represent collector currents into any junction embedded into the substrate and can cause disturbances in sensitive analog circuits, e.g., the bandgap reference.

To overcome the problems of minority-carrier (i.e., electron) injection into the substrate and the issue of high-temperature junction-leakage currents, we have developed a new topology for the bandgap reference circuit. In this topology, all n-wells which are potential collectors of the parasitic n-p-n transistor are supplied by a low-impedance path to ensure that parasitic currents at these nodes will not affect the circuit’s performance. Since the largest junction-leakage currents at high temperatures also occur at these nodes, the new topology also shows excellent performance at very high junction temperatures.

Measurements show that parasitic currents do not disturb the functionality of the new bandgap reference which operates accurately up to 260°C.

Future Trends

Whereas the previous examples demonstrate the state of the art we will now try to extrapolate today's findings into the future. A well-suited instrument for this is the ITRS (International Technology Roadmap for Semiconductors) [7]. What we have seen in the past is the shrinking of feature sizes in general. This leads to higher speed, and lower power dissipation and cost per function. Process technology developments were mainly driven by the requirements of digital chips, and the analog circuits had to adapt to that. But to be honest – with the addition of linear resistors and capacitors most of the so defined processes were quite suitable to analog circuit design as well. Will this prolong in future?

The first thing we can note from the ITRS is that the development of digital process technologies will not be as smooth as in the past. We see that even for logic we can find three different roadmaps. One for "High performance logic", one for "Low operating power", and one for "Low standby power". As time passes, these three branches are predicted to diverge even further. In the year 2001 the roadmap sees at least the same supply voltage for all of them, which is 1.2 V. In the year 2007 the nominal supply voltages show a spread between 0.7 V and 1.1 V. At first sight it seems astonishing that the lower power we want to achieve the higher the supply voltage is. This is in some contradiction to the well-known practice that supply reduction helps in saving power. In order to understand this we have to go to a different viewpoint. If we look into the "High performance logic"-table again we see that the subthreshold leakage current goes from 10 nA/µm width in 2001 to 1 µA/µm in 2007. Having a full chip of such leaky devices leads to an unacceptable high leakage level in many applications. Assuming e.g. 10 mio. gates with 1 µA leakage each we end up at 10 A leakage current. And this is for room temperature with a significant increase towards higher temperatures. So we learn that many applications in future are just power-limited. With a given subthreshold slope of approx. 85 mV/decade the only way to reduce this leakage current is to increase the threshold voltage. This, however, leads to slower transistors. In order to speed them up we have to use a larger gate overdrive which leads to a larger supply voltage. This again leads to higher switching power dissipation. So this scenario makes only sense when most of the power is coming from static leakage power and it is of primary importance to reduce this. At the bottom line we find out that if we want do optimize for low power consumption we have to balance static against dynamic power dissipation and the optimization result depends on factors like the activity of the circuit and the acceptable delay time. Depending on this we find optimums requiring different transistor parameters causing different process flows.

Another trend we see is that useful analog supply voltages divert more and more from digital supply voltages. The "Mixed-signal device technology roadmap" shows a typical analog supply voltage of 1.8 – 2.5 V in the year 2007. Since the digital supply voltage tends to go down whereas the analog supply voltage stays more or less constant the gap between analog and digital gets even bigger. In addition to that even for plain digital circuits we see that the cost per wafer further goes up due to increasing process complexity and increasing equipment cost. As long as analog functions can live with the options provided by the digital process this will be ok for analog. So, if analog circuit parts can be designed with the digital core devices, eventually using digital I/O devices for getting higher supply voltages, this does not add extra cost. However, if analog circuits are requiring transistors for their own, it is quite likely that this will be just a cost overhead as compared to multi-chip solutions. It should be noted that the big success of SoCs was not due to the elegance of this approach, it was mainly because it also was a cost optimum. So the future of SoCs will greatly depend on the ability of system architects and analog designers if they continuously will manage to deal with processes mainly defined for digital use.

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[3] R. Gaggl et al: “A 14-Bit Delta-Sigma Modulator for ADSL-CO Applications in 0.18µm CMOS”; ESSCIRC 2002

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[7] ITRS: http://public.itrs.net

Nano-Technology

Micro@Nano-Fabrication-Austria

E.J. Fantner

IMS Nanofabrication, Vienna, Austria

Micro@Nano-Fabrication-Austria (MNFA) is a cluster-project within the Austrian Nano-initiative. It is carried by 19 partners from university, Fachhochschule, non-university centers, Kplus-competence centers and industry. The cluster consists of 33 specific projects which cover 5 topical issues. These are

- Micro@Nano Structuring
- Bio-inspired Materials
- Functionalised Nanomaterials
- Nanodevices
- Sensors & Actuator Systems

The common denominator of all these projects is the use of large-field ion projection optics for 2- and 3-dimensional direct structuring of matter in the micro & nano scale.

The main topic of my talk will be the description of the innovative business creation approach based on the rather unique co-operation between basic research, applied research and commercial product development in the early phase of the Technology Adoption Life Cycle. The resulting competitive advantages in terms of time-to-market, risk-to-market and road-to-market will be discussed. Describing the business life cycle in the environment of a discontinuous innovation by 4 phases, it will be shown how the complementary strengths of basic (university) research and commercial product development can be exploited in the best way. Criteria and specific examples within the MNFA-project will be presented.

An attempt to benchmark this Austrian cluster approach against other concepts within relevant segments of the global micro & nano market will made.

Applications of Micro- and Nanotechnologies

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Carbon nanofibers and nanotubes are promising to revolutionize several fields in material science and are suggested to open the way into nanotechnology. Further market development will depend on material availability at reasonable prices. We have achieved bulk production capacities of high purity carbon nanofibers (CNFs) at low cost by a catalytic chemical vapor deposition (CCVD) process. Reasonably low temperatures and yields of up to several g/m^{2}min at more than 70% carbon gas-to-fiber conversion rates allow considerable cost reductions. Polymer composites have been prepared by shear mixing of CNFs into polymer matrices and extrusion. Another application of our Carbon nanofiber process technology has demonstrated their satisfying field emission properties for large display flat panel devices. We are also studying new carbon fiber composites for hydrogen storage and electronic thermal management applications. Combined with our existing microcooler technology we will reach new horizons in thermal management of high power devices. Microchannel microcoolers have been enabling a breakthrough of semiconductor lasers for industrial applications.

Nanomechanical Systems

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Cornell University, Ithaca, NY USA

We have created mechanical devices using a variety of materials that we have been studying as sensors and other applications. In most cases, the motion of these devices was detected and in some cases actuated by the application of light. Spatially varying mechanical driving of micromechanical structures was also demonstrated using a scanning probe tip for actuation and an electron beam to detect motion. Sensor applications include immunospecific detection of single bacterial cells and chemical monolayers. Parametric amplification of mechanical motion was demonstrated in a variety of device configurations with optical and electrodynamic drive. High-resolution lithographic processes have been used to create similar resonant mechanical systems with dimensions down to tens of nanometers. Related nanofabrication approaches have also been used to create nanostructures for the mechanical manipulation and sorting of molecules by mechanical and physical properties in a variety of fluid containing system configurations. Mechanical confinement of fluid systems has also been used to enable optical detection and analysis of individual biomolecules.

Organic Electronics

Integrated Organic Electronics

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The class of organic materials, conjugated polymers, and organic molecules has reached a quite mature and highly accepted status after more than 20 years of intense research and development. The quality and the purity of these new semiconducting materials have been improved by new approaches of chemical synthesis and chemical purification processes and are now demonstrating purity levels which are comparable with state of the art values of inorganic semiconductors. The question of the intrinsic electronic properties of these organic semiconductors is still not answered but the high quality of the available materials made it possible to fabricate electronic devices like field-effect transistors (FET) and optoelectronic devices like organic light-emitting diodes and solar cells. We will report on our research activities targeting the manufacturing of organic field-effect transistors (OFET) with thin films of acenes and other organic semiconductor candidates including results on the growth and characterization of single crystals of acenes. We will outline the current status and the perspectives of these organic electronic devices concerning their performance and integrability into electronic circuits of other platforms, which provides a wide spectrum of applications for new integrated functions.

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Sensors

A Modular MEMS Accelerometer Concept

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A quasi-monolithic MEMS concept setting up a new family of MEMS-based sensors is presented. The concept combines the advantages of hybrid MEMS with respect to optimal technology choice, and of monolithic integrated MEMS with respect to system integrity, on chip signal conditioning, self-calibration and size.
A sensor signal conditioning circuit and a micro-mechanical sensing element are joined face-to-face by eutectic bonding on wafer level. This sealed system can be used as is, or can be assembled in standard SOIC plastic package. Using this approach, austriamicrosystems AG has developed high performance, low-cost accelerometer sensors.
The accelerometer micro-system consists of the mechanical component die with a single clamped poly-silicon cantilever and an ASIC die with counter-electrodes to measure the distance between cantilever and IC surface. The operation in closed loop mode yields high linearity and large bandwidth. Specific advantages of the concept are: (1) the modular approach is open for advanced sub-micron technologies, (2) the hermetic seal approach paves the way to new vacuum-on-chip MEMS products.

Introduction

Accelerometers gained a significant market share within the multi-billion microsystem market (2002: 90-100 Mio units expected representing a turnover in the range of 400-500 Mio US$ [1]).

Presently, main applications can be found in the automotive market segment (e.g. front and side airbag sensors, ESP respectively chassis stabilization, active suspension, roll over detection). However, low-g sensors enter also new application areas like inclinometry and vibration sensing for instance for anti-theft devices or activity monitoring for pacemaker control. Like in the microelectronics RAM market the 50 g airbag sensor market has been ruined by a prestigious price war. Presently the low-g sensor market, which partially covers also the Inertial Measurement Module (IMM) market, is gaining weight and speed.

Automotive components are high volume products (some million units per year). Beside stringent performance, environmental and reliability requirements, cost became the decisive factor for success in this market. The manufacturing costs consist of

- fabrication cost for the core microsystem including signal conditioning,
- packaging cost, and
- test cost including quality assurance tests.

[1] austriamicrosystems AG, with headquarter in Unterpremstaetten near Graz (Austria), is one of the world's leading designers and manufacturers of custom specific mixed signal ICs. The company has 940 employees and offices in 14 countries worldwide. Despite the semiconductor downturn austriamicrosystems' sales grew in 2001 by 20% to approximately EUR 147 million.

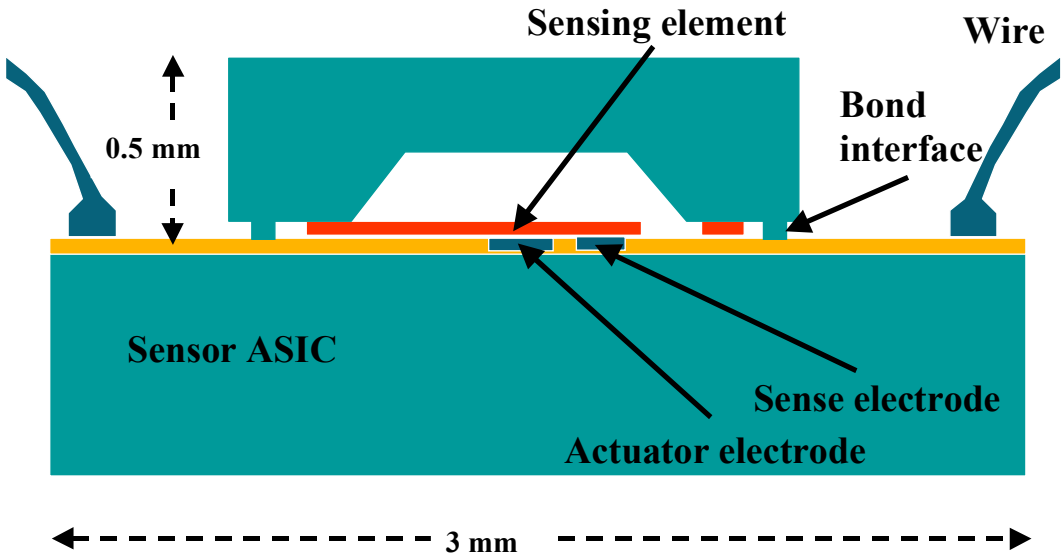

Fig. 1: Schematic view of the accelerometer.

Packaging and test are very often the cost determining factors. Generally, highly efficient designs for manufacturability, packaging and testing are required. Desirably, they should include harmonically integrated first level packaging methods and extensive self-test as well as cheap calibration. The latter should be based on single temperature measurement. However, a highly efficient design is not sufficient. Very often, effort and time needed for the industrialization of a properly chosen design constitutes the main barrier for coming up with the right product at the right time (i.e. time to market). One of the deeper reasons for the difficulties of industrialization of new MEMS is the very sensitive interdependency of performance and technology parameters. This becomes especially important in situations where the technology is not yet mature and stable enough to guarantee the finally required small process tolerances.

Design Approaches and Products on the Market

The first monolithically integrated, commercially available accelerometer sensor was industrialized by Analog Devices [3]. It is based on the capacitive detection of the in-chip-plane movement of a comb structure. The monolithic concept requires a trade-off in IC technology (feature size) and mechanical performance. Therefore, the complexity of signal conditioning on-chip is limited. This affects self-test and diagnostic functions, fine adjustments and calibration. This forces to keep complexity of signal processing at a lower level. The non-modular concept asks for long development times for new design options and, moreover, is yield critical. A ceramic or metal can package is needed.

Industrialized concepts of hybrid accelerometers are available, comprising comb like sensor elements as well as out-of-plan movable beam/cantilever like structures made from dedicated MEMS processes (e.g. Bosch, Motorola [6], VTI [7], [10], Sensonor [8]). They are based on piezoresistive or capacitive measurement principles. Signal processing is placed on a separate IC. Sensor elements and signal processing ICs are packaged in one body, forming the hybrid system. Hybrid systems allow optimized sensor structures as well as the signal processing part to be realized by dedicated and well established manufacturing processes. Larger size and still a considerable packaging effort are the weak points of the hybrid concept. Bosch´s hybrid accelerometers are

based on Surface Micromachining using EPI-poly Silicon with DRIE and cap for first level packaging. The concept requires larger sensing elements due to the less sensitive external signal conditioning. This concept is well suited for high performance accelerometers and also supports special applications (e.g. angular acceleration sensor), however the cost structure is an issue and the concept is not suitable for high vacuum applications due to out-gassing of glass seal ring. Similar concepts are used by a number of other MEMS companies (e.g. ST).

Motorola released a hybrid sensor for the ±8 g range. A low-g accelerometer development is ongoing as well, but information on the actual status was not available to the authors.

VTI is currently market leader for automotive low-g acceleration sensors. The hybrid sensor has probably costs advantages over Bosch like surface micro machined hybrid concepts at similar sensor performance but seems to be still a rather high cost technology. The sensor requires dedicated package that is significantly thicker compared to standard.

Some new principles are becoming interesting for commercial applications. Memsic has developed a sensor based on a thermodynamic principle with a hot gas bubble. The sensor is limited to applications with close to horizontal mounting for lateral acceleration measurement, z-axis measurement is not possible. No data on the impact of vibrations in the z-axis direction were reported which may be a critical issue for some applications.

The number of accelerometer developments (and corresponding publications) following the described concepts is huge. Only few of them have successfully entered the market.

Sensor Design

The quasi-monolithic concept of austriamicrosystems represents a unification of the monolithic and the hybrid approach. The movable out-of-plane sensing element is formed by simple bulk micromachining on a second, so called top wafer and can be designed easily for different acceleration ranges. The basic wafer carries the dies with measurement and actuation electrodes as well as with the whole signal processing part. This wafer is processed in standard CMOS technology. Joining the two parts on die (soldering) or wafer level (eutectic bonding), a quasi-monolithic system is created which combines the advantages of the monolithic and hybrid approaches.

To a large extent the concept was the solution and consequence of the following, quite conflicting development goals:

- High performance accelerometers for low, medium and high g applications
- Cost efficient solution for high volume production
- Usage of available CMOS technologies with
- low cost add-ons
- Modularity of sensor design and signal conditioning part
- Usage of standard packaging technologies

The accelerometer concept is demonstrated in Fig. 1. The top die is forming the mechanical sensing component and the bottom die carries the actuating and sensing electrodes and the ASIC. The joined dies are packaged as a single unit. As mentioned, the mechanical sensor module is customizable for different g ranges. The corresponding control and signal-conditioning module can be adapted to the different ranges from a

low-g sensor (1 or 2 g for electronic chassis stabilization) to high-g applications (up to 200 g and more for airbag release).

The sensing element is a single clamped poly-silicon cantilever, which forms the mass loaded spring of the accelerometer (see Fig. 2). It is fabricated by photolithography and reactive ion etching followed by a subsequent release step using anisotropic wet etching in KOH solution. This yields a very robust, cost efficient sensing element with most simple shape and practically no cross-axis sensitivity.

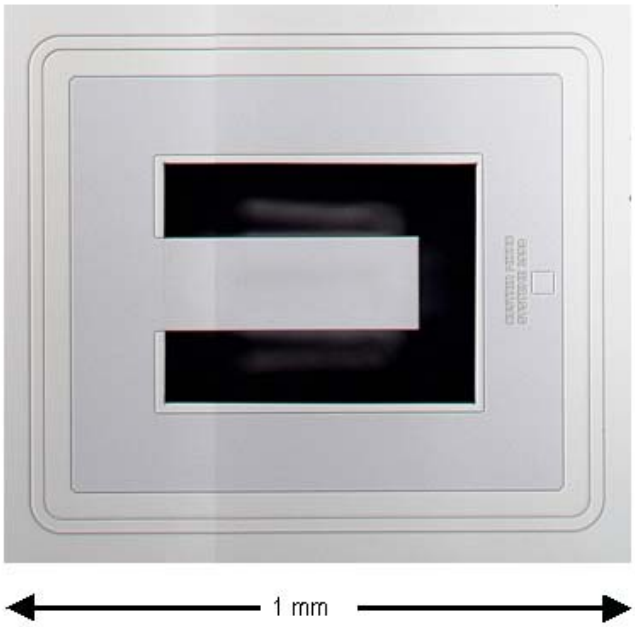

Fig. 2: Mechanical component with poly-silicon cantilever (Top view).

The sensing element die is joined face to face to a CMOS ASIC using a eutectic bonding procedure on wafer level. Thus, the cantilever is hermetically sealed and electrically shielded. In this way, a first level package for the movable cantilever is simultaneously provided, allowing for standard plastic injection molding of the composite structure. An air gap of a few micrometers between cantilever and the ASIC is formed.

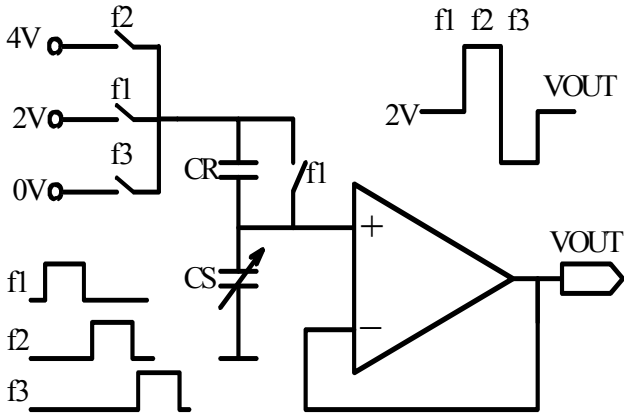

Fig. 3: Sensor Front End: the reference capacitor CR is connected in series with the variable sensing capacitor CS.

The ASIC contains the counter electrodes for the actuation and capacitive position sensing of the cantilever, and the electronics for signal processing and trimming (0.8 µm double poly, double metal CMOS). The patented integrated capacitive distance sensing circuit is capable to measure changes down to <0.5 atto-farad/√Hz. To achieve such high resolution, parasitic cancellation techniques have been extensively used. This involves low capacitance switches, dedicated architecture for low input capacitance buffers, and shielding techniques. The schematic in Fig. 3 shows the basic principle of the measurement front end.

The measurement cycle is a good example for the inherent feedback of any capacitive measurement system. The applied measurement voltages should be large enough in order to increase the signal to noise ratio (in our example short pulses of 2 V, 4 V and 0 V within one system cycle). They create electrostatic force pulses inversely proportional to the square of the actual distance between the cantilever and the counter-electrode. These forces cannot be neglected. Assuming a pulse time much shorter than the response time of the cantilever, an average DC force is created by the measurement pulses which will bend the cantilever and becomes part of the offset signal setting. This can be demonstrated by the simulation results of the transient behavior of the cantilever movement shown in Fig. 4. For demonstration purpose a highly unrealistic thin cantilever was chosen where the nonlinear electrostatic feedback of the measurement forces can drive the cantilever into the instability region.

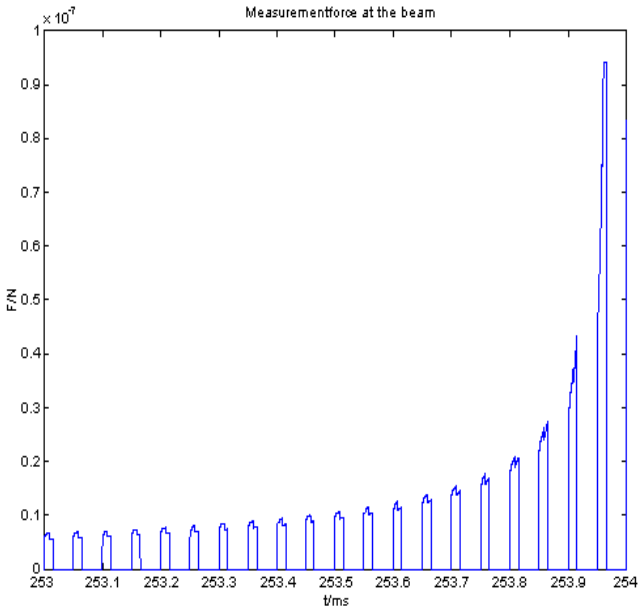

Fig. 4: Transient behavior of a very thin cantilever with too large measurement force

The developed simulation system can be used for the analysis of the overall system behavior and of specific effects in different applications. Additional FEM analyses were used for the determination of key parameters of the SIMULINK model.

For excellent linearity and large bandwidth up to some kHz (depending on the configuration of the cantilever for the different full-scale ranges), the system is operated in closed loop mode. The actuating force is a PWM modulated signal in order to generate a force that linearly depends on the capacitance change. This electrostatic actuation keeps the mechanical cantilever close to its initially adjusted position.

Loop stability is ensured by the uncritical modal behavior of the cantilever and overcritical squeezed-film damping in the air gap. The bandwidth of the output signal is limited by outside loop filtering (typically 100 Hz for low g and 1 kHz for high g application).

The microsystem is packaged in a standard low-cost plastic injection-molded package (SOIC 16). A decapsulated device is shown in Fig. 5. For stress reduction, a silicon gel globe top spreading over the mechanical component is employed. 2D and 3D packages with orthogonal positioning of two or three sensors are in preparation.

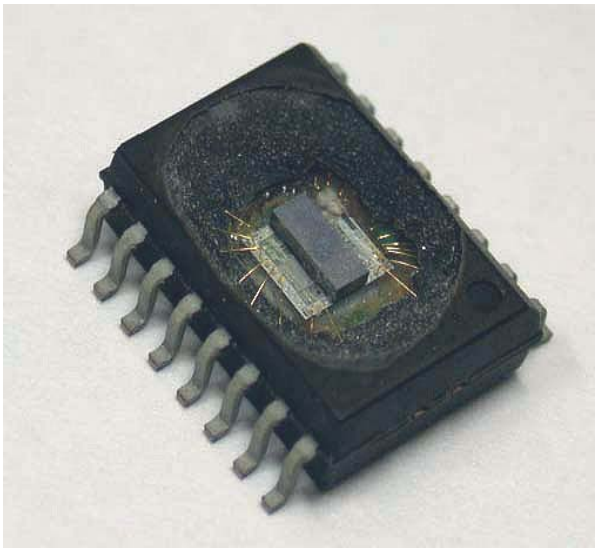

Fig. 5: Top view of a decapsulated sensor within SOIC 16 plastic package.

Main Performance Parameters

The typical sensor performance can be demonstrated for instance for a ±7 g z-axis sensor in PLCC28 package with a sensitivity of 250 mV/g is:

- Peak to peak noise at 140 Hz bandwidth <0.01 g
- Temperature coefficient of zero-g level <2 mg/K
- Zero-g stability over lifetime <0.15 g.
- Linearity better 1%

The sensors are fully calibrated for sensitivity, offset and self test. The ASIC provides a fully calibrated analog output signal, ratio metric to supply voltage with self-test function. Calibration is performed through a serial interface with one-time programmable Zener fuses.

Conclusion

The described technology is well capable to achieve the performance / cost expectations for automotive applications.

Exclusively mature technology modules are used like:

- Fully qualified standard CMOS process.
- Low temperature, one mask post processing for the bond interface.

- High yield, high performance micro-mechanical process utilizing only a few mask layers.
- Wafer bonding process similar as used in volume MEMS production
- Packaging with mechanical stress isolation.

The sensor design does not imply yield limiting factors known from other sensor concepts like fragile mechanical structures, dedicated cleaning technologies to avoid sticking of released sensing elements or more expensive process steps like deep trench etch technologies. Zero-level packaging is an intrinsic feature of the sensor device concept, and is not an additional cost factor as in present commercial sensor designs.

The on-chip sensing with atto-farad resolution enables orders of magnitude better resolution than competitors at equivalent sized sensing elements.

The accelerometer offers low noise, low drift, low cross-axis sensitivity, high linearity, combined with excellent robustness versus mechanical shock.

Basically with the same technology other MEMS devices like high performance capacitive pressure sensors can be built.

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Sensors and Interface Electronics for Oil Condition Monitoring

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In this contribution, we discuss the suitability of physical sensors for oil condition monitoring. For the oil's viscosity, microacoustic sensors can be utilized. Standard readout concepts for microacoustic sensors are currently based on either bulky and expensive measurement equipment or electronic oscillator circuits. These oscillators malfunction in case of higher viscosities due to the associated higher device damping. Thus, we present an alternative measurement approach, which can be implemented in a compact fashion with cost-effective standard components.

Introduction

The monitoring of oil and oil-based liquids (including emulsions) is an important task in a number of application areas ranging from the food industry to automotive applications. In the latter field, there has recently been increased interest in monitoring the condition of lubricants facilitating proper engine operation. Monitoring the engine oil condition at first instance allows the implementation of increased oil drain intervals. Moreover, it provides increased insight into the actual state of the engine, which enables the detection of possibly approaching engine failures but also the monitoring of the performance of engine oils of varying quality. Similar considerations hold for other applications where oils are used as lubricants.

An Example – Sensors for Automotive Engine Oil

Flexible oil drain intervals for engine oil are currently commonly determined by continuously monitoring characteristic engine and driving parameters (such as, e.g., driven distance, speed, and oil temperature) [1]. The proper oil drain interval is then indirectly estimated by means of corresponding algorithms processing these parameters. However, ideally the evaluation of the oil condition should solely be based on parameters measured *directly* in the oil itself. Considering the procedures that are utilized in "off-board" oil condition evaluation by experienced, specialized laboratories, one finds that an oil condition evaluation based on physical parameters would require a large array of sensors, which often cannot be integrated in an on-board sensor system or do not offer the desired long-term stability. Alternatively, a multifunctional sensor for the oil's viscosity, permittivity, temperature, and oil level can be used [2]. These parameters are to be processed by algorithms, which combine the ease of the indirect approach and the advantages of directly considering physical oil parameters. The measured viscosity and permittivity are the primary quantities supporting the oil condition evaluation. The temperature measurement is necessary, as the measured parameters are temperature-dependent. This approach represents the implementation of a so-called *physical chemosensor* [3] where *chemical* liquid properties ("oil quality" in this case) are sensed solely by means of *physical* sensors. In contrast to *chemical sensors*, these sensors do not use chemical interfaces, which feature a number of disadvantages like ageing, drift and lacking reproducibility.

The determination of two indicator quantities for the oil quality allows the discrimination of different oil strain scenarios. As an example, Fig. 1 shows measured values for a “normally” strained oil, which has been sampled from an engine after 19,000 km of test driving, and the same oil type which has been used during cold start tests (15 starts @ -15°C) which leads to fuel dilution of the oil [4]. These oils and the corresponding new oil each correspond to a point in the permittivity–viscosity plot in Fig. 1. It can be seen that, as expected, the oil with fuel dilution shows a decrease in viscosity (fuel features a lower viscosity than engine oil) whereas the “normally” aged oil leads to an increase in viscosity (mainly due to the oxidation of the oil). However, the permittivity signal only shows a major change for the “normally” aged oil, because fuel shows a similar permittivity as engine oil. This example illustrates the increased insight gained by monitoring two parameters compared to monitoring a single quantity.

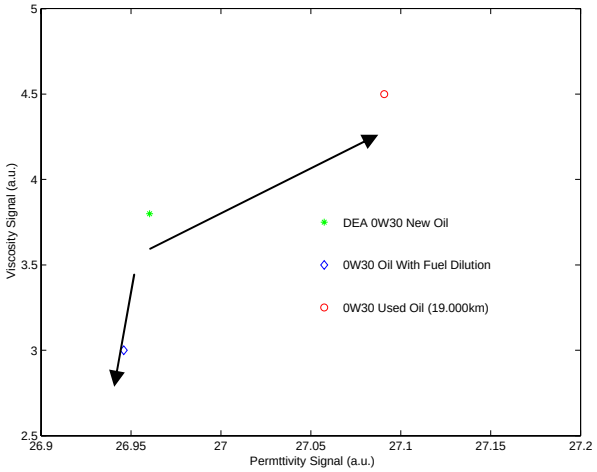

Fig. 1: Simultaneous measurement of viscosity η and permittivity ε @ 25°C [4].

Microacoustic Viscosity Sensors

While the implementation of permittivity sensors is straightforward (this can be, e.g., done by using a coaxial capacitor immersed in the oil to be measured [5], [6]), the viscosity measurement is more sophisticated. In order to avoid macroscopically moving parts as they would be used in conventional viscometers, so-called microacoustic viscosity sensors can be used. These devices excite special shear-polarized mechanical (or acoustic) oscillations in a piezoelectric crystal. Due to the coupling with an adjacent viscous liquid, the electrical device characteristics change according to the viscosity of the liquid. Examples for shear polarized microacoustic wave-types are BAW shear resonators (also called transverse shear mode or TSM resonators), leaky SAWs showing a dominant shear polarization, shear polarized acoustic plate modes, and Love waves (see [7] for an overview). Figure 2 shows the principle of a Love wave delay line which can be used as sensor. The device consists of a piezoelectric substrate supporting shear-polarized modes, interdigital transducers for the excitation and detection of the wave, and an isotropic guiding layer [7].

Liquid loading of a device performing a shear oscillation leads to an entrainment of a thin liquid film with exponential decay of the entrained shear movement (see Fig. 2, [7]), where the decay length δ is given by $\delta = \sqrt{2\eta / \rho\omega}$. Here η and ρ denote the dynamic viscosity and the mass density of the liquid, and ω stands for the angular frequency of the oscillation. The entrainment leads to (i) a mass-loading of the device

causing a change in resonance frequency (in case of a resonator) or a change in phase velocity (in case of a delay line as described above), and (ii) a damping of the oscillation or the wave. Both effects are to first order proportional to $\sqrt{\omega\eta\rho}$ and thus a sensor for the viscosity-density product can be realized. For non-smooth surfaces, parts of the liquid can be "trapped" leading to an additional pure mass-loading effect, which corresponds to the density of the liquid. Thus using two sensors, one with a smooth and one with a corrugated surface, makes it possible to distinguish between the effects of viscosity and density [7]. However, in many applications, changes in viscosity outweigh changes in density such that sensors with smooth surfaces represent efficient monitoring devices for the viscosity.

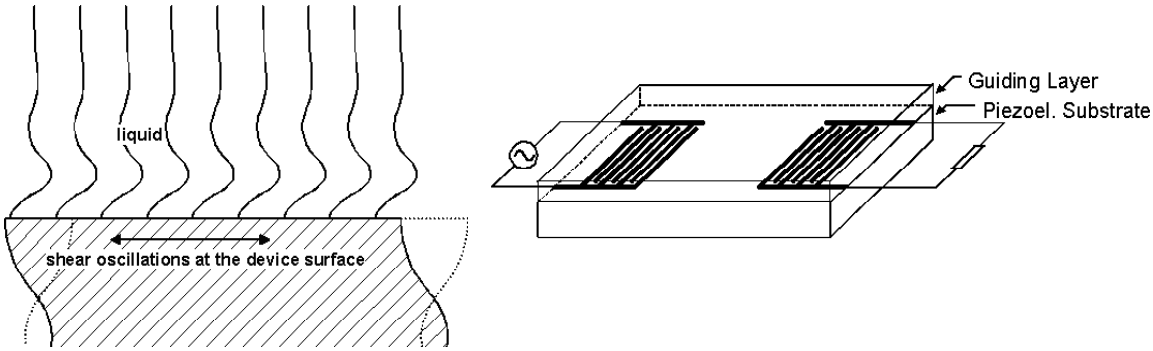

Fig. 2: Entrainment of a liquid with a shear oscillation (left) and principle of a Love wave delay line (right).

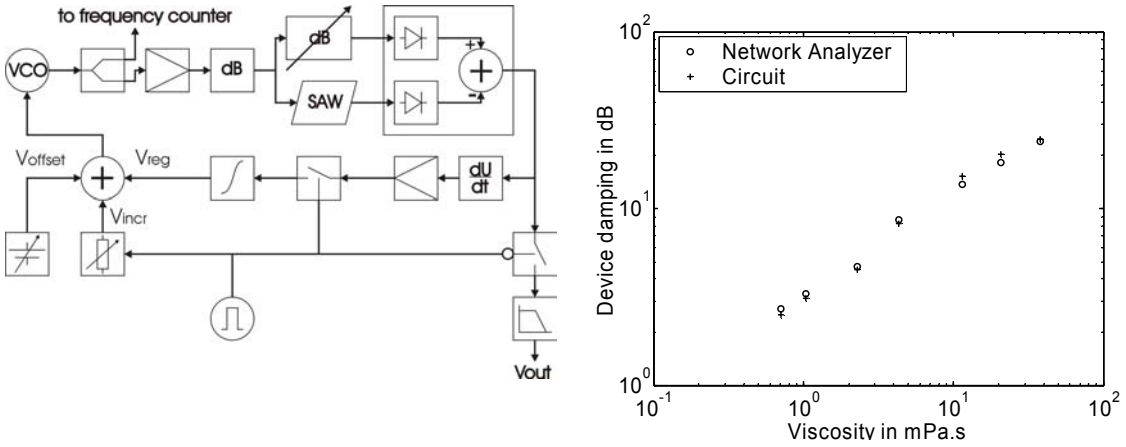

Fig. 3: Block diagram of the circuit (left) and measurement results (right).

Interface Electronics for Love Wave Viscosity Sensors

Standard readout concepts for microacoustic sensors are currently based on either bulky or expensive measurement equipment or electronic oscillator circuits using the sensor (resonator or delay line) as frequency determining element. These oscillators malfunction in case of higher viscosities due to the associated higher device damping. Hence we developed a dedicated circuit which automatically measures the damping of the delay line at its resonance frequency. This is achieved by implementing a control loop, which detects the slope of the damping-frequency characteristics by means of

feeding the delay line with a frequency modulated VCO signal at its input and detecting the amplitude at the output. At the center frequency f_0 this slope and thus also the amplitude changes due to the frequency modulation vanish, which is utilized to tune the center frequency of the VCO to f_0 by means of a control loop. Figure 3 shows the block diagram of the circuit and measurement results showing the correlation of the device damping (obtained from the circuit and a network analyzer measurement as reference), with the viscosity as obtained by using a rotational viscometer. More details can be found in [8].

Summary

For many applications, the monitoring of oil-based liquids is of crucial importance. In this contribution, we reviewed recent developments in the field of physical chemosensors for this purpose. Particularly we discussed a novel approach for the readout of Love-wave viscosity sensors, which avoids the problems occurring with commonly used oscillator circuits.

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Thermal Imaging

Local Thermal and Current Imaging in Power Devices

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This paper summarizes recent results obtained at TU Vienna in the field of thermal and free-carrier mapping of semiconductor devices using backside transient interferometric mapping (TIM) technique. The technique is based on measuring optical phase changes due to temperature and free carrier induced variations in semiconductor refractive index. Scanning transient heterodyne and 2D holographic interferometers are used for phase measurements. Thermal distribution, hot spot dynamics, current filament movement, and failure mechanisms are investigated in electrostatic discharge (ESD) protection devices and power vertical DMOS transistors.

Introduction

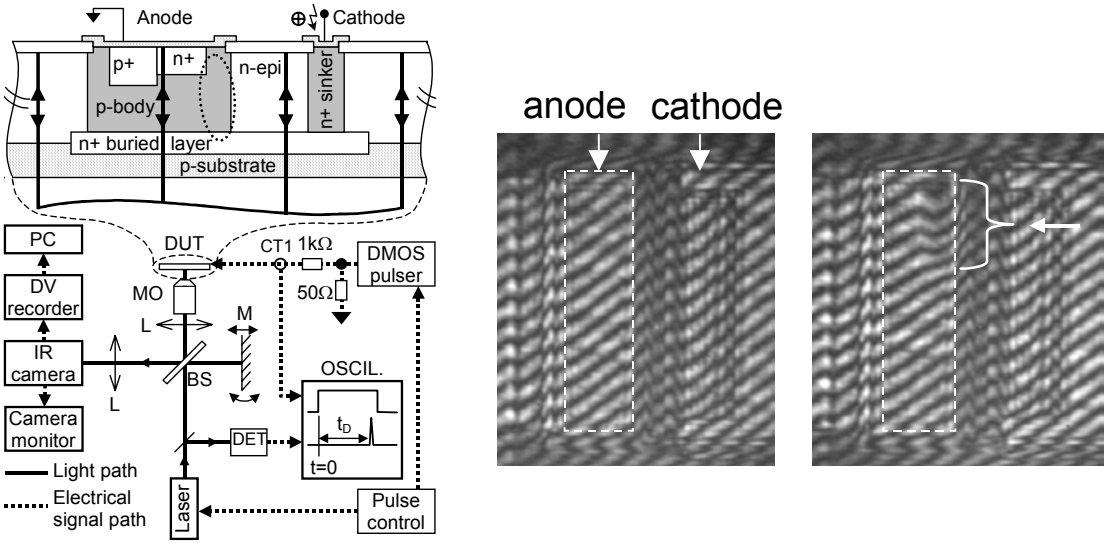
Experimental access to internal parameters of semiconductor devices as carrier concentration, current densities, power dissipation, temperature, etc. is of great interest for the understanding of device physics and for device optimization. Monitoring of temperature is especially important for power [1] and electrostatic discharge (ESD [2]) protection devices (PDs), where the self-heating effect is a main cause of device failure [3]. These devices operate at high current and power densities where the internal device behavior predicted by device simulation has a limited degree of confidence [4]. This is due to a lack of calibrated physical models at high temperatures. Thermal runaway phenomena in power devices occur in microsecond to millisecond time scale [1]. During an ESD event, large currents (1 – 10 A) and power densities (approx. 100 W) are dissipated in the device during 1 – 100 ns [2].

The backside transient interferometric mapping (TIM) technique has shown its potential in quantitative nanosecond thermal, free carrier and current flow mapping in silicon [5] – [8] and III-V [9] electronic devices and far-infrared quantum cascade lasers [10]. In this paper, recent development in the optical testing and analysis methodology is briefly reviewed. The application of TIM method to study hot spots and current filament dynamics in ESD and power DMOS devices is presented.

Experiments and Methodology

In the TIM method, an infrared non-absorbed laser beam (wavelength λ = 1.3 μm) probes temperature- or free carrier-induced changes in the semiconductor refractive index inside a device [5], [7]. The beam passes through the substrate, is reflected on the device topside and returns. The resulting phase shift is detected interferometrically. In a scanning heterodyne interferometer, a focused laser beam scans the device active area and the device is repetitively electrically stressed for each scan position [5]. Transient phase shift is obtained with 3 ns time resolution. A Michelson-like interferometer is used for phase measurements with 0.4 ns time resolution [11]. In a 2D holographic interferometric version of the TIM method, a broad beam illuminates the whole device area [6]. Figure 1 (a) shows a simplified arrangement of the setup. The phase profile is obtained by analyzing a 2D interference fringe pattern, see Fig. 1 (b), (c). The thermal image in the whole sample can be obtained using a single laser pulse, so non-

repeatable phenomena can be studied. The pulse width of 5 ns determines the time resolution. By varying the delay between the laser and stress pulse, the time evolution of thermal distribution can be obtained.



(a) (b) (c)

Fig. 1: Schematics of the 2D TIM method (a). Typical fringe interference pattern in an unstressed (b) and stressed (c) device. The deformation of fringes in (c) marked by an arrow results from local heating causing the phase rise; after [6].

It has been shown that if thermal effects dominate over the free carrier contribution, the measured phase shift $\Delta\varphi(x,y,t)$ can be directly related to a 2D thermal energy density E_{2D} in semiconductor according to the relation [7]:

$$\Delta\varphi(x,y,t) = \frac{4\pi}{\lambda\, c_V}\frac{dn}{dT}E_{2D}(x,y,t) \tag{1}$$

where c_V is the volume specific heat and dn/dT the thermo-optical coefficient. E_{2D} is a "memory" quantity representing the time integration of all the preceding power dissipation. The instantaneous 2D power dissipation density $P_{2D}(x,y,t)$, representing the well the current density if a constant voltage on the device is assumed, can be calculated according to [8]:

$$P_{2D}(x,y,t) = \frac{\lambda}{\dfrac{dn}{dT}}\frac{c_V}{4\pi}\frac{\partial\Delta\varphi(x,y,t)}{\partial t} - \frac{\lambda}{\dfrac{dn}{dT}}\frac{\kappa}{4\pi}\left(\frac{\partial^2\Delta\varphi(x,y,t)}{\partial x^2} + \frac{\partial^2\Delta\varphi(x,y,t)}{\partial y^2}\right) \tag{2}$$

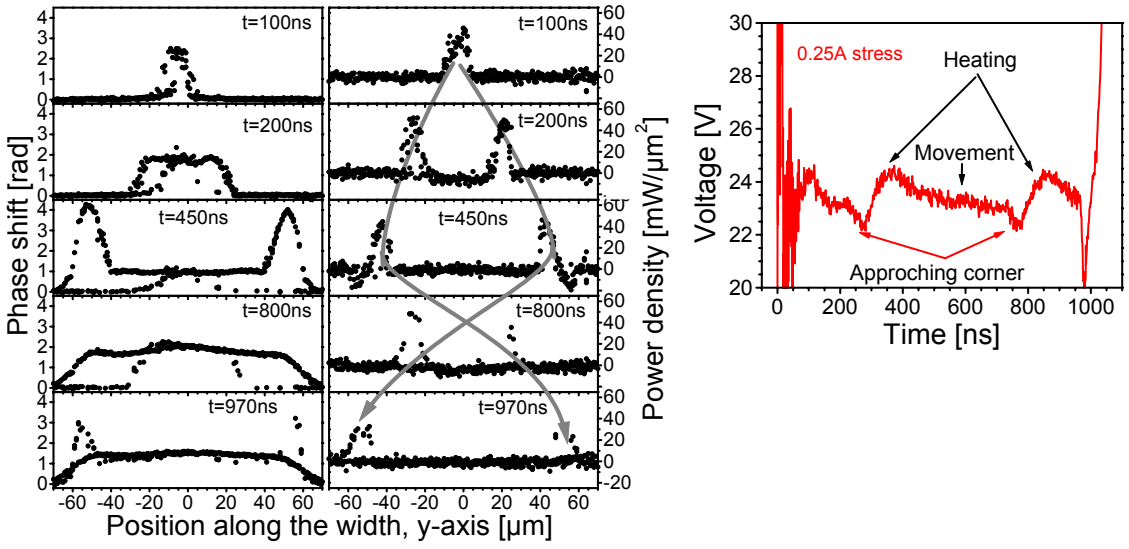
where κ is the thermal conductivity.

Smart power ESD and vertical power DMOS devices have been investigated. The devices have a common n^+ buried layer serving as collector of a parasitic npn transistor. The devices were stressed by rectangular current pulses of 100 ns – 1 µs duration. If not specified elsewhere, this drives the devices in a bipolar snapback mode.

Results

The dynamics of current flow in ESD PDs has been studied by analyzing the absolute phase shift itself (representing the temperature), the 2D power dissipating density P_{2D}, (representing the current density) and the device voltage waveform [12]. Strongly localized moving current filaments (see Fig. 2(a)) have been observed in devices exhibiting near zero or NDR part in IV characteristics. The filament characteristics, as starting place, size, speed, travelling mode and its occurrence probability depend strongly on stress magnitude I_S. The filaments exhibit pulse-to-pulse instability in their movement direction and position of origin, i.e. the device internal state differs from pulse to pulse. This is due to fluctuations in carrier densities.

At long pulses of low current magnitude the filament can several time travel over the device width without destroying the device, see Fig. 2(a). The filament passage over the device produces a specific fingerprint across the voltage on the device, see Fig. 2(b). When the filament approaches a region with higher impact ionization, e.g. at terminations, or when it passes from a hot region into a cooler region the voltage decreases due to negative temperature dependence of the impact ionization rate [13]. When the filament does not move, as it is initially in the middle and then at corners, the voltage increases due to the self-heating effect to keep the same impact generation rate under the constant current. When the filament moves, a constant voltage is typically observed, which is due to a stabilizing effect of the movement on the temperature in the filament. The filament localization and persistence is caused by fast cooling to lateral sides.



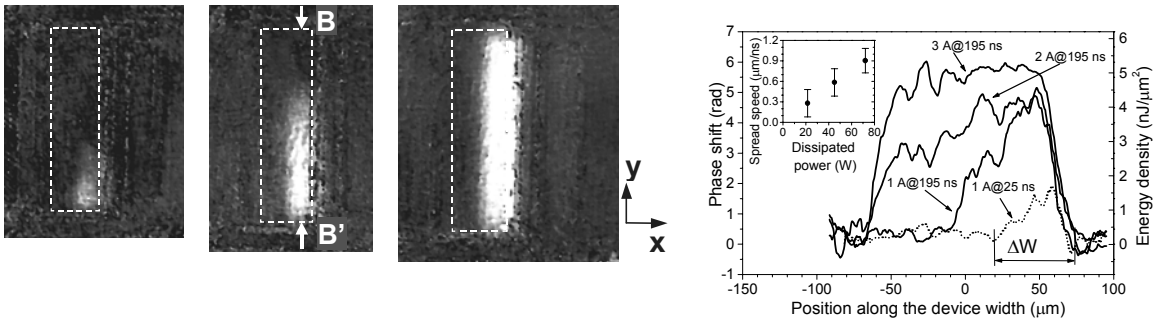
(a) (b)

Fig. 2: (a) Scatter plot of measured phase shift (left) and extracted P_{2D} at several time instants in a silicon controlled rectifier device exhibiting moving filaments at current of 0.15 A. The filament path is marked by the gray lines with arrow. The scattered nature of data is due to pulse-to-pulse instability in the filament movement. (b) Voltage waveform related to the filament movement; after [12].

At higher stress currents, the number of filamentary modes typically increases. Figure 3 shows the 2D thermal distribution at high stress levels, demonstrating the spreading of current flow with time. The high-energy input in the filament exceeds the energy output by cooling to lateral sides. This causes that the current density decreases with time,

which leads to a current homogenization or spreading with time [6]. Similar effects have previously been observed indirectly by repetitive photon emission measurements [14].

The speed of the current filaments and of the filament spreading increases with time and with the stress current I_S, see inset of Fig. 3(d). This effect, beneficial for ESD robustness, is due to a negative temperature dependence of impact ionization rate [13]. The pulse-to-pulse instabilities in the device internal behavior leads to formation of a pattern in IV curves when plotting the IV curve point by point without time or ensemble averaging [12].



(a) (b) (c) (d)

Fig. 3: Single shot 2D phase profiles in a ESD protection device demonstrating the spreading of current flow with time and I_S: (a) 1 A @ 40 ns, (b) 1 A @ 195 ns, (c) 3 A @ 195 ns. (d) Phase profiles along the B-B' line in (b). Inset: Filament spreading speed as a function of I_S; after [6].

Vertical DMOS transistors with different number of cells were investigated before [15] and in bipolar snapback operation [16], [17] using TIM method. Before snapback, the current sharing between the cells is homogeneous, due to a negative thermal feedback during the avalanche breakdown [15]. Under snapback conditions, the current flow is strongly inhomogeneous, forming localized current filaments, see Fig. 4. The cells at the drain terminations are triggered first due to higher electric field there. With time the neighboring cells trigger as well, causing that the current flow moves toward the device area or along the termination (Fig. 4). The observed feature of DMOS behavior in snapback is qualitatively reproduced by 2D and 3D device simulation [16]. The base-push-out or Kirk effect and the negative temperature dependence of the impact ionization rate were found to play a decisive role in the cell-to-cell hoping of the current flow. This is plausible for ESD robustness.

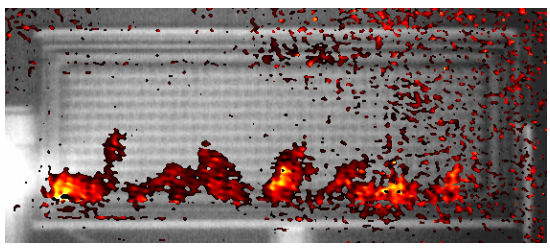
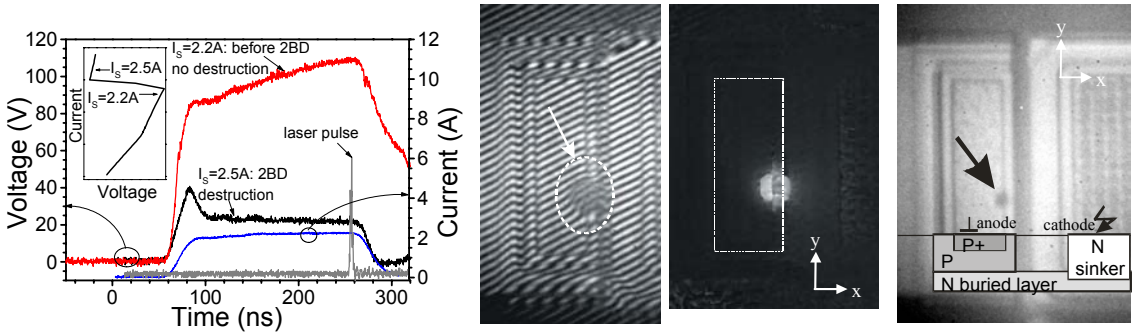


Fig. 4: Phase image in a 440 cell DMOS device recorded at time 150 ns after the beginning of a 7A current stress pulse. The phase image is aligned with the backside infrared device image; after [16], [17].

Finally, failure mechanisms have been studied during single destructive pulses [18]. Fig. 5 shows the device interferogram and extracted phase shift in a diode structure, recorded during a single destructive 2nd BD event. At the destruction, the voltage across the device drops from the pulse beginning, indicating a current density driven instability, see Fig. 5(a). This leads to a formation of a current filament (see Fig. 5(c)), whose size, taking into account the thermal diffusion length of 4.2 µm for a 200 ns long pulse, was estimated to be 3 – 4 µm. The diameter of the filament correlates with the size of permanent damage at this position (see Fig. 5(d)). A decreased intensity of the interference fringes was observed during this event (see Fig. 5(b)), which indicates the onset of band-to-band absorption (E_G reduction with temperature increase). Taking into account the data of temperature dependence of absorption coefficient for λ = 1.3 µm [19], the temperature in the filament was estimated to exceed 900 K.



(a) (b) (c) (d)

Fig. 5: Voltage waveform during the destructive event in a diode (a). Fringe pattern (a), extracted phase shift (b) and IR image with defect position (d), after [18].

Conclusion

Current filaments and hot spot dynamics has been investigated in ESD protection and DMOS devices. Using the single shot capability of TIM method, current flow instabilities and destructive mechanisms have been revealed. The movement and spreading of current filaments have been identified as a thermally driven process. The TIM method is a powerful tool providing the design engineer a unique insight into internal device behavior of semiconductor devices and to verify device simulation models.

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Opto-Electronics

Quantum Cascade Lasers

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In this work, we intend to present our latest results on the improvement of GaAs/AlGaAs QCLs. The emission wavelength of the mid infrared lasers covers now a range from 8.7 µm up to 23 µm. Room temperature operation is now achieved for several band structure designs.

Introduction

Quantum cascade lasers (QCLs) are powerful light emitters in the mid infrared and, most recently, also in the far infrared [1]. The light generation is based on intersubband transitions, usually within the conduction band. The strong light emission in the mid infrared spectral region is interesting for chemical sensing, and a potential application for far infrared emission is astronomy and tomography in medicine. Recently, continuous wave operation at room temperature of InP based QCLs has been demonstrated [2].

Theory

The design of the band structure of quantum cascade lasers is a challenging task. The population of the individual levels is determined by different scattering processes like electron-electron scattering, LO-phonon emission or absorption, and photon emission or absorption. The population of the energy levels together with the position of the doping atoms modifies the band edge energy. Almost all laser structures are designed so far by very simple one-band calculations, based on an effective mass approximation. The band structures are calculated neglecting the electron population and assuming a constant electric field across each cascade. The non-parabolicity of the energy dispersion is taken into account by an energy dependent effective mass [3]. Only for a few designs more sophisticated calculations were done afterwards, because they are too time consuming to be used as design tool [4], [5].

The advantage of AlGaAs/GaAs grown on GaAs over InGaAs/InAlAs grown on InP is that the $Al_xGa_{1-x}As$/GaAs material system is lattice matched to GaAs for all Al contents x. The Al-content of QCLs working at room temperature in pulsed operation is x=0.45. The emission wavelength of these lasers is in the range of 9 µm [6], [7] up to 12.6 µm [8]. The barrier height in respect to the GaAs wells is 390 meV, large enough to prevent carrier escape into the continuum. In the case of a longer emission wavelength, a lower Al-content is preferred in order to obtain a reasonable thickness of at least one monolayer for the thinnest barrier. Another advantage of GaAs is the far infrared performance. Undoped InP substrates have a rather high background doping which causes free carrier absorption.

The band structure of a chirped superlattice design is shown in Fig. 1 [8]. The laser transition takes place between the lowest level of the second miniband and the highest level of the first miniband. The optical matrix element is large but the total lifetime in the upper laser level is short as LO phonon emission is possible to many final states in the first miniband. In the case of a three well design [6], fewer levels are below the upper laser level, and therefore the total lifetime in the upper laser level is longer. A drawback

of the three well design is the lower optical dipole matrix element in comparison to a chirped superlattice design and the slower carrier extraction form the lower laser level.

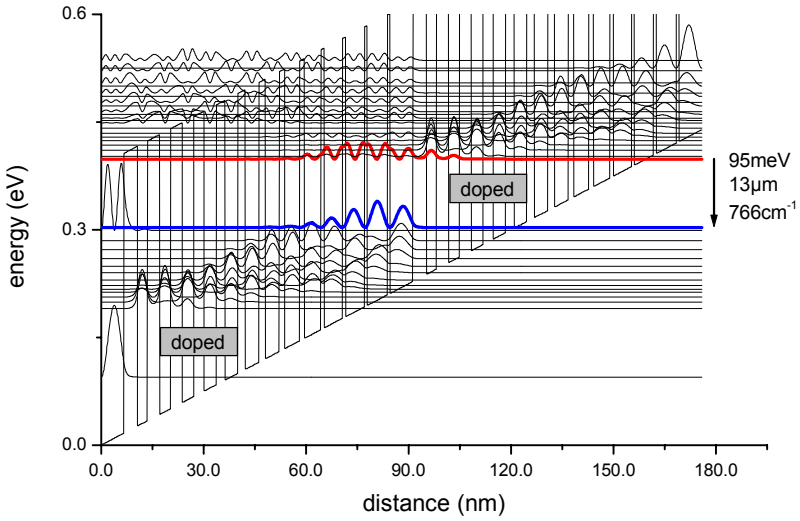

Fig. 1: Calculated conduction band diagram and squared wave functions of a chirped superlattice design for emission at 13 µm wavelength.

Experimental

Sample Preparation

The laser material is grown by molecular beam epitxy on (100) GaAs substrates. The gain media is embedded in the most cases in a double plasmon enhanced waveguide. Such a waveguide consists of ~1 µm thick highly doped cladding layers (~4x10^{18} cm^{-3}), and ~3.5 µm thick low doped spacer layers (~4x10^{16} cm^{-3}). The highly doped layers are used for light confinement and the spacer layers reduce the penetration of the guided mode into the cladding layers as they show huge free carrier absorption. A surface plasmon waveguide [9] is usually used for long wavelength material (λ > 20 µm) because of the reduced thickness, which is important for MBE growth.

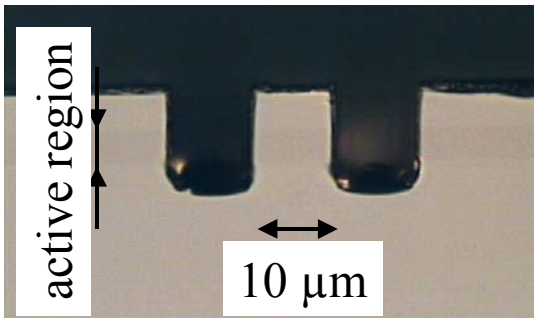

Fig. 2: Image of a laser facet of a 10 µm wide FP laser. The trenches are etched by reactive ion etching.

Different cavity types such as Fabry Perot (FP), distributed feedback (DFB), and cylinder lasers were fabricated. Reactive ion etching was used for directional etching to obtain vertical etch profiles (Fig. 2). SiN is used for insulation and the extended contacts are sputtered. The grating for the DFB lasers was etched into the surface of the top cladding layer and covered with metal. The light is confined by total internal reflection in the case of cylinder shaped lasers. The lasers were soldered with In on Cu plates and wire bonded.

Measurements

Spectral measurements were performed with a Fourier Transform Infrared (FTIR) spectrometer. The absolute light power was measured with a thermopile detector, and the optical power versus current curves were measured in some cases with a DTGS detector or LN_2 cooled MCT detectors, depending on the optical power. Typical operation conditions are 100 ns long pulses and repetition rates in the order of 5 kHz up to several MHz. Pulsed room temperature operation (Fig. 3) was achieved for three different design strategies, a three well design [6], a chirped superlattice design [8], and a bound to continuum design. A bound to continuum design combines the advantages of the three well design and the chirped superlattice and allowed pulsed operation up to 100°C.

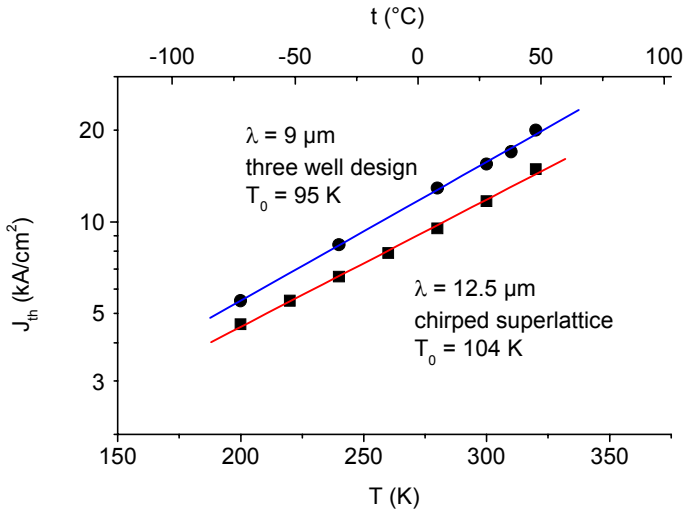

Fig. 3: Threshold current density of cylinder lasers as a function of the heat sink temperature for a three well design (circles) and a chirped superlattice (squares). The lines are fits of the characteristic temperature T_0 ($J_{th} = J_0 \exp(T/T_0)$).

Acknowledgements

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Light from Silicon: SiGe Quantum Cascade Structures

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Recently, encouraging results on electroluminescence of valence band SiGe cascade structures in the mid- and far infrared (THz) spectral regions have been reported. In this paper, we review these results an compare them to **kp** bandstructure calculations based on a strain dependent Luttinger Kohn Hamiltonian.

Introduction

The working principle of a quantum cascade (QC) emitter is based on optical transitions of only one type of carrier (uni-polar emitter). Typically, one period of the cascade consists of an active region and of an injector region. The active region is built up of typically 1 – 4 quantum wells (QW) that are designed for intense emission at the target wavelength, for long non-radiative life time in the excited state of the laser transition and for efficient depopulation of the laser-transition ground-state. The injector consists of a chirped superlattice in that the ground states of adjacent QWs become aligned in energy for a certain voltage drop across the cascade period. At this voltage, an energetically flat miniband is formed in the injector superlattice through that the carriers coherently tunnel from the ground state of the active region to the excited state of the active region of the following cascade period. (For an illustration of the QC principle, see for example [1].) Up to now, quantum cascade lasing has been demonstrated only in structures made from III-V materials. In these systems, the quantum cascades are formed in the conduction band.

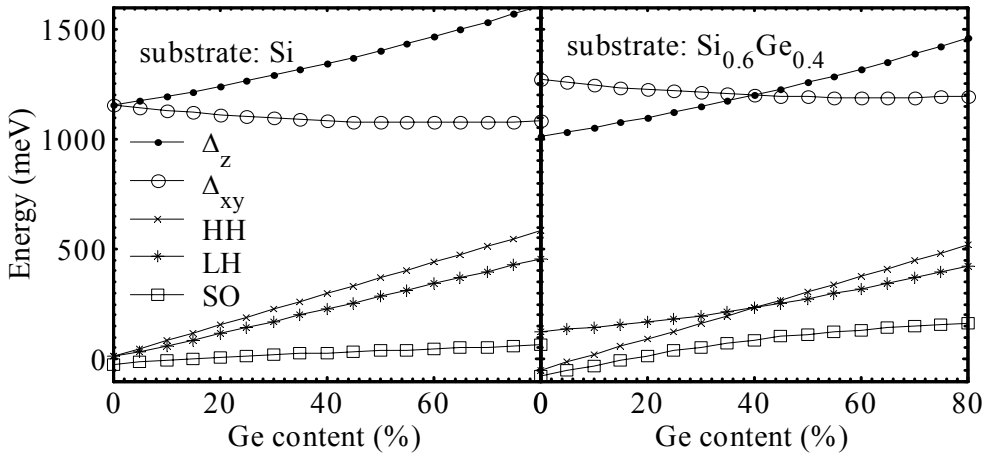

Fig. 1: Calculated band line-up for pseudomorphic SiGe alloys grown on a Si substrate (left panel) and a $Si_{0.6}Ge_{0.4}$.pseudo-substrate (right panel).

Since no optical transitions over the fundamental band gap are involved in the emission process of a quantum cascade device, the QC concept is a promising strategy to achieve light emission also in indirect fundamental band-gap materials like Si and Ge. For the Si/Ge material system, the calculated alignment of the conduction and valence band edges as a function of the SiGe alloy composition is shown in Fig.1. for growth on a Si (left panel) and a $Si_{0.6}Ge_{0.4}$ (right panel) substrate. In the calculations, the parameters given in [2] were used. Due to the uniaxial strain in the epitaxial SiGe layer, the heavy (HH) and light (LH) hole valence band maxima as well as the Δ_{xy} and Δ_z conduction band minima become split. Figure 1 shows that holes are always confined to the Ge rich layers for both types of substrates. The ground states in the valence band QW are HH states, the HH band offset increases by approx. 70 meV per 10% of Ge in the alloy. For electrons, nearly no band offset occurs in the conduction band for growth of SiGe alloys on a Si substrate. For SiGe epitaxy on SiGe substrates, QW are formed in the conduction band of the Si rich layers. The ground states of these QWs are built up from the Δ-valleys in the growth direction. However, the electrons in these valleys have a huge effective mass (0.98 m_0) in the direction of the confinement so the coupling of neighboring QWs is extremely weak. Therefore, all of the work on light emission of SiGe cascades published so far has been performed on valence band QWs.

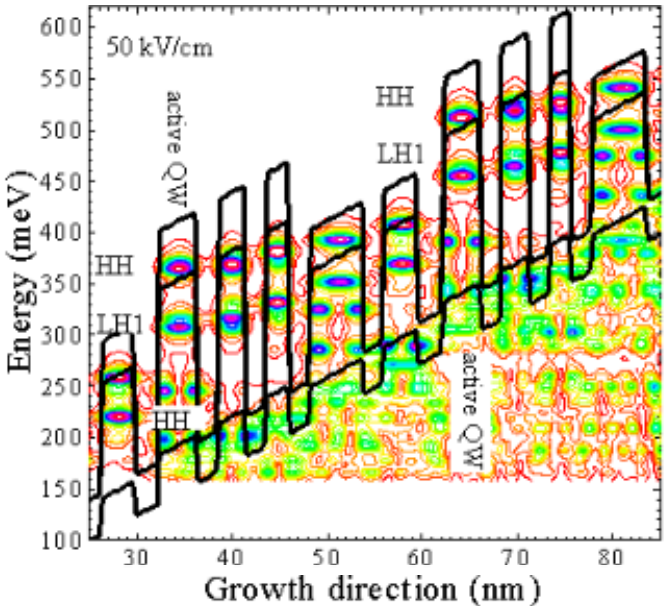

Fig. 2: Valence band potentials, eigenstates and hole wave functions for a typical QC structure grown on Si substrate. The details of the plot are described in the text.

Experimental Results

Mid-Infrared Emission

Cascade light emission in the mid-infrared spectral region around 150 meV has been reported recently [3] – [6]. In Fig. 2, the band structure of a typical Si/SiGe cascade structure [3] calculated according to [2] is shown. The alignment of the HH, LH and split off (SO) hole bands edges are indicated by the dashed, full and dashed-doted lines, respectively. The moduli of the wave functions are plotted as contour lines centered

around their eigenenergy. The broadening of the contours along the energy axis indicates the broadening of the eigenenergies (assumed to be 5 meV FWHM in the calculations). The emission wavelength is determined by the energy difference between the HH1 and HH2 in the QW labeled “active QW” in Fig. 2. From the HH1 state in the active QW, the holes tunnel via the HH groundstates in the neighboring QWs into the HH2 state of the next active QW.

Unlike in the case of cascade structures in the conduction band, in the valence band additional states exist between the HH2 and the HH1 states. These states are the ground states confined to QWs formed by the LH valence bands (labeled LH1 in Fig. 2). Pump and probe experiments have shown that the holes in the HH2 states are efficiently scattered into the LH 1 states by optical phonon deformation potential interaction reducing the hole life time in the HH2 state to approximately 250 fs [7]. Reducing the LH1-HH2 energy difference by a proper design of the active QW below the energy of an optical phonon blocks this recombination channel and enhances the power efficiency of the QC emission by approximately a factor 100 [3].

The growth of sophisticated cascade structures on Si substrates is limited by the accumulated strain energy in the epitaxial SiGe layers. These limitations can be overcome by growth on SiGe virtual substrates: Intersubband absorption of high quality $Si_{0.2}Ge_{0.8}$ QWs on a $Si_{0.5}Ge_{0.5}$ virtual substrate [8] as well as electroluminescence around 175 meV due to a bound-to-miniband transition in a QC structure consisting of up to 30 cascades each containing 14 $Si_{0.2}Ge_{0.8}$ QWs separated by Si barriers grown on a $Si_{0.5}$ $Ge_{0.5}$ virtual substrate [6] were observed recently.

THz Emission

In the THz region, up to now no emission from typical cascades containing an injector and active QW region has been published. However, THz emission from $Si_{0.72}Ge_{0.28}$ multi-QWs separated by Si barriers grown on a $Si_{0.77}$ $Ge_{0.23}$ virtual substrate has been observed [9] under an electrical field parallel to the growth direction. For this sample, the in-plane dispersions in [100] direction of the four hole states within the energy range of the experiments are plotted in Fig. 3.

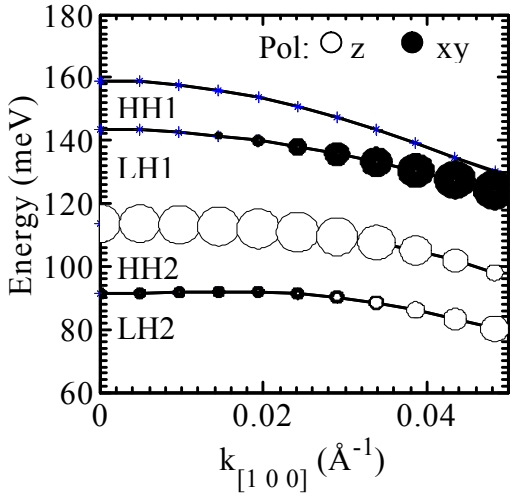

Fig. 3: In-plane dispersion along [100] direction for a $Si_{0.72}Ge_{0.28}$ QW on a $Si_{0.77}$ $Ge_{0.23}$ virtual substrate. The diameters of the symbols indicate the relative size of the optical dipol matrix element for transitions to the HH1 ground state. The open (full) symbols refer to light polarized parallel to z (xy) direction (growth direction: z).

The diameter of the open (full) symbols in Fig. 3 indicates the magnitude of the matrix-element for optical dipole transitions in z (xy) polarization between the HH1 ground and the LH1, HH2, LH2 excited states. Experimentally, the HH1-LH1 as well as the HH1-HH2 emission bands have been observed close to the calculated transition energies (at 10 meV and 40 meV) with the polarization selection rules indicated in Fig. 3 [9]. For the LH2 emission band, the matrix element is calculated to be much smaller than for the LH1 and HH2 bands. Consequently, in the emission experiments, the signal was close to the noise level at the calculated transition energy around 65 meV. In [10], a power conversion efficiency in excess of that observed for III-V *electroluminescence* devices is reported.

Conclusion

Both in the MIR and THz regime encouraging results have been obtained from electro-luminescence experiments. While for the samples emitting in the MIR range, typical QC designs are employed, the samples for THz emission contain a series of uncoupled QWs. The experiments and model calculations indicate that in both spectral regions the realization of Si/Ge based QC lasers appears feasible.

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In-Situ Growth Monitoring and On-Line Composition Determination of MOCVD GaN by Spectroscopic Ellipsometry

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In-situ ellipsometry measurements during MOCVD growth of GaN and its ternary compounds AlGaN and InGaN were performed. We show that individual process steps can be identified and resolved with much higher detail than with currently available reflectometry setups. Using the Virtual Interface Approximation (VIA), we are also able to calculate the Al content of the growing layer in real time with good accuracy. For In containing samples we observe a rather large drift originating from a concentration gradient in the layer due to the immiscibility in the GaN/InN system.

Introduction

Group III nitrides have attracted tremendous R&D effort in the past few years resulting in the commercialization of optoelectronic devices operating in the blue and ultraviolet spectral range. Other fields of application include high mobility transistor devices (HEMT's), UV detectors and laser diodes for tomorrow's range of optical storage products [1]. The fabrication of GaN layers is mostly done by Metalorganic Chemical Vapor Deposition (MOCVD), which provides high growth rates and throughput in a non-UHV environment, both of which are well suited for industrial size production. The range of real-time diagnostic tools for MOCVD reactors is however quite limited, as electron diffraction techniques like RHEED (reflection high energy electron diffraction) cannot be used at atmospheric pressure. Optical methods like spectroscopic ellipsometry (SE) or reflection difference spectroscopy (RDS) have been successfully employed for in-situ monitoring of III-V and II-VI compounds. [2], [3]

We show the successful installation of a spectroscopic ellipsometer to a commercial MOCVD reactor and that these measurements have considerable advantages over reflectometry setups regarding sensitivity and an improved signal-to-noise ratio. Our further attention was focused towards the on-line monitoring of ternary alloy compositions in AlGaN and InGaN layers. The Virtual Interface Approximation (VIA) provides an easy and accurate way of determining the dielectric function of a growing layer which can be correlated to a certain Al content by cross-calibration with ex-situ methods like high resolution X-ray diffraction (HRXRD) or secondary ion mass spectroscopy (SIMS).

Experimental Setup

For the growth of group III nitrides, we use a modified commercial AIXTRON AIX200RF-S reactor with extra viewports to accommodate a spectroscopic ellipsometer. Strain free windows are necessary to avoid stress-induced polarization effects on incident and measured light beams. SE measurements were made with an ISA Jobin Yvon ellipsometer operating in the spectral range of 1.5 – 5.2 eV. Additional characterization was done with a laser reflectometer operating at 1.86 eV.

Figure 1 shows reflectivity and kinetic ellipsometry measurements during the growth of a hexagonal GaN layer on sapphire (0001) substrates. Both measurements have been performed below the fundamental absorption edge of GaN to avoid damping of thickness oscillations. We can clearly identify the important steps necessary to achieve high quality layers [2]:

(a) Heating of the substrate to 1200°C: the reflectometry signal increases due to thermal emission of the sample

(b) Desorption under H_2 atmosphere at 1200°C

(c) Decrease of temperature to 540°C for the deposition of low-temperature GaN nucleation layer

(d) Growth of nucleation layer: an islanded film covering the substrate surface is formed and an oscillation representing the first thickness fringe is recorded

(e) Annealing of nucleation layer through increase of the temperature to 1050°C: The behavior of both signals originates from the coalescence of GaN islands and a roughening of the surface. Spectroscopic measurements before and after annealing show layer thicknesses of 50nm and 30 nm respectively.

(f) Growth of GaN at 1050°C with low growth rate (large period oscillations in both reflectometry and SE)

(g) Deposition of GaN with a growth-rate of ~3 µm/h.

It can easily be seen that all the information contained in the reflectometry signal is also contained in the ellipsometry measurement. In this stage, ellipsometry offers the advantage of being independent of absolute intensities (only polarization and phase change are measured), which makes it immune to influences like wobbling of the sample and thermal emission at high temperatures.

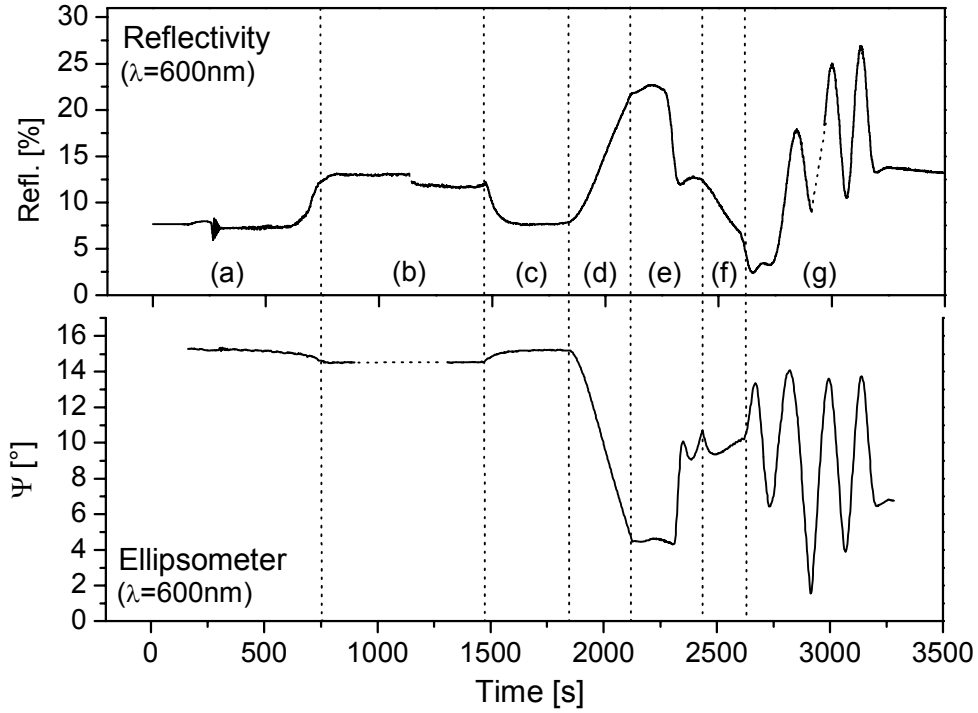

Fig. 1: Reflectometry vs. ellipsometry during the growth of hexagonal GaN layers on sapphire.

Concentration Monitoring

To relate optical information to sample parameters like ternary alloy compositions, it is necessary to perform complementary measurements and relate them to optical data. In our case, we performed high-resolution x-ray diffraction (HRXRD) measurements to gather data about the composition and stress and strain state of the samples. The precision in concentration from these measurements is in the range of ±0.5%.

As there is very little published data of optical constants of these compounds at growth temperature, we had to determine first the dielectric responses of layers with different Al content. Together with the exact concentration values from XRD, it was used as the input data for an algorithm based on the virtual interface approximation (VIA), which determines Al concentrations in real time [4]. The main idea of the VIA is to divide the sample structure into two parts, namely an overlayer and a so-called pseudosubstrate representing the whole structure below. From this 3-layer system (substrate, overlayer, ambient), the dielectric response of the overlayer can be calculated at each time step. The input parameters are the angle of incidence, the monitoring wavelength, the currently measured dielectric function, and its derivative with respect to the thickness of the growing layer. The last point implies the precise knowledge of the growth rate in the case of a measurement with a single wavelength only, which is accomplished by reflectometry in our case.

Figure 2 shows a typical kinetic measurement during the growth of an AlGaN layer. The dielectric function plotted in the complex plane describes an exponential spiral originating from the point for GaN and converging in the point for AlGaN. The inset shows an ellipsometric spectrum at growth temperature.

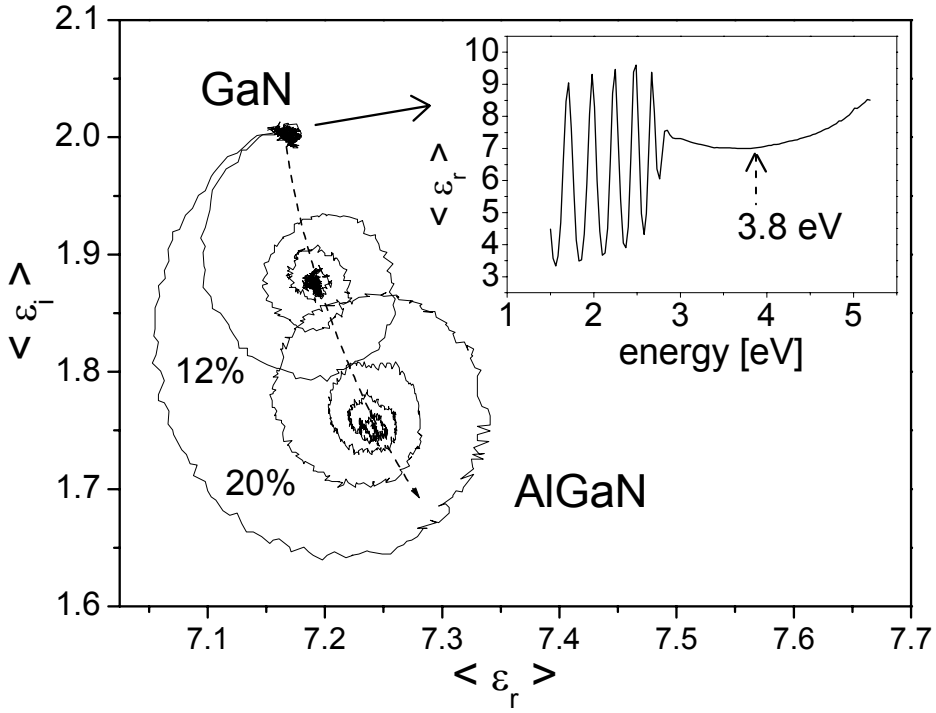

Fig. 2: Evolution of the pseudodielectric function during the growth of AlGaN layers with different Al contents on a GaN buffer. The inset shows a spectroscopic measurement at growth temperature (1050 °C).

A possible application of this method is the monitoring of superlattices as used in devices like vertical emitting laser diodes or transistors. Figure 3 shows the results of a

real-time measurement during the growth of a 30nm/50nm GaN/AlGaN superlattice with 12% Al in the barriers. Also shown in Fig. 3 is a composition profile of a structure with continuously varying Al content.

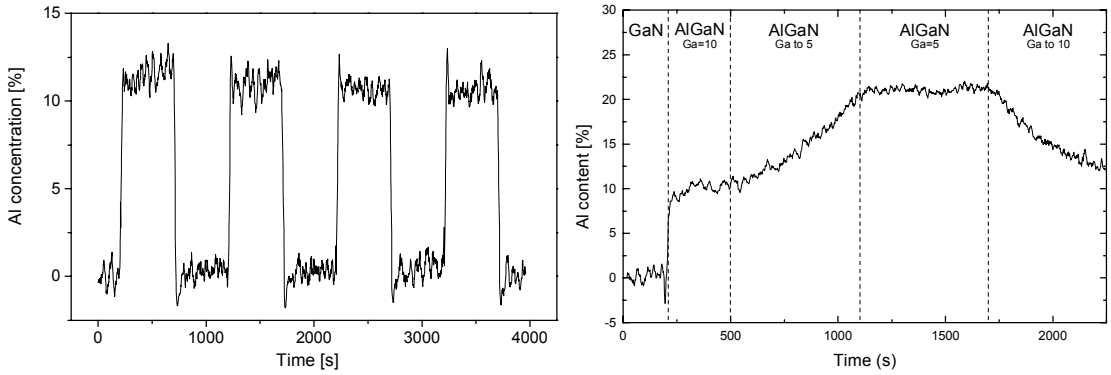

Fig. 3: Left: VIA calculated concentration in a GaN/AlGaN superlattice.
Right: Graded composition layer with Ga fluxes as indicated.

For In containing compounds, concentration monitoring is considerably more difficult. The system GaN – InN has a large miscibility gap resulting in a maximum concentration of a few percent in the crystal. Due to this behavior, InGaN layers also show rather large composition gradients in growth direction [5]. During in-situ measurements, the spirals of the dielectric function do not converge as nicely as for AlGaN compounds. Simulations show that this drift is due to a composition gradient in the layer.

Conclusion

We have demonstrated a method for the optical characterization of MOCVD growth processes of group III nitrides. Characterization of standard growth processes as well as accurate information about ternary layer compositions are obtained in real time thus yielding higher output and enhanced device quality.

Acknowledgements

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Opto-Electronics (Posters)

Electrically Pumped Quantum Cascade Ring Lasers

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Introduction

Circular cavities from a quantum cascade material have been investigated by several groups [1] – [3]. It is generally believed that light propagates as a whispering gallery mode in microcylinder or microdisk [4], [5] cavities. This implies that almost all of the light is at the periphery of the device and the centre of such a device should have little or no influence on the light field. Nevertheless, current will also flow through the centre region and provide gain, which is wasted due to the almost complete absence of a relevant light field. This was a motivation to remove the centre portion of microcylinders and thereby obtain a ring shaped laser cavity (as shown in Fig.1). It was expected that the threshold current required to achieve lasing would drop due to the decreased area of the device.

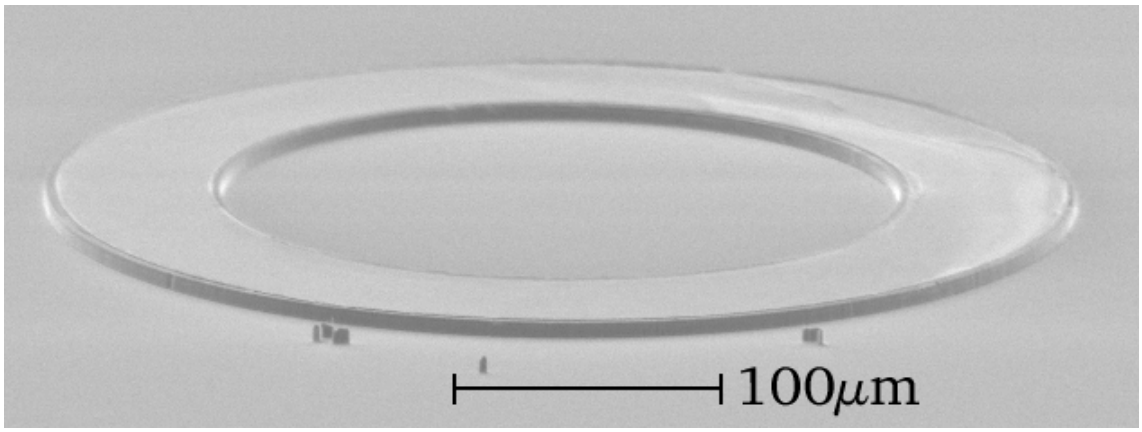

Fig. 1: Ring laser; the height of the laser is approximately 10 μm.

Experimental

The material from which the ring lasers were processed was grown by solid source molecular beam epitaxy. It is based on a three-well design quantum cascade structure. When processed as a standard ridge waveguide, this material functioned at least up to room temperature [6]. An x-ray-rocking curve (shown in Fig. 2) indicates that the actual period of the chosen material is about four percent less than the designed one, but also reveals the accurate periodicity. The deviation between the grown and the simulated period is only 1.8 percent. It thereby denotes the high quality of the material with regard to the cascaded structure and reproducible interfaces.

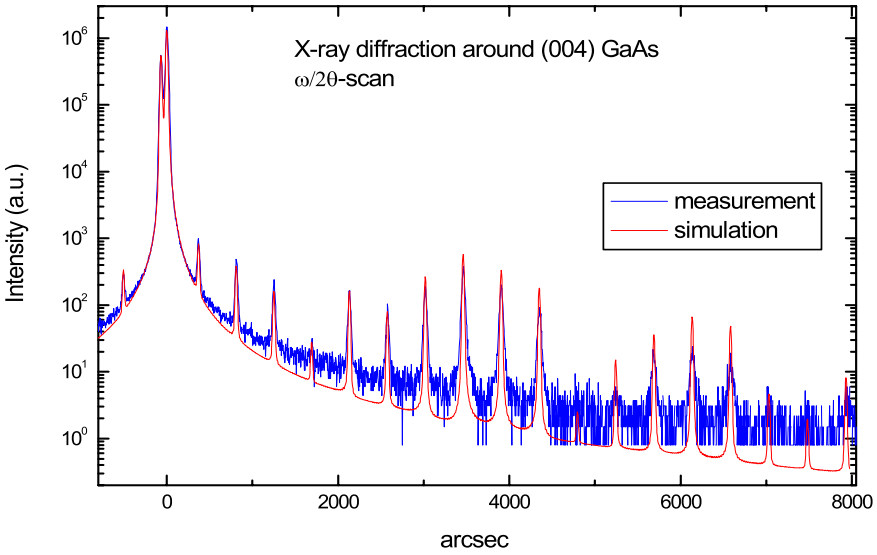

Fig. 2: X-ray-rocking curve.

The rings were processed using standard photolithography and reactive ion etching to achieve smooth and perpendicular sidewalls. These are considered critical for device operation, as deviations from a vertical sidewall will lead to deviations in the length of the optical path. Even small deviations suffice to degrade device performance. This would represent an additional loss mechanism in addition to standard wave-guide losses. Circular cavities that work above room temperature have already been demonstrated [7].

Rings with outer diameters of 200, 300 and 400 µm and various inner diameters were fabricated. Several measurements were conducted, including a temperature dependence of the emitted spectra of the rings (as shown in Fig. 3). It can clearly be seen that the emission wavelength shifts to lower wave numbers and thereby to lower energy as temperature is increased. The frequency shift per Kelvin is somewhat higher than for a Fabry-Perot laser made from the same material where it is in agreement with the temperature dependence of the index of refraction. Presumably, the relatively large shift in emission wavelength indicates an additional loss mechanism in the ring laser. Since the emission wavelengths at higher temperatures approach that of a Fabry-Perot laser from the same material, but shift to smaller wavelengths at lower temperatures, we infer that the additional loss mechanism is less dominant at higher temperatures. But not only the energy of the emitted light changes, but also the number of modes. We note that the number of lasing modes decreases as the temperature increases. This can be attributed to the fact that the lasing threshold increases with temperature and so the same current is not as far above the lasing threshold at different temperatures.

Figure 4 depicts spectra of several rings with a constant outer diameter and different inner diameters. The outer diameter is 400 µm and the inner diameters are varied between 240 and 320 µm in steps of 10 micrometers, with the exception that there is no ring with an inner diameter of 290 µm. The spectra have all been measured at the same temperature of 77 K. The modes are not regularly spaced as would be expected for whispering gallery modes of lowest order. Interestingly, the diameter of the hole influences the emission wavelengths of the lasers, such that the emitted light has a shorter wavelength with decreasing thickness of the ring.

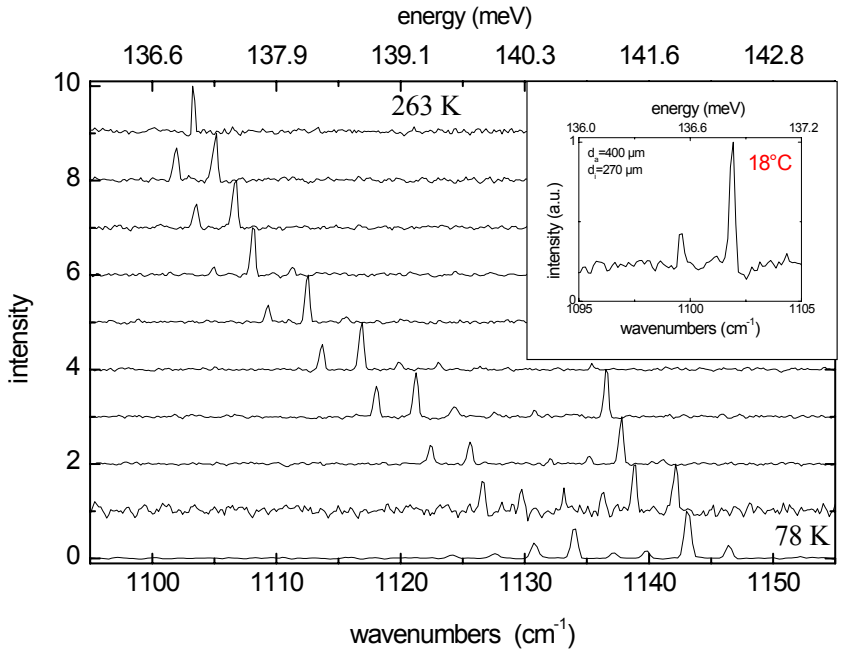

Fig. 3: Temperature dependence of emitted spectra. Temperatures are 78, 98, 118, 138, 158, 178, 198, 218, 238, and 263 K.

This is in contrast to previous assumptions that the light field should not enter the central region of the device and therefore should not be influenced by any changes in the centre section. Considering these facts, it seems necessary to reconsider the idea of whispering gallery modes within these devices.

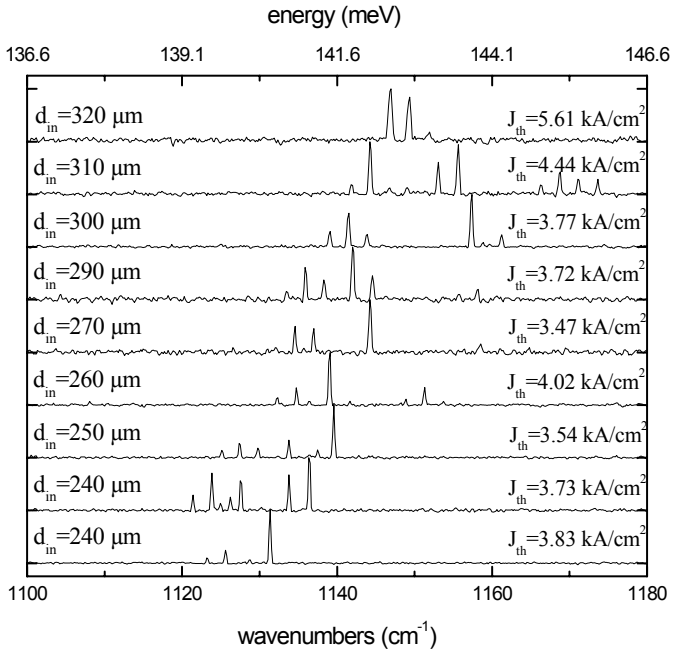

Fig. 4: Spectra of rings of different widths. The outer diameter was 400 µm; the inner diameters are as indicated.

Threshold current densities for the individual lasers are also indicated in Fig. 4. They show a tendency to increase as the inner diameter of the ring increases. We note that the shift in emission wavelength is not caused by a shift in threshold. The threshold current density scatters considerably more than the emission wavelength. Further, we checked that the envelopes of the spectra do not depend on the bias.

Conclusion

We manufactured electrically pumped quantum cascade ring lasers and characterised their optical properties. The emission wavelength was found to be sensitive to changes in the centre section of the device, which is in contrast to the general assumption that circular cavities dominantly support whispering gallery modes. Together with the observation of irregular mode spacing our results suggest that a different mode structure is preferred.

Acknowledgements

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Oriented Organic Semiconductor Thin Films

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In this part of our investigations, we use atomic force microscopy and X-ray diffraction to study the growth of para-sexiphenyl (PSP) films on mica. It is shown that self-organization of PSP molecules occurs during the growth controlled by the substrate temperature and deposition time. X-ray diffraction studies confirmed very high crystalline quality of the grown organic films.

Introduction

The ability to control the molecular order in organic thin films consisting of long anisotropic oligomers like *oligo-thiophenes* or *oligo-phenylenes* is essential to study the relation between their structure, surface morphology and their optical and electrical properties. On the other hand, ordered thin films of organic semiconductor *para-sexiphenyl* (PSP) are interesting for the application in organic light-emitting diodes (OLED) with polarized blue light emission [1]. Recently, we reported that a self-organization of PSP molecules occurs during Hot Wall Epitaxy (HWE) on mica resulting in well ordered crystalline needle-like structures with a length to width ratio up to 500 [2], [3]. However, the growth regularities of such highly anisotropic films were not clear yet. In this work, we have used atomic force microscopy (AFM) and X-ray diffraction (XRD) to investigate the morphology, growth kinetic and crystalline quality of these films in the early growth stages, in order to find the process controlling parameters.

Experimental

PSP obtained from Tokyo Chemical Industries was purified by threefold sublimation under dynamic vacuum. HWE was used as evaporation technique [2], [3]. The used substrates were freshly cleaved (001)-oriented mica. The base pressure during growth was about $6x10^{-6}$ mbar and the PSP source temperature was fixed at 240 ºC. The substrate temperature was 90 ºC or 150 ºC, the growth time was varied between 5 sec and 60 min. The film morphology was imaged by AFM using a Dimension 3100 system (Digital Instruments) operated in tapping mode on air. XRD investigations were performed at the F3 station at the Cornell High Energy Synchrotron Source (CHESS). Monochromatic radiation with a wavelength of 1.23985 Å was used in combination with a 4-circle goniometer.

Results

The PSP film morphology with increasing growth time in the range from 5 to 90 sec is shown in Fig.1. The growth temperature was 150 °C. As depicted in Figs.1 (a) and (b), only small uniformly distributed 3D-islands with a compact shape can be detected for the samples grown within 5 – 10 seconds. The surface morphology changes drastically if growth time was increased from 10 to 25 sec: island shape transition occurs resulting in typical needle-like structures with elongated 3D-islands. Figs.1 (c) and (d) show that the islands become thereby progressively longer, quickly reaching a fixed asymptotic width while their height remains much smaller than their length and width. A similar

behavior was found for the samples grown by 90 °C; however, in this case the island shape transition occurs later – between 25 and 45 seconds of growth time.

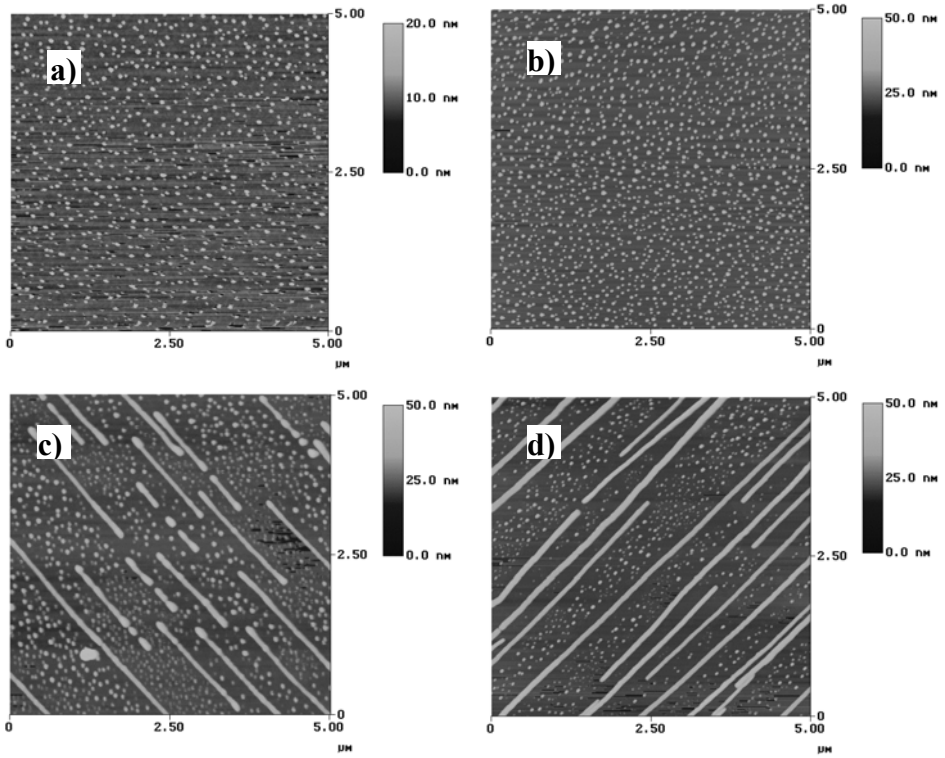

Fig. 1: AFM images of the films grown at 150°C within (a) 5; (b) 10; (c) 25; (d) 90 sec.

Some of these extraordinary features can be explained qualitatively in terms of strain-induced heteroepitaxial island growth, well known in inorganic heteroepitaxy. For example, Tersoff and Tromp [4] have predicted theoretically a strain-induced, spontaneous shape transition from compact square islands to elongated ones of asymptotic constant width. This means that compact 3D-islands grow to a critical size in width and length considerably larger than their height (which remains nearly constant). Above the critical size, the islands grow only in length, but not in width, which converges towards an asymptotic value. Generally, our results agree well with these theoretical predictions.

We performed also XRD measurements in $\Theta/2\Theta$ mode for PSP films of different thickness in order to get information about the variation of interplanar spacing in the growth direction d(11-1) with increasing layer thickness, i.e. about presence of lattice deformation (strain). As shown in Fig.2, the d(11-1) value increases rapidly with increasing needle height approaching the bulk value at a thickness of ≈25 – 30 nm. Such behavior implies that thin PSP layers are strained and this strain is relaxed within the first ≈25 – 30 nm (~60 monolayers) of the film. These observations suggest that weak Van der Waals interactions between the PSP film and the mica substrate are nevertheless strong enough to produce a lattice deformation, which is likely to be the driving force [4], [5] for the needle-like morphology shown in Fig. 1.

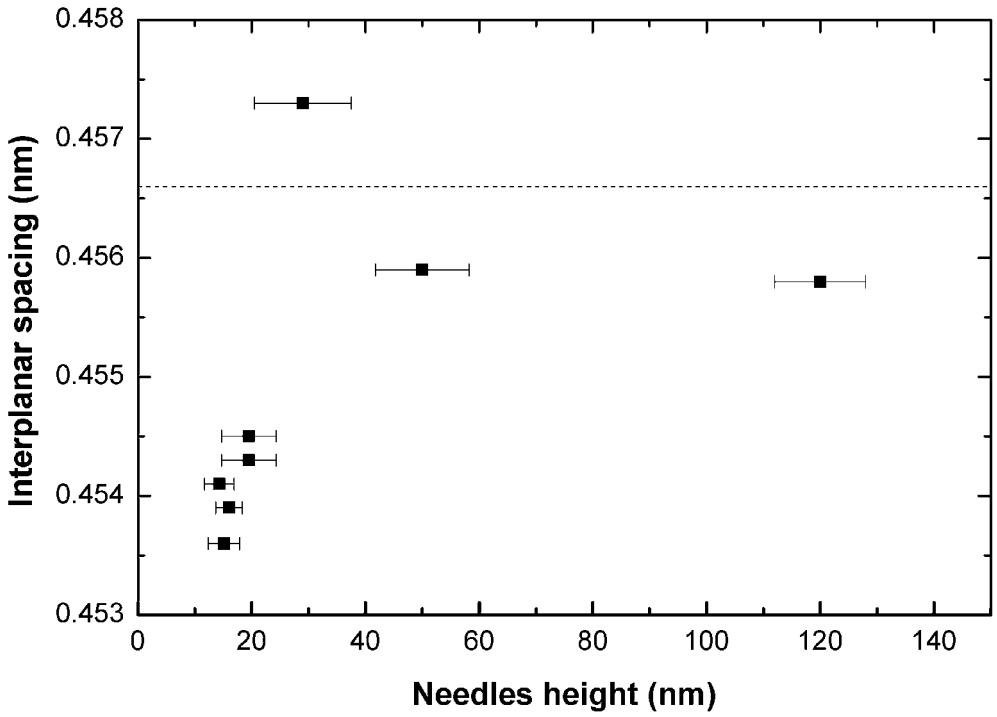

Fig. 2: Interplanar spacing d(11-1) as a function of the average needles height for PSP layers grown at 90°C.

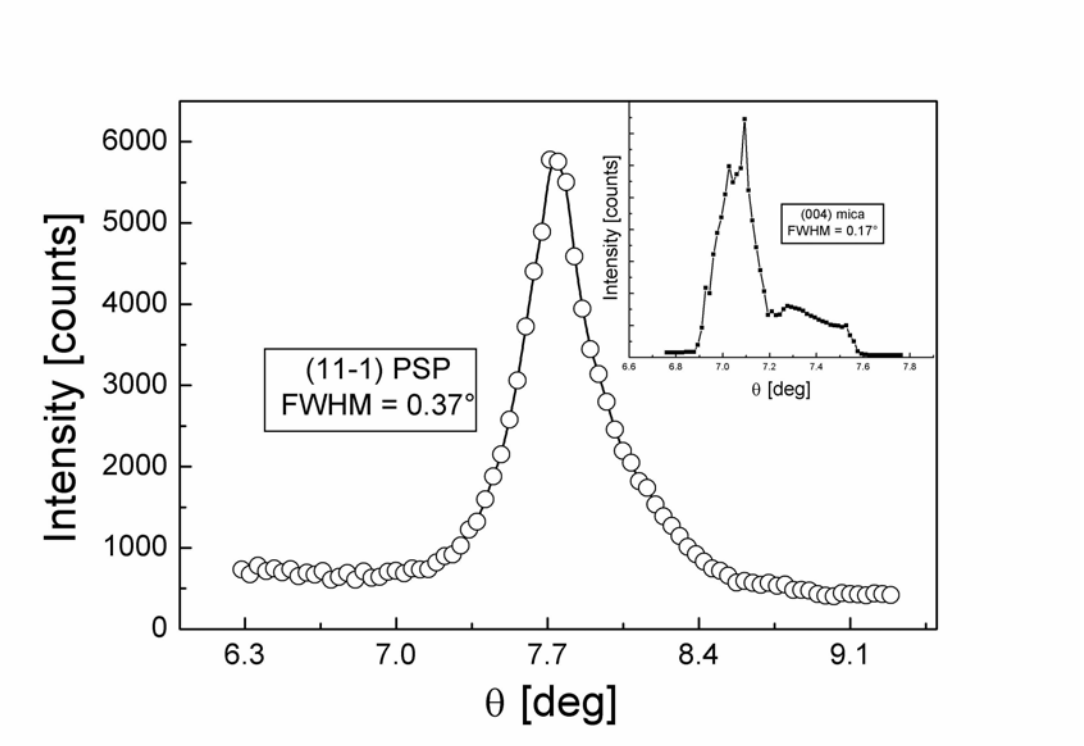

Fig. 3: Rocking curve for the 11-1 reflection of the PSP film. Insert shows corresponding curve for the 004 reflection of the mica substrate.

The so-called Rocking curves (i.e. Θ–scans) provide us a direct measure for the degree of order of the grown films. Additional interest in these investigations arises from the fact that there are only very few papers published, in which rocking curves were reported for organic thin films [5]. Figure 3 shows a typical Rocking curve measured at $2\Theta = 15.67°$ for the characteristic 11-1 reflection of the PSP film grown at 150 °C within 90 sec (see also Fig. 1(d)). The Rocking curve is remarkably narrow for organic films with a FWHM of only 0.37°. For comparison, the Rocking curve of the mica substrate (004) reflection at $2\Theta = 14.26°$ was measured (see inset in Fig.3). The rocking curve of mica shows an irregular shape, which appears often in single crystals of layered compounds like graphite, mica, a.o. The FWHM value of the mica substrate differs not much from the corresponding FWHM of the PSP film itself. These data confirm a very good out-of-plane alignment of PSP crystallites and thus a high degree of order in the film.

Conclusion

The HWE growth of oriented thin films of PSP on mica substrates was investigated. AFM studies of the earlier stage of the growth have clearly shown that self-organization of PSP molecules occurs during HWE resulting in highly anisotropic needle-like structures. XRD investigations using synchrotron radiation confirmed a very high degree of epitaxial order of the films and demonstrated that thin PSP layers are strained and this strain is relaxed within the first ≈25 – 30 nm of the film.

Acknowledgements

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New Generation of Photoconductive Terahertz Emitters

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A photoconductive Terahertz (THz) emitter based on low-temperature-grown GaAs and integrated with Bragg mirror is presented. The emitter exhibits improved terahertz emission efficiency due to the increased pumping light absorption in the Bragg mirror assisted resonant cavity, due to spatial confinement of the photocurrent, and due to optimized photoconductive response.

Introduction

The generation of few-cycle Terahertz radiation into the free space from a biased photoconductive gap illuminated by an ultrashort laser pulse is known more than a decade [1]. Since then, many attempts were presented to increase the generated THz power without compromising the radiation bandwidth [2], [3].

In this contribution, we report on a low-temperature-grown GaAs (LT GaAs) based photoconductive THz emitter integrated with a Bragg mirror. This design improves the generator's THz output power by about one order of magnitude. The optical resonance and the confinement of the photogenerated carriers in the high electric field region of the LT GaAs layer are responsible for the observed enhancement of the THz emission.

In addition, we have focused on optimization of the growth temperature of the LT GaAs layer with respect to a maximum photoresponse of the material and a maximum breakdown field. It is known that annealed LT GaAs changes its properties (resistivity, carrier lifetime) with the growth temperature. Our experiences from THz emission experiments suggest a decrease of the output THz power when the growth temperature is lowered. Therefore, we designed and tested a multilayer LT GaAs structure to increase the performance of the THz emitters.

Photoconductive THz Emitters

A low-temperature MBE GaAs layer grown at temperatures 220 – 350 °C and annealed in-situ at 600 °C (10 minutes) was used as photoconductive material. The modified THz emitter is made of a 326 nm thick LT GaAs grown directly on a Bragg mirror (Fig. 1). The Bragg mirror itself consisted of 30 pairs of $Al_{0.2}Ga_{0.8}As$/AlAs layers designed for a center wavelength of 800 nm. As reference emitter, a 2 µm thick LT GaAs layer was used grown directly on a high resistive GaAs (100) substrate. Electrical contacts to the LT GaAs layers were made of Ti/Au metal and had the shape of coplanar striplines (20 µm wide and separated by a gap of 300 µm (Fig. 1)). The same contact shape was used also for the reference THz emitter structure made of the semi-insulating GaAs. The emitter chips were mounted onto a highly resistive silicon aplanar extended hemisphere lens to efficiently couple the generated THz radiation into free space.

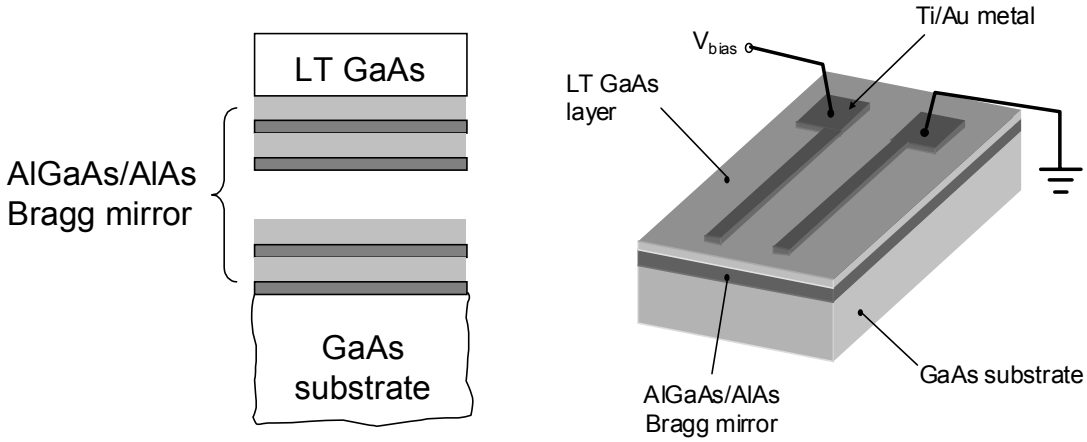

Fig. 1: Schematic of the photoconductive THz emitter.

To access the photoresponse of the LT GaAs layers grown at various temperatures, we used the attenuated unfocused laser beam from a Ti:sapphire laser to homogeneously illuminate the area between the electrodes of the emitter structures. In this configuration, the measured DC photocurrent depends on the lifetime and mobility of the photogenerated charge carriers. As expected, the lagest photocurrent was observed for the emitter structure made of semi-insulating GaAs, a material with the highest carrier lifetime-mobility product (Fig. 2). All structures involving LT GaAs exhibited much lower photocurrent with clear monotonic decrease with decreasing growth temperature.

To compare the emitters with respect to their THz emission efficiency, we have excited the emitter structures with pulses from a *fs* Ti:sapphire oscillator. The repetition rate was 76 MHz and the average excitation power reached about 250 mW. The emitted THz beam was collimated and then focused by a set off-axis parabolic mirrors onto an electro-optic sensor.

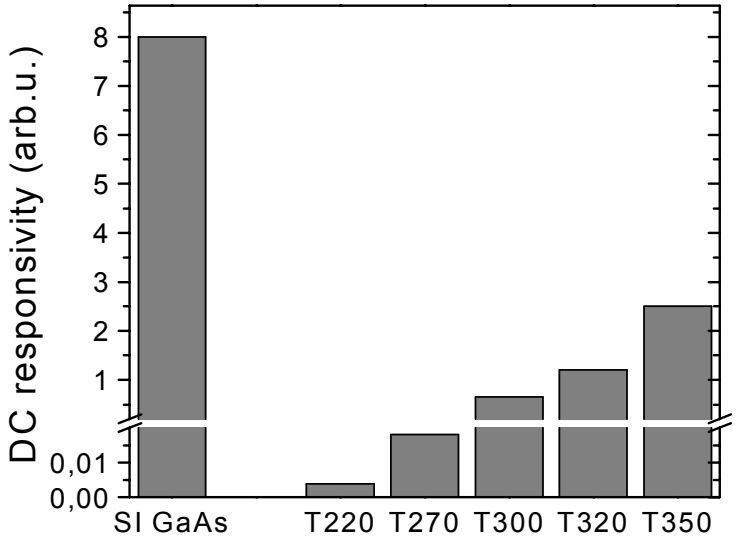

Fig. 2: Photoresponse of the THz emitters.

Figure 3 shows the bias dependence of the amplitude of the THz transients for emitters made of semi-insulating GaAs, a 2 µm thick LT GaAs grown at 220 °C, and a 328 nm thick LT GaAs grown at 220 and 320 °C on the Bragg mirror. The steepest rise of the THz emission with emitter bias was observed for the structure made of semi-insulating GaAs, however, the structure exhibits early breakdown at about 130 V related to heating by the photocurrent. On the other hand, the emitter structure made of 2 µm thick low-temperature GaAs grown at the lowest temperature of 220 °C on semi-insulating GaAs exhibits the weakest increase of the THz radiation with bias. The THz amplitude increases linearly with the applied bias up to 260 V. At biases above 260 V the THz amplitude begins to saturate or even decreases because of Joule heating of the emitter. A heating related device failure is observed for long time operation at these biases. The structure breakdown occurs at biases above 280 V. The lowest THz generation efficiency well correlates with the weakest photoresponse observed for this type of THz emitter (see Fig. 2) and is due to the short lifetime of photogenerated charge carriers and low mobility.

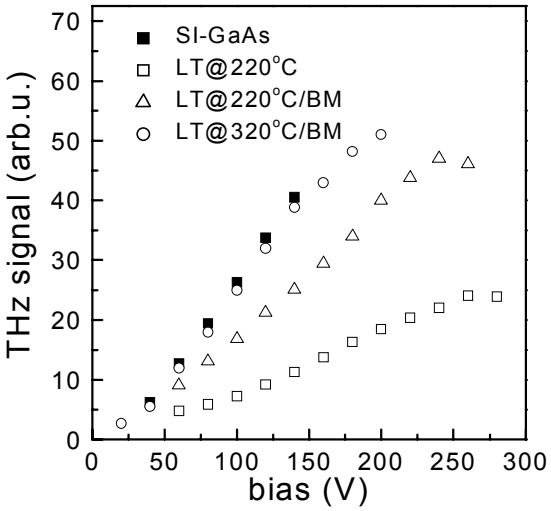

Fig. 3: THz emitter output power as a function of bias.

The emitters based on thin LT GaAs grown on a Bragg mirror exhibit much higher THz generation efficiency in comparison to that based on thick LT GaAs. The presence of the Bragg mirror leads to a doubled THz signal from the same LT GaAs material. The main enhancement is ascribed to the effect of the resonance cavity created by the Bragg mirror, the LT GaAs layer, and the air/GaAs interface. The calculation of the performance of this optical system yields an increased absorption in the LT GaAs [6]. Finally, when we have chosen a LT GaAs material providing a maximum photoresponse (see Fig. 2), the THz generation efficiency has reached a level comparable to that of semi-insulating GaAs. However, the breakdown voltage is higher and so the maximum reachable THz output power. At a bias of 200 V and for an excitation pulse energy of 2.5 nJ the maximum the THz output power was estimated to be 3.8 µW.

Conclusion

The performance of photoconductive antenna THz emitters based on epitaxial GaAs grown at different temperatures on an AlGaAs/AlAs Bragg mirror is presented. The growth occurred at temperatures between 220 and 350 °C. The maximum output THz power was observed for a growth at a temperature of about 320 °C. Moreover, the

resonant cavity effect as well as the effective optical and electrical isolation of the photoconductive layer from the substrate by the Bragg mirror leads to an enhancement of the optical-to-THz conversion efficiency. A photoconductive THz emitter with such a design was recently successfully used as an intra-cavity THz generator in a *fs* oscillator [7].

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Enhanced Luminescence of Erbium Doped Silicon Due to Hydrogen

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Erbium- and oxygen-doped silicon was additionally doped with hydrogen, using plasma-enhanced Chemical Vapor Deposition. Samples treated with solid-phase epitaxy (SPE) before hydrogen doping and annealing at 900 °C after show a large enhancement of the photoluminescence yield. Secondary Ion Mass Spectroscopy gives evidence for an enhanced diffusion of both oxygen and erbium at this temperature towards the surface. This change in local concentration leads to a dominance of the cubic center that is usually only found for lower Er concentrations. Controlled etching shows that the PL does stem from a deeper region with lower erbium concentration. The luminescence yield in the hydrogenated samples is significantly higher even if compared to samples prepared to optimize the cubic center luminescence. We thus conclude that hydrogen can enhance the solubility of the cubic center in Si:Er,O.

Introduction

Erbium (Er) doped semiconductors have attracted a lot of attention as they seem to indicate a way to obtain temperature stable emission at a well defined wavelength [1] – [7]. Furthermore, the wavelength close to 1.5 µm of this emission stemming from an intra-4f-transition coincides nicely with the absorption minimum in conventional optical fibers. The main problem for applying this material system to devices working at room temperature is the temperature induced quenching of the luminescence efficiency. Investigations showed that co-doping of Si with Er and light elements, in particular oxygen (O), leads to a reduction of this quenching [3] and room temperature electroluminescence (EL) and photoluminescence (PL) [4], [5] were subsequently reported.

The low solubility limit of Er in Si necessitates the use of non-equilibrium methods like ion implantation for its incorporation. Because of the required high doses for Er and O, a thermal annealing step for re-crystallization is necessary. To achieve room temperature EL, Er has to be incorporated in $SiO_{2-\delta}$ precipitates, which are formed at high annealing temperatures (> 950 °C) [6]. Both Er and O stay relatively immobile even at temperatures that high. The shallow dopants required for a diode structure, however, show substantial diffusion already at this temperature. [7]

Hydrogen is a very common impurity in all semiconductor materials. Focusing on its positive characteristics – gettering of metal impurities and passivation of residual defects – as well as on the known enhancement of the diffusion of interstitial oxygen [8] and the formation of Er-O complexes and precipitates [9], we expected an overall positive effect on the performance of our structures. We also hoped that hydrogen might decrease the necessary annealing temperature for precipitate formation thus helping to prevent diffusion of the dopants.

Results and Discussion

Samples were prepared from boron doped (10 Ohm·cm) Cz-Si (100) with an oxygen content of approx. 2 x 10^{18} cm^{-3}. Er was implanted at 300 keV with a dose of 1 x 10^{14} cm^{-2} resulting in a peak concentration of 5 x 10^{18} cm^{-3} in 100 nm depth. Oxygen was implanted at 40 keV with a dose of 1 x 10^{15} cm^{-2} resulting in a peak concentration of 5 x 10^{19} cm^{-3}. Both profiles overlap spatially according to TRIM code simulation and SIMS. Two sets of samples were prepared – one treated by SPE (600 °C/15 min. in N_2 atmosphere), the other "as implanted" – and hydrogenated for 1 hour at 260 °C by a hydrogen plasma (110 MHz, 200 sccm hydrogen flux, 400 mTorr pressure) which leads to a hydrogen concentration of about 10^{19} cm^{-3} throughout the wafer [10]. The samples were then annealed at various temperatures in the range between 450 °C and 1000 °C.

In samples not treated with SPE, the effect of hydrogen is rather limited. The Er-related line spectra closely resemble those in samples without hydrogen treatment, although the intensity due to Er-O complexes is smaller in respect to the cubic lines than in non-hydrogenated samples at elevated annealing temperatures. In samples previously treated with SPE, the PL-intensity is slightly higher than in the reference samples at first. The peak PL-intensities of the annealed samples are shown in Fig. 1 as a function of annealing temperature. The difference becomes significant at higher annealing temperatures (800 and 900 °C), where the luminescence yield is about five times bigger than in the non-hydrogenated samples.

Furthermore, we observe a change in the PL spectra. For samples with hydrogen and annealing temperatures larger than 700 °C, the so-called "cubic" center becomes more and more prominent, and it dominates the spectra after annealing at 900 °C. This center is attributed to Er on an interstitial site and was previously only observed in samples with a low concentration of Er, i.e., when the implantation doses are below the amorphisation limit [11]. The lines due to Er-O complexes are completely absent for samples annealed at 900 °C.

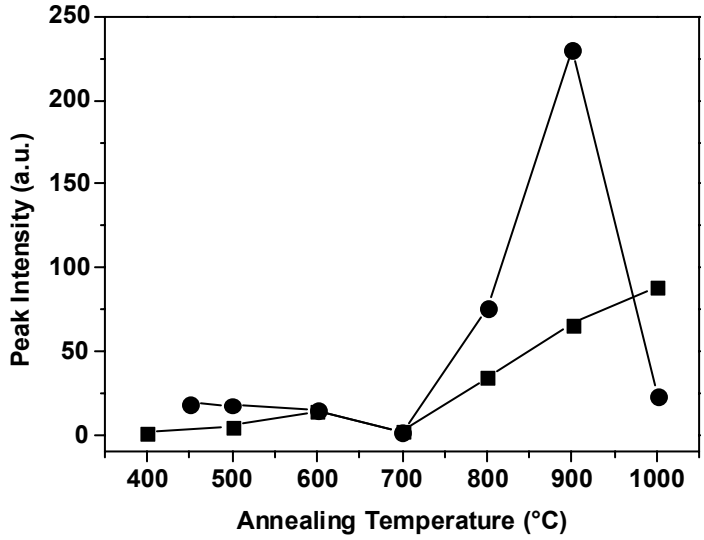

Fig. 1: Peak intensities versus annealing temperatures. Circles show the intensities for the hydrogenated samples, diamond symbols represent the reference samples.

We applied SIMS to gain information on possible changes in local concentration. The results show that hydrogen does not only enhance the diffusion of oxygen but also af-

fects erbium. The usual Gaussian profile is broadened and an accumulation of both species near the surface can be clearly seen. Most of the Er is concentrated within 50 nm of the surface reaching concentrations of up to 1020 cm^{-3}.

To determine the origins of the luminescence we removed 60 nm from the top of the wafer using reactive ion etching. However, although we removed approx. 80 % of the incorporated erbium according to SIMS, the luminescence dropped only by 10 %. This observation points strongly to a PL origin in the region with lower concentration further inside the sample. Using the incorporated doses and the SIMS results as landmarks, we estimate the remaining concentration of erbium in the sample to be approx. 3×10^{12} cm^{-2}. Maximum PL yield for the cubic center is achieved for an implantation dose of 1×10^{13} cm^{-2} and annealing temperatures of 900 °C. Comparing the PL yield to such samples, the intensity is still significantly higher in the hydrogenated samples (Fig. 2). This is an indication for a higher percentage of optically active erbium in our hydrogenated samples.

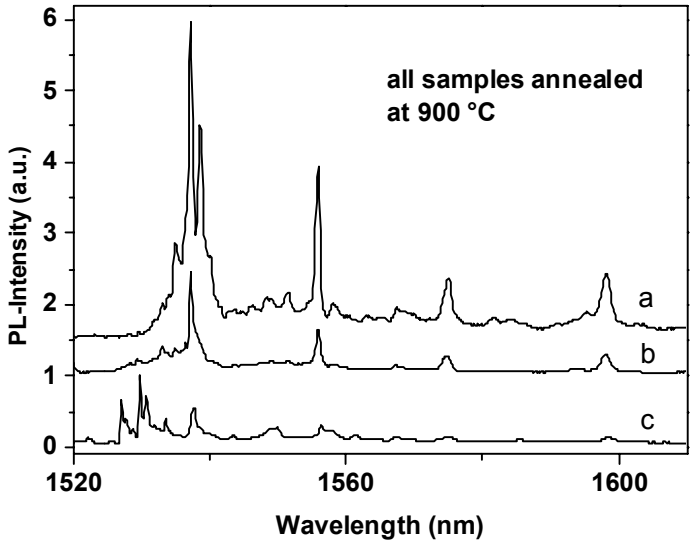

Fig. 2: (a) The cubic lines dominate the PL-spectra in the hydrogenated samples. (b) Spectra of a sample with low Er concentration and (c) of a reference sample (set 4) are shown. The lines at 1.53 µm due to Er-O complexes are absent in the hydrogenated sample. Spectra shifted for clarity.

Studies of power dependence support this interpretation. In the high power regime, the PL-yield I_{Pl} is given by $I_{PL} \propto N_{Er}^{*} / \tau$ with N_{Er}^{*} being the number of optically active erbium and τ being the radiative lifetime. The hydrogenated samples show a higher saturation intensity compared to both the reference sample and samples optimized for cubic center luminescence. The comparison to the reference sample is valid, because although the emitting center is different, the lifetime is identical for both centers [12]. The higher saturation intensity demonstrates a higher number of optically active erbium ions. The “thermal” quenching of the PL intensity with increasing temperature is not influenced by hydrogen. So additional co-doping with hydrogen does not help with room temperature applications. However, it may be advantageous for applications at low temperatures to make use of the higher percentage of optically active erbium and the narrow linewidth [11] of the cubic center.

Conclusion

In summary, hydrogen influences the PL of Si:Er,O indirectly by mobilizing the implanted Er and oxygen. SIMS measurements give evidence for an enhanced diffusion of both species at elevated temperatures towards the surface. Subsequently the local concentration of both dopants is changed. This change in local concentration leads to a dominance of the cubic center, which is usually only found for lower Er concentrations. We find a substantial increase of the luminescence yield for annealing temperatures in the range of 800°C to 900°C. The luminescence yield in the hydrogenated samples is significantly higher even if compared to samples prepared to optimize the cubic center luminescence. Comparing luminescence yield and local concentration, we obtain strong indications for an enhanced solubility of the cubic center in samples co-doped with hydrogen.

Acknowledgements

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Time-Resolved Measurement of Intersubband Population Dynamics

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We apply an interband pump/intersubband probe technique to monitor the temporal evolution of the electron population in the first and second subband of an undoped GaAs/AlGaAs asymmetric double quantum well after interband optical excitation. The spacing between the two subbands is smaller than the longitudinal optical phonon energy. The time dependence of the intersubband absorption can be explained by a simple rate equation model. We extract an intersubband lifetime of T_{21} = 14 ps at an excitation density of $n_S = 1 \times 10^{10}$ cm^{-2}.

Introduction

Semiconductor nanostructures are fascinating quantum systems, which allow engineering of wavefunctions and transition energies. The development of quantum cascade lasers [1] has shown that applying quantum mechanics can lead to new optoelectronic devices. Several other novel devices have been proposed employing intersubband transitions in semiconductor nanostructures [2]. For all these proposals, the population dynamics and the dephasing times are the most crucial parameters. Ultrashort optical pulses with a large spectral width make it possible to study dephasing and relaxation times of carriers in the subbands of quantized structures. The optical pulses can be used to generate ultrashort broadband mid-infrared (MIR) pulses making it possible to measure the complete time-resolved absorption spectrum of a sample with a single pulse, offering simultaneously high resolution in both the time and frequency domains. In our experiment, an interband pump pulse injects electrons into the first and second subband of an undoped asymmetric double quantum well (ADQW) with a level spacing smaller than the LO phonon energy. The time evolution of the electron population in these two subbands is monitored by probing the MIR intersubband transitions to a third (empty) subband. The direct measurement of the subband populations allows us to determine whether there is intersubband THz gain in optically pumped structures.

Experimental

The ADQW sample was grown by molecular beam epitaxy on a semi-insulating (SI)-GaAs substrate. It consists of 40 periods of undoped GaAs wells with widths of 75 Å and 65 Å, separated by a 25 Å $Al_{0.30}Ga_{0.70}As$ barrier. The separation between each double well is 200 Å. A 100 Å AlAs sacrifice layer was grown between the substrate and the ADQW epilayer film. The sample was cleaved into a 1×1 mm^2 piece and etched for about 6 h in 10 % HF. After the QW film had been lifted off the substrate it was bonded via van der Waals forces to the base of a ZnTe prism. The prism forms a waveguide for the mid-infrared probe pulse and enables a considerable electric field component along the growth axis to achieve a strong coupling to the intersubband transition dipoles. Moreover, the ZnTe prism is (in contrast to GaAs) transparent for the probe as well as for the pump light, which allows collinear pumping to achieve a high time-resolution. The difference between the refraction indices of ZnTe in the near- and mid-infrared regions, however, leads to a walk-off between the pump and the probe

pulses that typically amounts to 150 fs. This is the time resolution that can be achieved in this geometry.

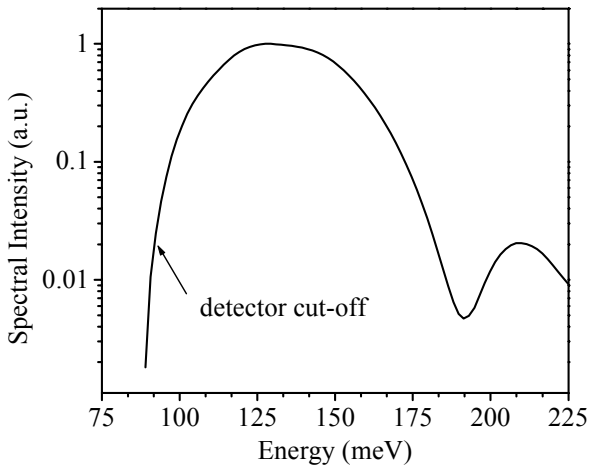

Fig. 1: Intensity spectrum of the MIR probe pulse generated by phase-matched difference frequency mixing in GaSe.

In our time-resolved photoinduced absoption (PIA) setup we use a mode-locked Ti:sapphire laser that delivers 12 fs pulses at a repetition rate of 75 MHz with an average output power of 800 mW. The laser pulses are centered at a wavelength of 780 nm, and the bandwidth is 110 nm (full width at half maximum). The laser beam is split into three parts: *pump*, *probe* and *analysis* beam. The *pump* beam is sent through a variable delay stage and is then used to excite the sample. The desired pump-pulse spectrum is selected through a grating pulse shaper. The sample is mounted on the cold finger of a He continuous flow cryostat and cooled to approximately 5 K. The *probe* is focused on a 30 µm GaSe crystal to generate the linear polarized MIR probe pulse through phase-matched difference mixing [3]. To satisfy the phase-matching condition the polarization of the laser pulse is rotated with a half-wave plate by about 45° out of the horizontal. By changing the orientation of the GaSe crystal it is possible to generate p- or s-polarized light. The MIR radiation transmitted through the sample is then focused on a liquid nitrogen cooled HgCdTe detector. This part of the setup corresponds to a conventional pump-probe experiment in which the total energy of the probe pulse is measured as a function of time delay after excitation. However, the determination of the electric field of the probe pulse requires heterodyne detection. This can be achieved by generating a quasi-single-cycle MIR pulse through optical rectification of the 12 fs *analysis* pulse in a 100 µm ⟨110⟩ SI-GaAs sample. In order to obtain time-resolution, the probe and analysis pulses are mixed at a Si beamsplitter and their superposition is detected as a function of time delay with the time-integrating HgCdTe detector. The signal is collected with a lock-in amplifier phaselocked to an optical chopper which modulates either the pump beam (PIA scan) or the analysis beam (reference scan). Figure 1 shows the intensity spectrum of the MIR probe pulse obtained through Fourier transform of the cross-correlation signal.

Results and Discussion

Figure 2 (a) shows intersubband absorption spectra taken at different time-delays after the excitation by an interband pump pulse. The spectra clearly exhibit two absorption peaks: one around 112 meV, the other one 14 meV above this value. The low-energy peak is due to the (2-3) intersubband absorption, while the second peak is attributed to

the (1-3) absorption. The amplitude of the first peak decreases with time-delay after excitation due to intersubband relaxation, while the amplitude of the second peak first rises slightly, and subsequently decreases due to carrier recombination. Since the area under the peak (i-3) (i = 1, 2) is directly proportional to the subband population $n_i(t)$, we are able to determine the population dynamics in the quantum well on the basis of the time-resolved absorption spectra [4]. Fig. 2 (b) shows the electron population of the first and second subband as a function of time delay after optical excitation (symbols). About 40% of the photo-excited carriers (1 x 10^{10} cm^{-2}) are injected into the second subband, while the remaining 60% are injected into the first subband at higher k-value. The population in the second subband (squares) shows an exponential decay. The carriers relaxing down from the second subband add to the population in the ground level. Subsequently, the population in the ground level drops due to carrier recombination. The lines in the inset of Fig. 2 (b) are the results obtained from a simple rate equation model. By fitting the calculation to the experimental data we deduce an intersubband relaxation time of T_{21} = 14 ps.

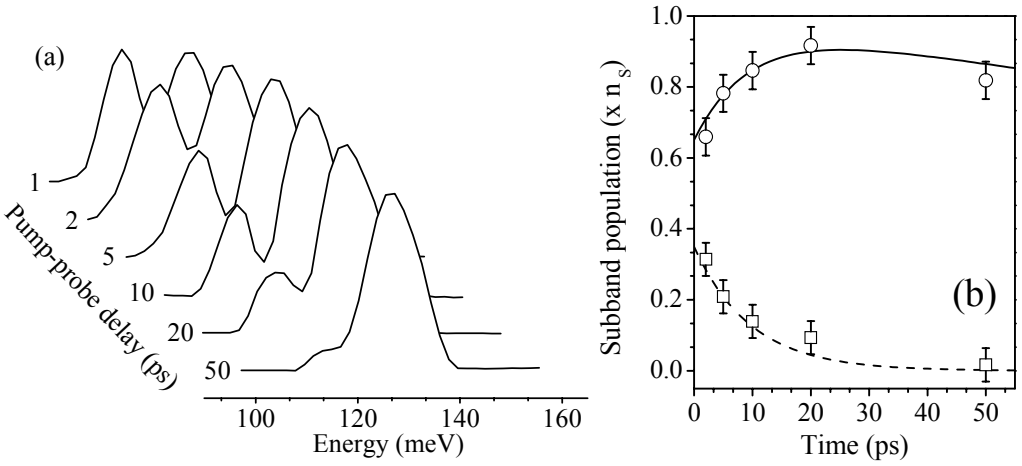

Fig. 2: (a) Time-resolved intersubband absorption spectra for the ADQW sample.
(b) Population in the first (solid line) and second (dashed line) subband.

We will now discuss possible intersubband scattering mechanisms and compare numerical estimates of scattering rates with the experimental results. Since the subband spacing in our sample is smaller than the LO phonon energy the electrons in the second subband do not possess sufficient energy to emit LO phonons and intersubband relaxation can only be due to acoustic phonon emission and electron-electron (e-e) scattering. We calculated the acoustic phonon scattering time to be some hundred ps for our structure. This time is much too long to explain our experimental findings. Recent calculations, however, show that the intersubband e-e scattering rates can be very high, almost approaching in some circumstances the intersubband scattering rate due to LO phonon emission [5]. We calculated the e-e scattering rates in the Born-approximation using static single subband screening within the random phase approximation. The most prominent intersubband e-e scattering processes are labeled 2211 and 2221, where *ijfg* describes an interaction, where an electron in state *i* scatters to *f* under collision with a second electron, which scatters from *j* to *g*. When working out the total population transfer rate between the first and second subband, both scattering processes and the number of electrons that are transferred by each process were taken into account. We calculated an intersubband e-e scattering time of $T_{21} = (2\ W_{2211} + W_{2221})^{-1}$ = 18 ps which is in good agreement with the experimental result. Some authors have also observed a strong reduction of the intersubband relaxation time due to

fast relaxation of electrons in the high-energy tail of the hot carrier distribution in the second subband by emission of LO phonons [6]. Due to the small subband spacing of our sample and the low excitation density, however, the injected electron population in the second subband is cold enough that LO phonon emission is suppressed. Finally, we should also mention our study of the excitation density dependence. We have measured photoinduced intersubband absorption spectra when varying the excitation density from 1 x 10^{10} to more than 1 x 10^{12} cm^{-2}. With increasing densities we observe a significant shortening of the relaxation times. Whereas, in the high density regime we observe a steep increase of the intersubband relaxation times (due to Pauli blocking of the final states). A similar excitation density dependence has been observed by Hartig et al. in a time-resolved photoluminescence experiment [7].

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Modification of the Photoresponse by Energy Level Engineering in InAs Quantum Dot Nanostructures

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We design the energy structure and the absorption properties of infrared photodetectors based on the combination of quantum dots structures with a surrounding superlattice. By embedding vertically coupled or decoupled quantum dots in a two-dimensional superlattice, the advantages of self-organized growth and band structure engineering can be combined. The transition energies and the form of the transition peaks between the dot levels and the extended states of the superlattice can be adjusted by the period of the superlattice and the dot alignment. We use this scheme in photodetectors made of InAs quantum dots embedded in an AlAs/GaAs superlattice. Besides the reduced dark current compared to devices without a superlattice we can demonstrate clear advantages of vertically coupled dot stacks compared to uncoupled dots in this application.

Introduction

InAs and InGaAs quantum dot (QD) ensembles embedded in GaAs matrices or GaAs quantum well structures offer remarkable properties for fast and efficient optoelectronic devices such as NIR lasers [1]. The energy spacing of electronic states coupled with efficient electron capture capabilities into these discrete states predestine dots to be used as MIR photodetectors and emitters. In contrast to subband transitions in two-dimensional structures, the density of states is peaked at the transition energy, which reduces the phase space for scattering. Thus, QD structures are expected to provide higher photocurrents and lower dark currents than quantum well structures due to the longer lifetime of the excited states [2], [3].

The infrared photoresponse of InAs dots embedded in GaAs was investigated very recently [4] – [9], and transition energies between the dot ground state and the GaAs conduction band were found in the range of 80 to 400 meV. In some cases the existence of the first excited dot state [4] or even higher excited states [6] could be observed. It was also shown that the electronic states within the QD and thus the emission or absorption energies can be tuned by changing the InAs dot size [10]. Further methods to lift the energy levels of the InAs QDs is the incorporation of an AlAs layer close to the QDs [11] or the confinement in an $Al_xGa_{1-x}As$ matrix causing a higher conduction band offset to InAs [12].

In this paper we demonstrate that band gap engineering combined with vertical dot alignment allows tailoring of transition and ionization energies as well as absorption properties for mid-infrared (MIR) and far-infrared (FIR) photodetectors. Because the band structure of the minibands in the superlattice (SL) is not, or only slightly, altered by the embedded QDs, their properties can be tuned independently from each other. While the dot properties are modified by their growth conditions, the SL band structure can easily be estimated by solving the one dimensional Schrödinger equation numerically.

Experimental

The basic device structure and a band structure scheme in growth direction are given in Fig. 1 (a). The devices were grown at 485 °C on a semi-insulating GaAs(001) substrate by molecular beam epitaxy. Three multiple dot (MD) device structures – denoted as MD-A, MD-B and MD-C in the following – were designed, grown and characterized. Device MD-A consists of periodically arranged InAs QD layers, which are spaced by a 10 nm thick GaAs matrix. As shown in [8], this thickness is thin enough to cause a vertical alignment of the QDs due to their strain distribution. Device MD-B is additionally provided with 1 nm thick AlAs barriers at a distance of 1 nm from the QD layer resulting in a SL period of 11 nm and an increase of the absorption energy in comparison with device MD-A. The SL period of MD-C is 14 nm. Single dot (SD) and double dot (DD) devices were fabricated by growing one (SD) or two (DD) SL periods under the same conditions as device MD-B. These layers are followed by 2 SL periods without QD layers preventing the vertical alignment of the QDs. This sequence is repeated several times in such a way that the total number of QD layers in all devices is 20 or 30 (only MD-A).

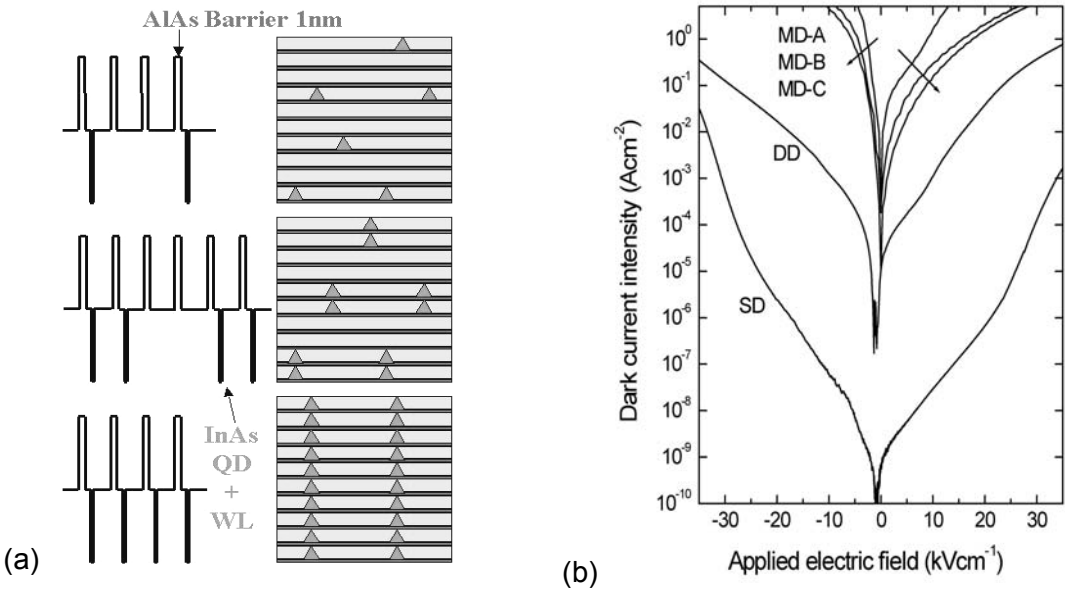

Fig. 1: (a) Device structure; (b) Comparison of dark current behavior.

For characterization of the devices, we performed photoluminescence (PL), photocurrent (PC), and current-voltage (IV) measurements in a LHe flow cryostat system. For the PC measurements, the devices were processed into mesas and provided with a back and front contact made of a thermally alloyed Ni/Ge/Au layer. The spectral photoresponse of the devices is measured in a standard FTIR spectrometer with a glow-bar infrared source.

Results and Discussion

The PL spectra of MD devices at 5 K shown in Fig. 2 are characterized by a PL peak at 1072, 1105, and 1100 meV for device MD-A, MD-B and MD-C, while there is a considerable and continuous shift of the PL peak energy to higher energies in the order of device MD-B, DD and SD in Fig. 2. In the first group, the peak is believed to be due to an electron-hole recombination between the heavy hole and electron ground state of

the QD. The second PL feature at higher energy, which is dominant in the second group, is attributed to higher excited states of the dot ensembles.

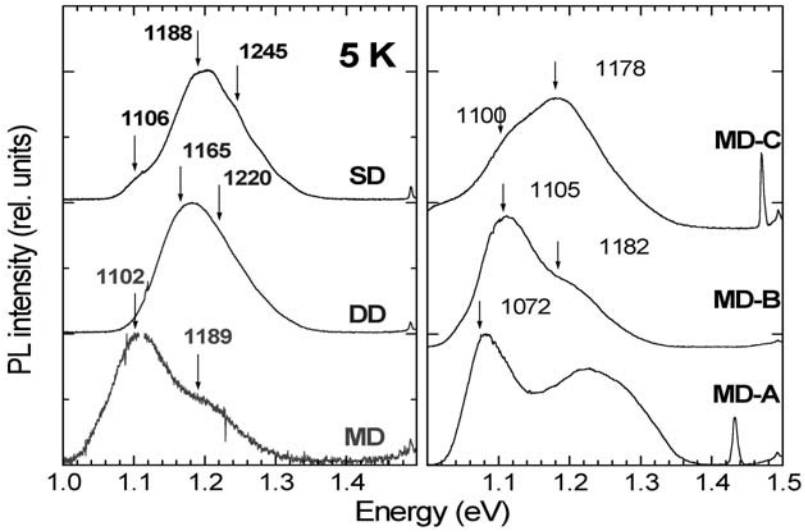

Fig. 2: Photoluminescence spectra of the different device structures.

PC spectra of MD devices at 4 K in Fig. 3 (a) are characterized by a single main peak at around 225 meV (device MD-A, MD-C) and at 247 meV (device MD-B). The full width at half maximum (FWHM) of these peaks amounts approximately to 13, 16 and 11 meV for device A, B and C, respectively. These peaks are assigned to the transition from the dot ground state to the continuum (device A) or to the first miniband of the SL (device B, C). Without vertical coupling of the QDs the situation becomes more complex and several PC peaks in the energy range between 170 and 320 meV can be observed (Fig. 3 (b)). It should be noted that the energy region between 190 and 200 meV is obscured by water absorption lines.

The IV characteristics of the devices at 4 K in Fig. 1 (b) show an asymmetric diode-like behavior. The dark current for the MD devices decreases by one order of magnitude from MD-A to MD-C. A larger decrease of the dark current is even seen in the order of MD-B, DD and SD.

The experimental results are used in the following to reconstruct the energy level scheme of the devices. In the following the heavy hole and electron ground state of the InAs QD are denoted as HH0 and E0, whereas the first excited electron state of the InAs QD and the first miniband of the AlAs SL is indicated with E1 and MB1, respectively.

According to the measurements an energy spacing of 1072 meV between HH0 and E0 and of 224 meV between E0 and the GaAs conduction band (CB) has been found for device MD-A. Although the dot growth conditions are the same for all devices, an enhanced energy spacing of 1105 meV between HH0 and E0 is observed for device MD-B in the PL measurement.

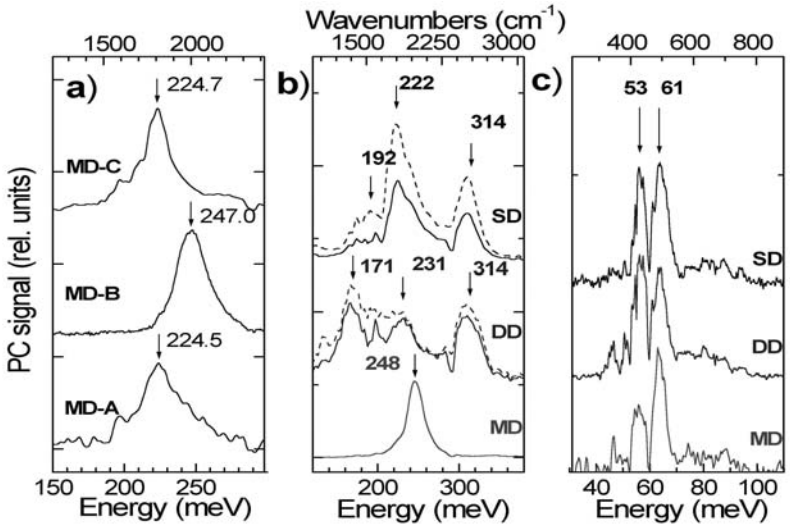

Fig. 3**:** Photocurrent spectra for the MIR region (a) and (b): (c) PC in the FIR region.

In [13], the calculated energy spacing for this transition is blue shifted if the dots are grown close to an AlAs barrier. As a result, the HH0→E0 transition energy increases by 33 meV in our sample. Because of the considerably heavier hole mass, we suppose in a first rough approximation, that the HH0 state remains nearly unchanged, and that the E0 state is lifted by the whole amount of 33 meV [14]. The energy of 247 meV obtained from PC measurements for the E0→MB1 transition can be now split into an energy of 191 meV for the distance E0→CB and an energy of 56 meV for the distance CB→MB1. The position of MB1 was calculated to expand between 48.6 and 53.2 meV above the CB.

The larger SL period of device MD-C lowers and narrows MB1, which now extends between 30.1 and 32.3 meV above the CB. The PC peak at 225 meV leads directly to the experimental value of 29 meV for the CB→MB1 transition. This value and the decrease of the width of the PC peak are in good correspondence with our theoretical prediction. Because of the SL the dark current in MD-C has been decreased by more than one order of magnitude (Fig. 1 (b)) compared to MD-A.

Without or with reduced vertical alignment the description becomes more complicated. Now three different cases have to be distinguished: a SL period without an InAs wetting layer, a SL period with a wetting layer, and a SL period with QD and wetting layer. Additionally to the MB1 in the first case, the wetting layer introduces a ground and first excited state WL0 and WL1. The split up of the former MB1 position in the case of DD and SD devices now enables several transitions to become likely, in good agreement with Figs. 3 (b) and (c). Unfortunately, the rough approximation to describe the QDs by thin quantum wells in our calculation does not allow a quantitative prediction of the PC peak energies in these devices.

The decrease of the dark current can easily be explained by the tunneling behavior of the electrons within the CB or MBs of the materials. Introducing AlAs barriers, the electrons have now to tunnel through the SL structure. Increasing the SL period leads to a decrease of the MB1 energy; thus, the relative barrier height for the electron is increased and the dark current decreases.

The suitability of the various device architectures for infrared photodetectors should be briefly discussed. In comparison with SD and DD devices, there is a clear preference for MD devices. Although SD and DD devices feature an extremely low dark current, their PC spectrum is complex, difficult to predict and of comparatively low intensity. In

contrast, the PC spectra of MD devices are characterized by an intense single peak, whose position can be designed by changing the SL parameters. Even with the crude approximation of a one-dimensional structure and the neglect of strain influences, this peak position can be calculated quite well.

Conclusion

In summary, we present an advanced method to design QD based devices by combining the self-organized growth of QD with band gap engineering. The spectral response was modified by changing the transition energy from the QD ground state to the lowest miniband of the SL. In comparison with isolated QDs, QD stacks are preferable concerning the PC intensity and the possibility to design the spectral dependence of the infrared absorption.

Acknowledgements

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Comparison of IV–VI Semiconductor Microcavity Lasers for the Mid-Infrared with Active Regions of Different Dimensionality

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A comparison between IV-VI vertical-cavity surface-emitting mid-infrared lasers containing active regions of different dimensionality is presented. Optically pumped laser emission is observed at wavelengths between 3.5 and 4.4 µm. The microcavities consist of high-reflectivity EuTe/PbEuTe Bragg mirrors, with active regions consisting of either a self-organized PbSe/PbEuTe quantum-dot superlattice, PbTe/PbEuTe multi-quantum wells or bulk-like PbTe. For the 0D active medium, laser emission is obtained at temperatures up to 150 K. The results for the lasers with 2D active region are similar to those with the 3D bulk-like active region, for which lasing is observed up to 317 K. The threshold pump intensity is only 4 kW/cm^2 at 195 K, and 15 W/cm^2 at room temperature.

Introduction

Coherent emitters for the mid-infrared range are of high interest due to various gas absorption lines in this region allowing high-resolution gas spectroscopy. For these applications, typically edge-emitting semiconductor lasers made from lead salt (IV-VI) compounds are used permitting to access emission wavelengths as long as 30 micron at cw operation temperatures as high as 223 K. Apart from the conventional edge-emitting lasers also surface-emitting lead salt microcavity lasers were recently demonstrated. The surface-emitting microcavity lasers offer several advantages over edge emitters, like small beam divergence, single mode operation, and simplified monolithic integration.

Up to now, different types of IV–VI microcavity lasers have been realized based on bulk material, quantum wells, as well as quantum dots as active regions, and with optically stimulated laser emission observed up to temperatures of 290, 340 [1], and 90 K [2], respectively. However, a direct comparison of the performance of the different types of lasers has been hindered by the fact that different cavity structures as well as different excitation sources have been used in these studies. We have done a comparison between IV–VI vertical-cavity surface-emitting lasers (VCSELs) containing active regions of different dimensionality but with a nearly identical optical design of the cavity [3]. In addition, the same optical set-up as well as pump source was used for laser excitation and characterization. This allows studying the influence of the dimensionality of the active material on the laser properties.

Design and Materials Issues

The multilayer VCSEL samples were grown by molecular beam epitaxy on (111) oriented BaF_2 substrates. The microcavity is formed by a high-reflectivity $Pb_{0.94}Eu_{0.06}Te$/EuTe Bragg mirror with only three layer pairs (bottom mirror) exhibiting a reflectivity above 99 %. This is possible due to the exceptionally high refractive index contrast of

up to 80 % between the mirror materials. In order to make the top mirror transparent for the pump wavelength of 1.907 µm, the Eu-content in the $Pb_{1-x}Eu_xTe$ layers of the top mirrors was increased to 30 %. Thus, four layer pairs have to be used to obtain a reflectivity of about 98 %.

The laser active regions consist either of highly-ordered PbSe/PbEuTe self-organized zero dimensional (0D) quantum dot superlattices [2] with 236 periods of 5 monolayers PbSe and 48 nm $Pb_{1-x}Eu_xTe$ (x = 0.05), two dimensional (2D) PbTe/PbEuTe multiquantum wells [1] with nine 20 nm wide PbTe quantum wells (QWs) embedded in $Pb_{0.94}Eu_{0.06}Te$ barrier layers, or three dimensional (3D) bulk-like PbTe with a thickness of 1115 nm grown on top of a 960 nm $Pb_{0.94}Eu_{0.06}Te$ buffer. The cavities are optimized for a wavelength of 3.7 µm, 3.5 µm or 3.3 µm, which are the spontaneous emission wavelengths of the respective active regions at room temperature.

Results

All samples were characterized by high-resolution Fourier-transform infrared transmission measurements clearly showing narrow cavity resonances with line widths between 1 and 3 meV. The VCSELs were optically pumped with 10 ns pulsed laser excitation at a wavelength of about 1.9 micron. The stimulated type of emission from the cavities is evidenced by a clear threshold behavior [3], a considerably line width narrowing with respect to the resonance line width in the transmission spectra [3] and a strongly forward directed emission profile with a divergence smaller than 1° as shown in Fig. 1.

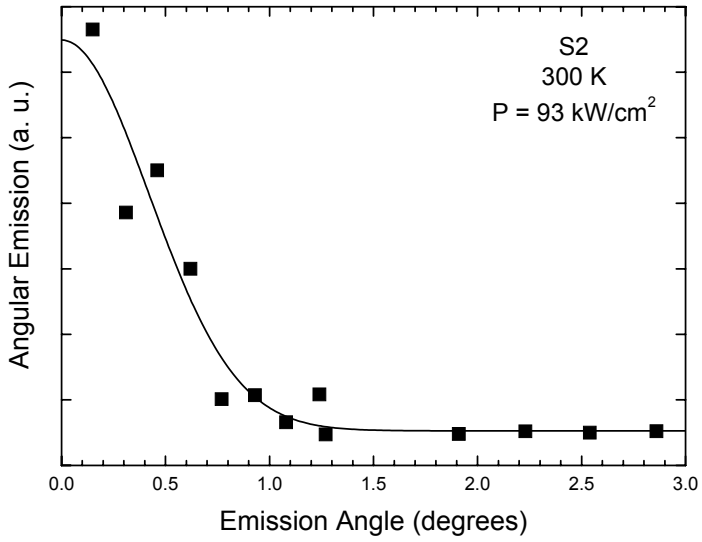

Fig. 1: Laser emission of a QW VCSEL plotted as a function of emission angle at T = 300 K evidencing the strongly forward directed emission with a divergence below 1°.

For the 0D quantum dot active medium, laser emission is obtained between 3.5 and 4 microns at several cavity resonances (due to the large cavity length) at temperatures up to 150 K [3]. The results for the lasers with 2D active regions, as shown in Fig. 2 by the temperature dependence of the laser emission, are similar to those with the 3D bulk-like active regions, for which lasing at 4.4, 3.8 and 3.6 microns is observed up to temperatures as high as 317 K (44 °C) for the 3D active zone and 307 K (34 °C) for the 2D active region. At 307 K the lower edge of the QW gain spectrum shifts out of the cavity resonance frequency and thus the laser operation is quenched as is explained in

detail in [1]. It is noted that a similar QW VCSEL with a central cavity mode at higher energy (400 meV) showed laser emission with fs-pulses up to 338 K (65 °C) [1]. The maximum emission intensity of the 3D VCSEL is of the same order of magnitude as that of the 2D VCSEL. Because the gain width in 2D systems is smaller than in 3D systems, the temperature range in which laser emission is observed is smaller for the 2D VCSEL.

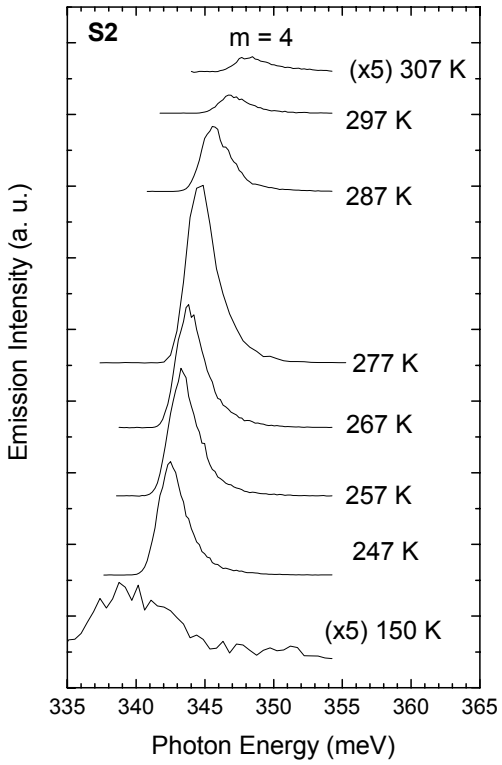

Fig. 2: Emission spectra of the QW VCSEL at various temperatures with constant pump power. The broad emission line at 150 K is due to spontaneous emission.

The threshold pump intensity is only 4 kW/cm^2 at 195 K, and 15.6 kW/cm^2 at room temperature. These values are much smaller than those reported for III-V mid-infrared VCSELs of 235 kW/cm^2 at 260 K, as well as those reported for a bulk-like PbSe VCSEL of about 70 kW/cm^2 at T = 239 K.

Conclusion

In conclusion, above-room-temperature lasing of mid-infrared IV-VI VCSELs with bulk-like PbTe as well as PbTe QWs in the active region was demonstrated up to a temperature of 320 K. The comparison of 0D, 2D and 3D systems in the active region shows that up to now the reduction of the dimensionality does not yield a laser improvement as expected from the squeezing of the wavefunctions. Bulk-like and QW VCSELs show comparable performance. This indicates that the nonradiative recombination losses due to defects are still limiting the laser process. This is obviously more important than the increase of the density of states and localization of carriers in low dimensions.

Acknowledgements

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IV-VI Semiconductors (Posters)

Molecular Beam Epitaxy of $PbSe_{1-x}Te_x$ for Strain Engineering in IV-VI Semiconductor Heterostructures

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Molecular beam epitaxy and the structural and electronic properties of ternary $PbSe_xTe_{1-x}$ layers on BaF_2 (111) for strain engineering of lattice-mismatched IV-VI semiconductor heterostructures is investigated. It is shown that although the ternary lattice constant exactly follows Vegard´s law, the energy band gap as a function of the ternary composition shows a substantial bowing behavior with a negative bowing parameter determined as –62 meV. Furthermore, the threading dislocation density in the layers is also found to depend drastically on the ternary composition due to alloy hardening that hinders the dislocation annihilation processes during strain relaxation. Nevertheless, very high quality layers are obtained for a selenium concentration of 78% for which the ternary compound is exactly lattice-matched to the BaF_2 substrate.

Introduction

The narrow band gap IV-VI semiconductors (PbSe, PbTe, PbS) have long been used for mid-infrared optoelectronic device applications [1]. These structures are usually grown on lattice-mismatched substrates such as BaF_2 or Si with appropriate fluoride buffer layers [1]. In heterostructures, band structure engineering is achieved by alloying with the wide band gap Eu or Sr chalcogenides for increasing the band gap, or with the Sn chalcogenides for reducing the band gap [1]. Because these compounds exhibit a lattice-mismatch of a few percent with respect to their lead salt counterparts, the lattice constants of the ternaries change with changing alloy composition. This can be compensated by admixtures of PbSe and PbTe, because the lattice constant of PbSeTe can be adjusted over a wide range due to the rather large difference of the PbSe and PbTe lattice constants (a_{PbTe} = 6.462Å, a_{PbSe} = 6.124Å). This can be utilized not only for achieving a lattice-matching to various substrate materials, but also for strain engineering in heterostructures as well as growth of high finesse epitaxial Bragg mirrors that are used for IV-VI compound vertical cavity surface emitting laser devices [2].

Experimental

In the present work, the growth behavior and the structural and electronic properties of $PbSe_xTe_{1-x}$ layers grown by molecular beam epitaxy onto (111) BaF_2 substrates was investigated. For this purpose a series of samples was grown at a temperature of 380 °C with ternary compositions adjusted in the range of x = 0 – 100% by controlling the flux rates from the PbTe and PbSe effusion cells. The alloy composition was determined precisely from beam flux rate measurements performed using a quartz crystal microbalance moved into the substrate position. These measurements were calibrated using several PbSe/PbSeTe and PbTe/PbSeTe superlattices in which the layer thicknesses were precisely determined by x-ray diffraction. Thus, a relative precision of the chemical composition of better than +2% could be achieved.

Results

All layers were characterized by high-resolution x-ray diffraction, Fourier transform infrared (FTIR) transmission, and atomic force microscopy (AFM) measurements. The ternary lattice constant was determined precisely from a detailed strain analysis using the asymmetric (264) Bragg reflection. In Fig. 1 (a) the resulting ternary lattice constant is plotted as a function of alloy composition. As indicated by the dashed line, it exactly follows Vegards law, i.e., corresponds exactly. The energy band gap of the ternaries was determined from the fitting of the FTIR spectra using a model dielectric function and the transfer matrix method as illustrated in the inset of Fig. 1 (b). The energy band gaps as a function of ternary composition (Fig. 1 (b)) are found to deviate significantly from a linear behavior, with only a minor change in the PbSeTe band gap as compared to the 325 meV PbTe band gap for Se concentrations up to about 50%. Above this composition, the band gap linearly decreases to the PbSe band gap of 180 meV at 300 K. This can be explained by the fact that the character of the conduction and valence bands of PbTe and PbSe are exchanged. With respect to the refractive index, a linear dependence of n versus x_{Se} was found.

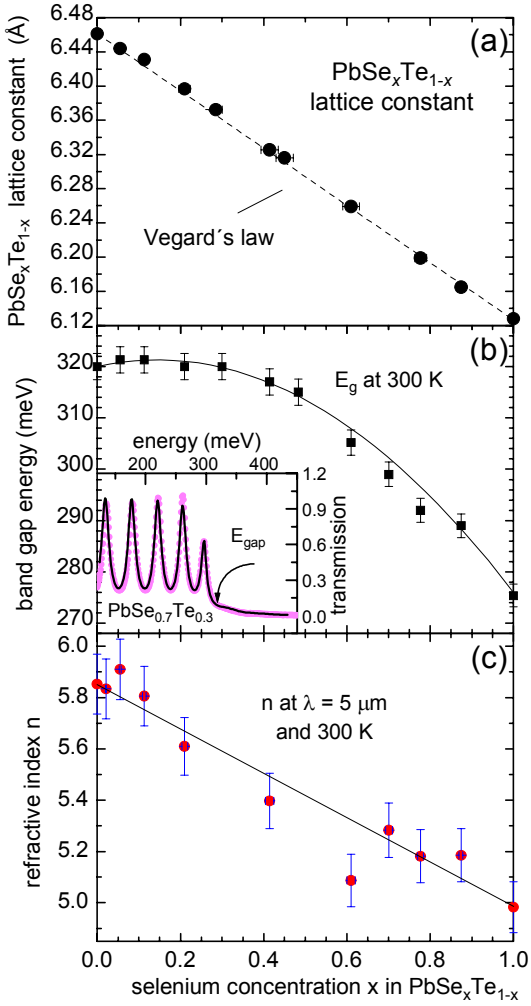

Fig. 1: (a) Lattice constant of $PbSe_xTe_{1-x}$ as a function of Se concentration. The solid line corresponds to the linear interpolation between the PbTe and PbSe bulk lattice constants (Vegard´s law). (b) Energy band gap and (c) refractive index at λ = 5 µm of $PbSe_{1-x}Te_x$ as a function of Se concentration. The insert in (b) shows the FTIR transmission spectrum of a sample with x_{se} = 70%.

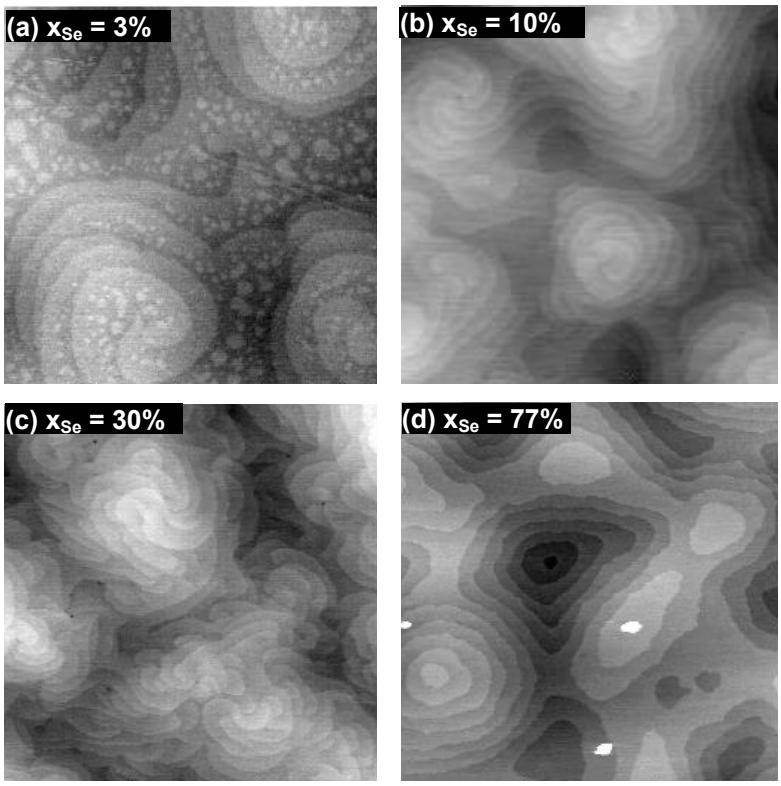

Fig. 2: Atomic force microscopy images (3 x 3 μm^2) of 3 µm $PbSe_xTe_{1-x}$ layers on BaF_2 (111) with different Se concentration.

A particularly interesting effect was observed concerning the structural properties and threading dislocation density of the layers as determined from an analysis of large-scale atomic force microscopy images as shown in Fig. 2. For the pure PbSe and PbTe layers, rather low threading dislocation densities of around 10^7 cm^{-2} were found [3] as well as narrow x-ray rocking curve widths. With increasing alloy composition, however, both parameters drastically increase reaching a maximum for Se concentrations of ~50%. This is shown in detail in Fig. 3, where the threading dislocation density evaluated from the atomic force microscopy images is plotted as a function of the selenium concentration. With increasing selenium concentration, the threading dislocation density more or less increases linearly up to values of around 2 x 10^9 cm^{-2} for selenium concentrations in the range of 20 – 60%.

At higher selenium concentrations, the dislocation density decreases again because the ternary lattice constant approaches the lattice constant of 6.200 Å of the BaF_2 substrate. This is because much less misfit dislocations are required for strain relaxation due to the resulting decrease of the layer/substrate lattice-mismatch. For a selenium concentration of 78%, the ternary layer is exactly lattice-matched to BaF_2. As a result, no dislocations are formed during deposition, and the dislocation density drops by more than two orders of magnitude below 10^5 cm^{-2}. As the selenium concentration further increases, again a lattice-mismatch to the substrate builds up, and the threading dislocation density again increases. However, as the ternary composition approaches pure PbSe, the dislocation density drops again reaching a value of around 10^7 cm^{-2} for pure PbSe. This marked behavior is attributed to a strong alloy hardening effect of the ternary layers, which prevents an efficient relaxation of the layer/substrate lattice-mismatch by glide of dislocations. Therefore, the efficient dislocation annihilation processes known, *e.g.*, for pure PbTe are kinetically suppressed in the ternary layers.

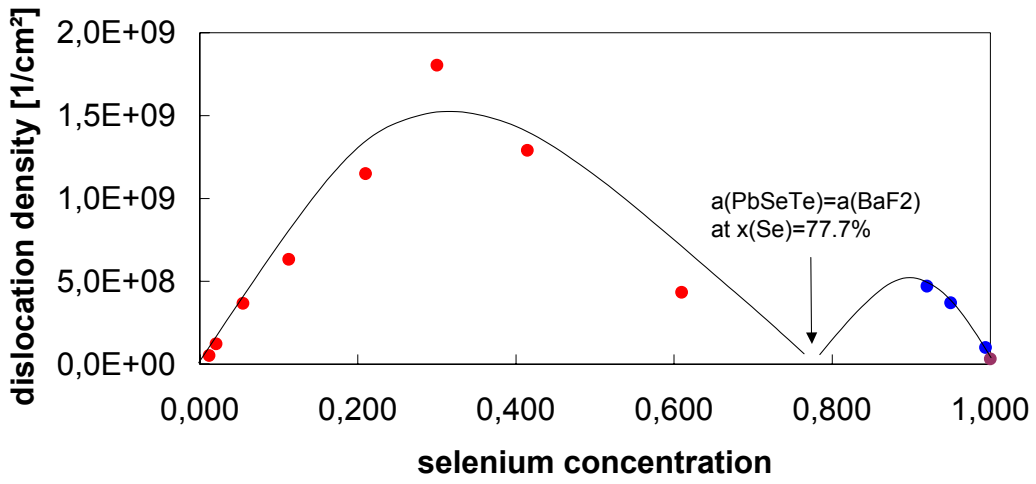

Fig. 3: Threading dislocation density of 2.7 µm $PbSe_{1-x}Te_x$ layers on BaF_2 (111) as a function of Se concentration. A minimal dislocation density is observed for x_{Se} = 78% because of the resulting layer/substrate lattice-match.

Conclusions

From investigation of ternary $PbSe_xTe_{1-x}$ layers grown by molecular beam epitaxy on BaF_2 (111) substrate it is shown that lattice constant exactly follows Vegard´s law, whereas the energy band gap as a function of the ternary composition shows a substantial bowing behavior. Although solution hardening effects in the ternary allows lead to a drastic increase of the threading dislocation density on the ternary composition, very high quality layers are obtained for a selenium concentration of 78% for which the ternary compound is exactly lattice-matched to the BaF_2 substrate. This opens promising perspectives for the growth of dislocation-free IV-VI based optoelectronic devices.

Acknowledgements

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Intermixing and Shape Transitions of PbSe Quantum Dot during Overgrowth

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The size and shape changes of self-assembled PbSe quantum dots during overgrowth by $Pb_{1-x}Eu_xTe$ barrier layers with different Eu concentrations is investigated using atomic force microscopy and in situ reflection high-energy electron diffraction. It is shown that whereas for overgrowth with pure PbTe a very strong intermixing of the PbSe dots with the cap layer material occurs, this effect is drastically suppressed with increasing Eu concentration in the $Pb_{1-x}Eu_xTe$ cap layers. As a result, the size and shape of the as-grown PbSe dot is essentially conserved during the capping process, which is important for opto-electronic device applications.

Introduction

Self-assembled semiconductor quantum dots synthesized via the Stranski-Krastanow growth mode have attracted great interest due to their excellent electronic and optical properties. For applications, quantum dots have to be embedded in a matrix material to avoid surface recombination effects. However, it is well known that *e.g.* for InAs dots embedded in GaAs there is significant intermixing between dot and matrix material [1] – [4], which leads to remarkable changes in the dot size and shape for the overgrown dots [5]. Similar effects have been also observed for SiGe dots overgrown by silicon layers, and the degree of intermixing was found to depend strongly on the growth conditions [6]. Since the optical and electronic properties depend crucially on size and shape of the embedded dots it is important to gain detailed knowledge about the changes of these parameters due to capping process.

Experimental

In the present work, we have investigated the overgrowth behaviour of self-assembled PbSe quantum dots grown by molecular beam epitaxy (MBE) on PbTe (111). The PbSe dots are formed due to strain-induced coherent islanding (–5.4 % lattice-mismatch) once the critical coverage of 1.5 PbSe monolayers (ML) is exceeded. The surface islands have a well-defined pyramidal shape with triangular base and with (100) side facets. For the overgrowth studies, a series of dot samples was prepared under identical conditions with a total PbSe thickness of 5 monolayers. Then the PbSe dots were overgrown with $Pb_{1-x}Eu_xTe$ cap material of different Eu concentration and different cap thicknesses. The evolution of the surface morphology was determined using *in situ* reflection high-energy electron diffraction (RHEED), as well as *ex situ* atomic force microscopy (AFM) under ambient conditions after rapid quenching of the partially capped samples to room temperature.

Results

In a first set of experiments, the evolution of the RHEED patterns during overgrowth of PbSe quantum dots predeposited on a PbTe buffer layer at Ts = 360 °C was investigated. Figure 1 (a) and (b) shows examples of the RHEED patterns before and after

dot overgrowth. The initial average PbSe dot height of the samples before overgrowth was 105 Å as determined from reference samples. For a more detailed analysis, the integrated intensity of the 3D (224) diffraction spot was measured as a function of cap layer thickness for several different $Pb_{1-x}Eu_xTe$ cap layer compositions as shown in Fig. 1 (c). The exact position of the (224) spot is marked in the RHEED images in (a) and (b). As is evident from Fig. 1 (c), the 3D (224) diffraction spot intensity is maximal for the initial surface with 5 ML PbSe coverage. During overgrowth, the diffraction spot rapidly decreases, and the RHEED patterns transform into the usual streaked diffraction pattern corresponding to the reformation of a planar 2D surface. This indicates that a rapid replanarization takes place in all cases. However, the cap layer thickness required for complete planarization, i.e., the thickness when the 3D spot has disappeared, strongly increases as a function of the Eu content in the ternary cap layer, indicating that the planarization process is much slower for the cap layers with higher Eu content.

Similar results were obtained from the AFM images of the partially capped samples shown in Fig. 2. In this case, the dots were overgrown with different cap layer thickness of $Pb_{1-x}Eu_xTe$, x = 0.065 and pure PbTe, respectively. In Fig. 2, left-hand side, the AFM surface images of PbSe dots overgrown with $Pb_{1-x}Eu_xTe$, x = 0.065 at cap layer thicknesses of 15 Å, 35 Å, 50 Å and 85 Å are shown for (a) – (d), respectively. At a cap thickness of 50 Å, the partially capped quantum dots are still clearly visible. For a cap thickness of 85 Å, the dots are fully overgrown although the initial dot height before overgrowth was 105 Å. This indicates that a certain intermixing between dot material and matrix material takes place and reduces the remaining dot height during capping. A closer look shows that the dots have not only vanished completely, but there are small holes on the surface, which have approximately the same density as the buried dots. From STM studies it is known that these holes are due the lattice deformations, which are caused by the highly strained buried dot.

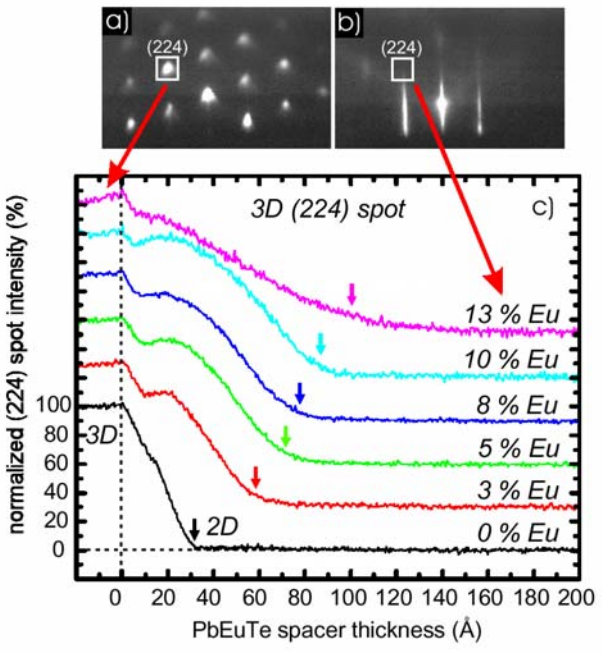

Fig. 1: Top: RHEED pattern of (a) 3D surface with PbSe quantum dots before overgrowth and (b) after complete overgrowth with $Pb_{1-x}Eu_xTe$ spacer layer. Bottom: Normalized intensity of (224) spot as a function of $Pb_{1-x}Eu_xTe$ spacer thickness for x = 0, 0.03, 0.05, 0.08, 0.1, and 0.13. Each curve has a relative offset of 20 for clarity.

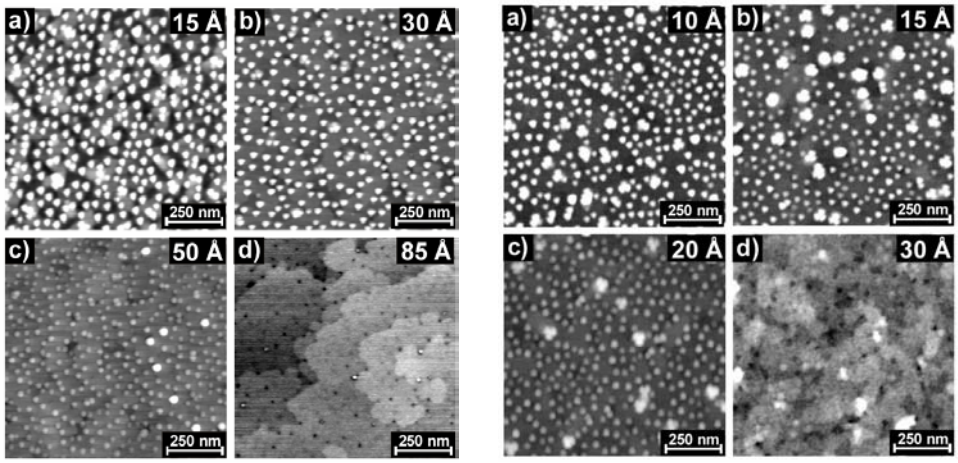

Fig. 2: Left hand side: Atomic force microscopy surface images (1 x 1 μm^2) of 5 ML PbSe quantum dot layer on PbTe buffer layer overgrown with different $Pb_{1-x}Eu_xTe$ (x = 0.065) spacer layer thickness of (a) 15 Å, (b) 35 Å, (c) 50 Å and (d) 85 Å. Right hand side: Atomic force microscopy surface images (1 x 1 μm^2) of 5 ML PbSe quantum dot layer on PbTe buffer layer overgrown with different PbTe spacer layer thicknesses of (a) 10 Å, (b) 15 Å, (c) 20 Å, and (d) 30 Å.

In Fig. 2 right-hand side (a) – (d), AFM surface images of partially overgrown dots with pure PbTe at a cap layer thickness of 10 Å, 15 Å, 20 Å, and 30 Å are shown respectively. In this case, the dots can only be detected up to a cap layer thickness of 20 Å. At 30 Å cap thickness the dots are fully overgrown, indicating that for pure PbTe the intermixing between dot material and matrix material is even more pronounced. Also for pure PbTe there are small holes detected on the surface when the dots are fully overgrown.

From the statistical evaluation of the AFM images, the remaining PbSe island height was determined as a function of the cap thickness, where the result is shown in Fig. 3. The residual dot height is plotted as a function of cap layer thickness d for x = 0, 0.03, 0.065, and 0.1. The dashed line gives the theoretical curve for the dot height, when full shape conservation is assumed and if the $Pb_{1-x}Eu_xTe$ capping material grows only around the dots and not on top. In this case the residual dot height h should be just equal to $h = h_0 - d$ with $h_0 \approx 105$ Å being the initial dot height before capping. Although, in all cases the dot height decreases essentially linearly with increasing cap thickness, the critical cap layer thickness required for planarization increases from only 30 Å for PbTe capping to about 100 Å for capping with $Pb_{1-x}Eu_xTe$ with x_{Eu} = 10%. The data obtained for x_{Eu} = 10% is remarkably close to the theoretical curve, indicating that the dot shape is almost completely conserved. For x = 0.065, there is already a clear deviation from the theoretical curve. The overgrown dots are clearly smaller than what would be expected in the case of shape conservation even for a thin cap layer thickness. It is evident that there is only little overgrowth on the top of the dots, and the intermixing at the dot base leads to further decrease in the remaining dot height. There is no evidence for discontinuities in the overgrowth and intermixing process since the measured residual dot heights follow a straight line. For x = 0.065, the dots have vanished completely after a cap layer thickness of 70 Å was deposited. For Eu contents of x = 0.03 and 0, the dots vanish already at a cap thickness of 56 and 32 Å, respectively. This indicates that while a very strong intermixing and dissolution of the initially 105 Å high dots takes place during pure PbTe overgrowth, this effect is strongly suppressed by the presence of Eu in the cap layer, *i.e.*, for sufficiently high Eu concentrations the dot shape is preserved during the overgrowth process.

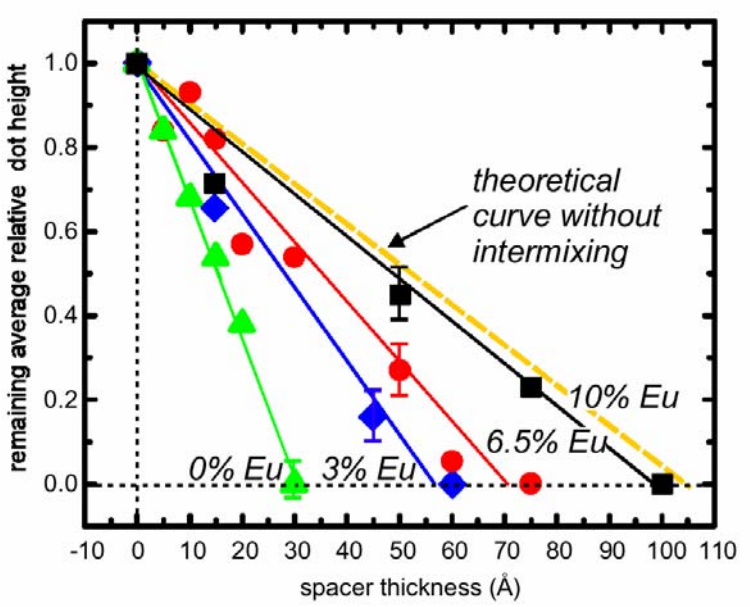

Fig. 3: Remaining average relative dot height as a function of $Pb_{1-x}Eu_xTe$ spacer thickness for different Eu contents of x=0 (▲), x=0.003 (◆), x=0.065 (●), and x=0.1 (■). The dashed curve is the theoretical curve without intermixing.

Conclusions

In conclusion, we have investigated the overgrowth behavior of self-assembled PbSe quantum dots by $Pb_{1-x}Eu_xTe$ barrier layers with different Eu concentrations. Whereas for overgrowth with pure PbTe a very strong intermixing of the PbSe dots with the cap layer material occurs, this effect is drastically suppressed with increasing Eu concentration in the $Pb_{1-x}Eu_xTe$ cap layers. As a result, in this case the size and shape of the as grown PbSe dot is essentially conserved during the capping process. This is important for optoelectronic device applications.

Acknowledgements

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Silicon and SiGe (Posters)

Transient-Enhanced Surface Diffusion on Natural-Oxide-Covered Si(001) Templates during Vacuum Annealing

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We report on the transient-enhanced shape transformation of nano-structured Si(001) surfaces upon *in vacuo* annealing at relatively low temperatures of 900 – 950 °C for a few minutes. We find dramatic surface mass transport concomitant with the development of low-energy facets on surfaces that are covered by native oxide. The enhanced surface mass transport ceases after the oxide is completely desorbed, and it is not observed on surfaces where the native oxide had been removed by HF before annealing.

Introduction

Commercial ultra-large-scale integrated circuits have reached physical gate lengths well below 100 nm, and self-organization phenomena are explored as an alternative route toward the fabrication of even smaller device structures. However, the fabrication of such small structures is only one precondition for shrinking device dimensions. It is as important to preserve their size, shape and electronic properties during subsequent device processing. Here we concentrate on the shape stability of Si nanostructures during vacuum annealing at around 900 °C for a few minutes. Such thermal steps are typically employed for native oxide desorption prior to epitaxial growth, but similar thermal budgets are frequently required during device processing, e.g. after ion implantation.

While the shape evolution of structured Si surfaces is well described [1], [2], most of the experimental studies employed long-term, high-temperature anneals. Also, quite often exotic annealing procedures (e.g. a flash to 1200 °C [3]) and direct current heating (prone to electro-migration artifacts [4]) were used. Here we employed only cleaning and annealing procedures adapted from standard Si device processes.

Experimental

Sample Preparation

Our studies were concentrated on samples consisting of periodic wire arrays of rectangular cross section fabricated by holographic lithography and subsequent reactive ion etching on Si(001) substrates (Fig. 1 (a)). Periods were varied between 400 – 2000 nm at etch depths of typically 250 nm. After photoresist stripping, the samples underwent an RCA clean with or without a final HF-dip immediately before transfer into the UHV environment of an MBE system.

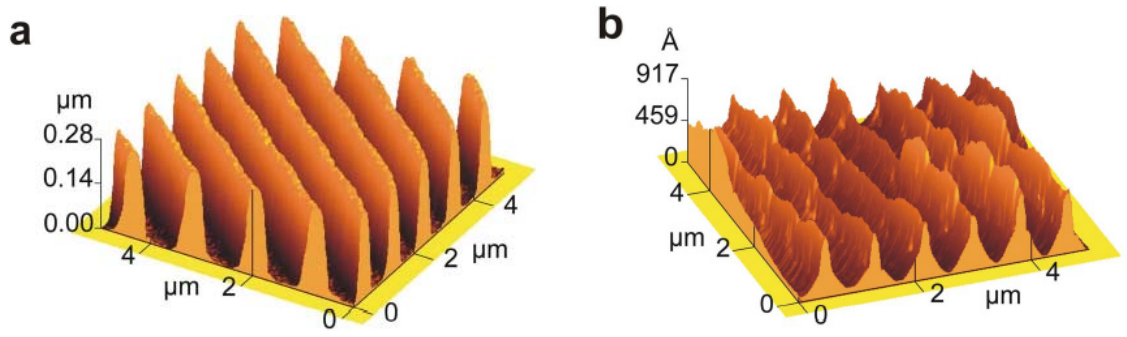

Fig. 1: 3D-AFM images of rectangular wire-template as processed (a) and after 4 min annealing @ 950°C without previous HF-dip (b).

Measurements

In the UHV environment of the MBE system the samples were radiatively annealed for 1 – 5 min at 900 – 950 °C, which corresponds to the standard oxide desorption step prior to epitaxial growth [5], [6]. On all samples covered by native oxide the originally rectangular profiles were transformed into {311}-faceted trapezoids concomitant with a loss of up to 80% of the peak-to-valley modulation (Figs. 1 (b), 2 “RCA”). In contrast, samples that had the native oxide removed by HF showed no significant morphological changes (Fig. 2 “HF”).

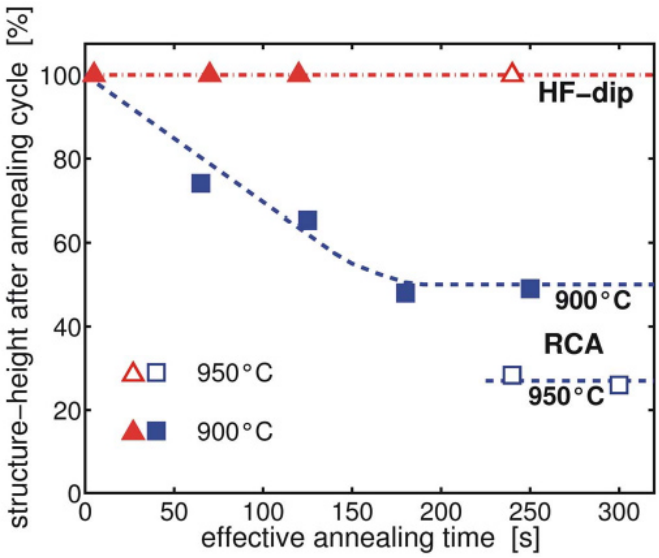

Fig. 2: Reduction of structure-height after different annealing cycles.

We followed the kinetics of faceting as a function of the annealing conditions by high-resolution XTEM imaging (Fig. 3), and compared the results to Monte-Carlo-type simulations that used the surface energies of the {111} and {311} facets as the only input parameters. We found good agreement, which is indicative of a shape transformation that behaves as expected near thermal equilibrium [1], [7], despite the fact that our experiments were conducted 500 °C below the melting point of Si.

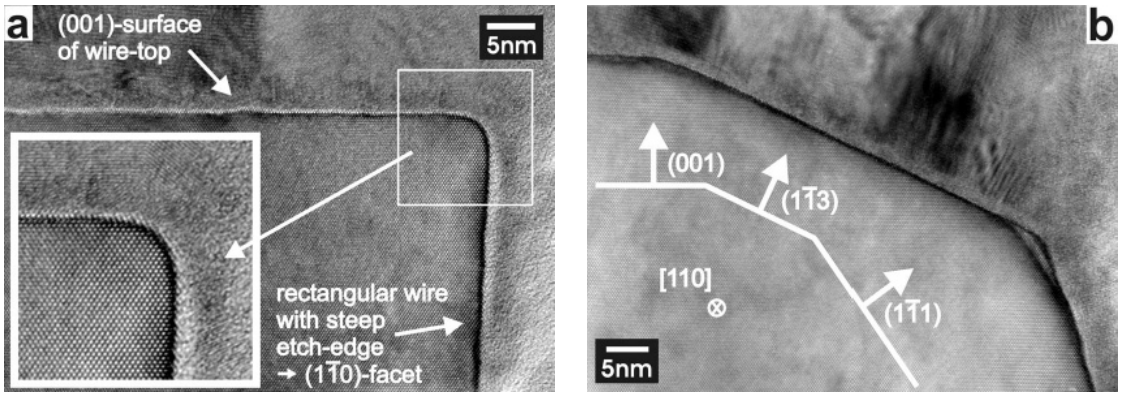

Fig. 3: High-resolution XTEM-images of rectangular and faceted wire-edges, as processed (a) and after 2 min annealing @ 900°C without previous HF-dip (b).

Since only oxide-covered structures reveal the transient enhanced shape transformation, the reaction [8] Si + $SiO_2 \rightarrow SiO\uparrow$, on which thermal oxide desorption at 900 °C is based, is most likely involved in this phenomena. This reaction takes place everywhere at the Si/SiO_2 interface, but it has been found that the oxide desorption reaction occurs mainly at the periphery of voids, which form in the early stages of thermal decomposition in the oxide layer [9]. No correlations between void nucleation and shallow structures at the Si surface have been found yet. However, it is not clear, whether this applies to our nanostructures, which provide almost atomically sharp intersections between two low-index planes (Fig. 3 (a)).

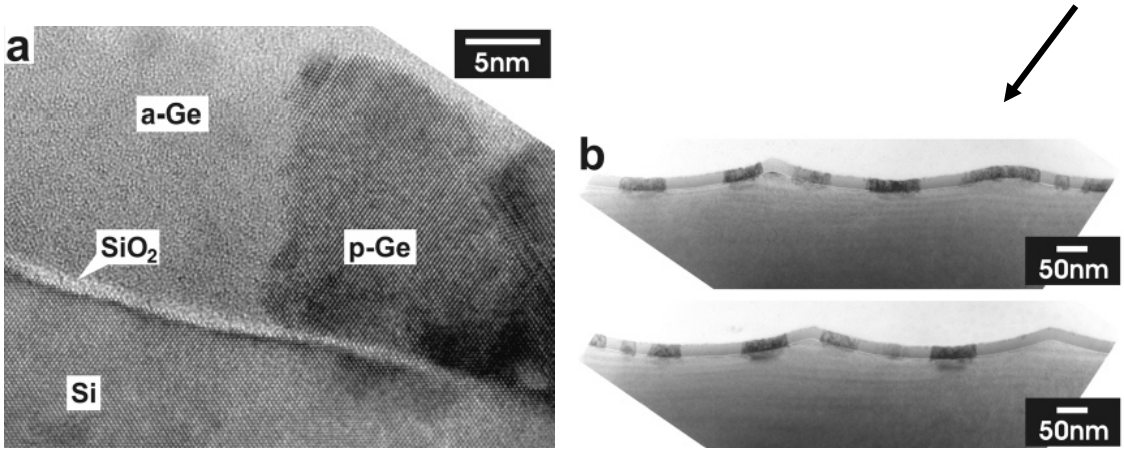

Fig. 4: (a) High-resolution XTEM-image of wire-template with a period of 400 nm after 1 min annealing @ 900 °C with posterior Ge-overgrowth at temperatures below 175 °C. On the SiO_2 covered Si structure amorphous Ge is formed, whereas polycrystalline Ge indicates regions of oxide-desorbed surface parts.
(b) Low resolution TEM images indicate that oxide break-up shows no correlation with the wire template.

In order to distinguish whether the shape transformation is linked to void formation or occurs beneath a still existing layer of oxide, we have developed an XTEM decoration technique. Covering annealed (1 min @ 900 °C) wire templates in situ with low temperature Ge leads to poly-Ge growing in the substrate-exposing voids, and to amorphous Ge on areas that are still covered by native oxide (Fig. 4 (a)). The p-Ge areas can easily be identified in XTEM images because the strain contrast makes them ap-

pear darker (Fig. 4 (b)). In addition, the mass contrast allows a straightforward identification of the SiO_2 layer, which appears as alight stripe.

Figure 4 (b) shows that no correlation whatsoever exists between void formation and the template structure: Most of the remnants of the wires are still buried underneath a continuous SiO_2 film. That means, the shape transformation takes place predominantly below the oxide, and the oxide follows this transformation. The voids do have some influence: The one ridge structure that accidentally coincides with a void in the oxide (arrow in Fig. 4) appears even flatter than the oxide-covered ridges. This effect is most likely responsible for the roughness overall in Fig. 1 (b).

Conclusion

Shrinking the dimensions of semiconductor devices structures to the nanometer range, the preparation and conservation of small morphological features becomes increasingly relevant. The surface free energy of a structured heterosystem is determined by composition, crystal orientation, and strain. The interplay between these parameters is widely exploited for the fabrication of self-organized nanostructures. Pre-patterned substrates can enhance ordering of these sub-micron structures. Here we report on the morphological integrity of such templates under chemical and thermal treatments typically employed during device processing. The results show that even proven and supposedly uncritical process steps can drastically affect the morphology of nanostructures.

Acknowledgements

We thank C. Schelling for his input during the early stages of this study, and A. Halilovic and G. Hesser for template and XTEM preparation, respectively. TEM work was performed at the Technical Services Unit (TSE) of the Johannes Kepler University. This work was financially supported by GMe and FWF (P12143PHY).

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Growth Instabilities in Si/SiGe Homo- and Heteroepitaxy

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We show that for a large set of growth parameters the reason for ripple formation in the Si/SiGe system is the kinetic step-bunching instability found in Si homoepitaxy. Single $Si_{1-x}Ge_x$ layers (with x around 0.5) do not show step-bunching. In superlattices, the instability has a similar behavior as the instability in homoepitaxy. Mainly the growth temperature influences the surface morphology; only little changes can be found when the germanium content in the superlattices is changed. In addition, the increase of ripple height and period with increasing amount of deposited silicon is similar to the one found in homoepitaxy. The more germanium is present in the superlattice the less pronounced the step-bunches appear. In kinetic Monte-Carlo simulations we show that only the interplay between diffusion anisotropy on the (2×1) reconstructed Si(001) surface and the attachment/detachment of adatoms on the step-edges is responsible for the growth instability in Si homoepitaxy.

Introduction

The Si(001) surface is the technologically most important surface for the semiconductor industry. The step-bunching growth instability on vicinal Si(001) is single $Si_{1-x}Ge_x$ layers and Si/SiGe superlattices was often believed to be strain-induced [1]. In fact, it has been found that a step-bunching instability resulting in an indistinguishable surface morphology appears already in Si homoepitaxy [2], where no strain is present.

Experiments

Single SiGe layers and Si/SiGe superlattices (SLs) have been grown by solid source molecular beam epitaxy (MBE) on RCA-cleaned substrates with a miscut of 0.66° in [110] direction to investigate the influence of germanium.

Single $Si_{1-x}Ge_x$ layers (with x around 0.5) do not show step bunching. They replicate the morphology of the underlying buffer layer, which can be chosen as flat or rippled by selecting proper growth conditions. These layers disintegrate into hut-clusters when allowed to reach thermodynamic equilibrium [3].

In superlattices the instability has a similar behavior as the instability in homoepitaxy. When miscut (0.66°) and growth rate (0.2 Å/s) are kept constant, mainly the growth temperature influences the surface morphology, only little changes can be found when the germanium content in the superlattices is changed (see Fig. 1). In addition, the increase of ripple height and period with increasing amount of deposited silicon is similar to the one found in homoepitaxy. Both follow a $y=a \cdot x^b$ type law, with critical exponents of 0.5 and 0.25 respectively. The more germanium is present in the superlattice the less pronounced the step-bunches appear. We attribute this slight decrease with in-

creasing germanium content to changes in surface kinetics, which are due to the segregation of germanium [4].

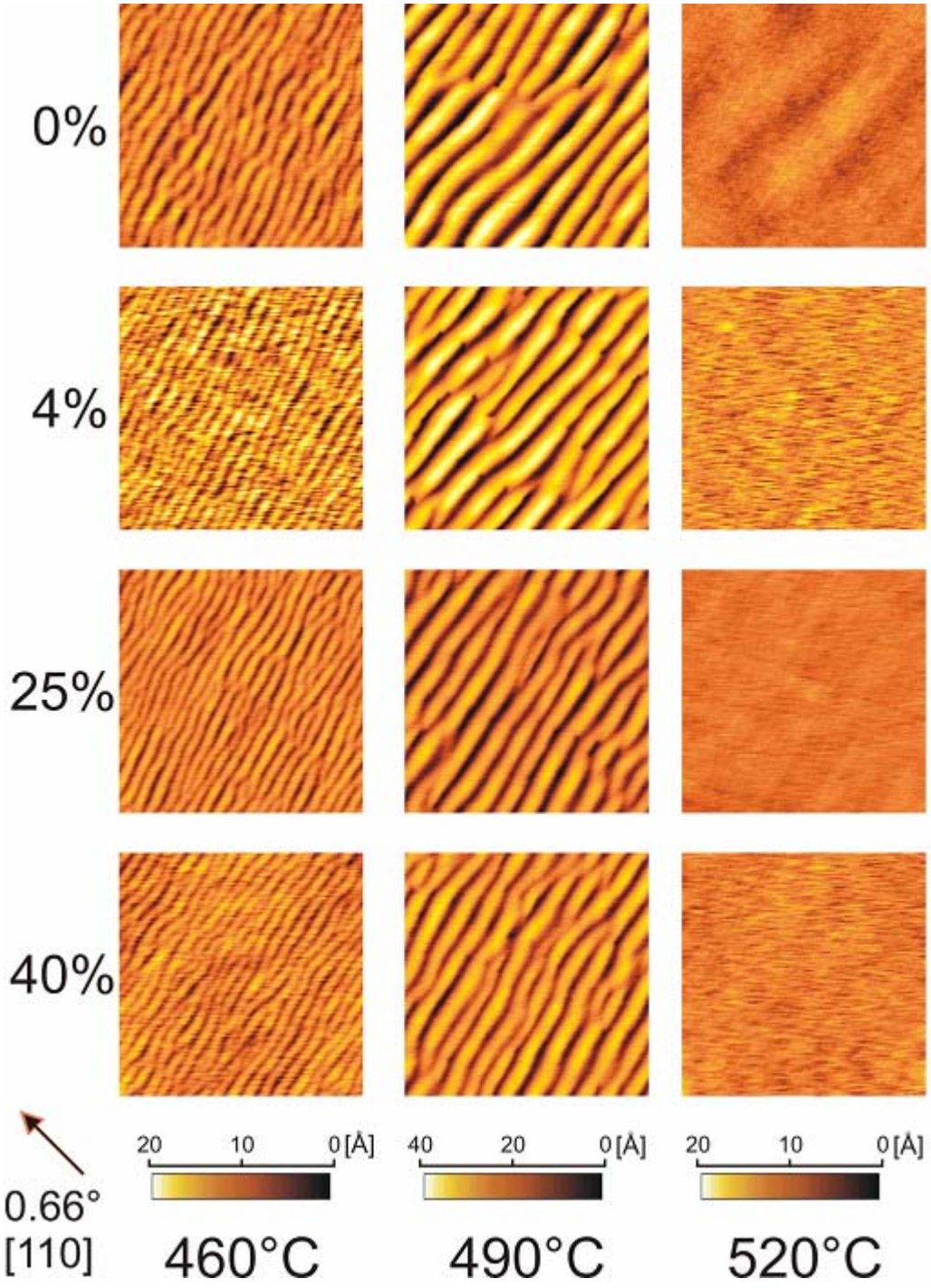

Fig. 1: AFM images of 10× [30Å Si / 300 Å $Si_{1-x}Ge_x$] superlattices grown at various growth temperatures (indicated on the bottom) and Ge-contents (indicated on the left). The miscut direction is given by the arrow on the lower left side. All images are 5×5 µm² in size.

Kinetic Monte-Carlo Simulations

In two-dimensional kinetic Monte-Carlo simulations, we show that growth kinetics is the mechanism, which is relevant for the step bunching. In Si homoepitaxy only the interplay between the diffusion anisotropy on the (2×1) reconstructed Si(001) surface and the attachment/detachment of adatoms on the different S_A and S_B step-edges is responsible for the growth instability in Si homoepitaxy. No step-edge barriers are necessary to explain the experimentally observed morphology [5]. Figure 2 shows images illustrating the time evolution of the sample surface during the simulation.

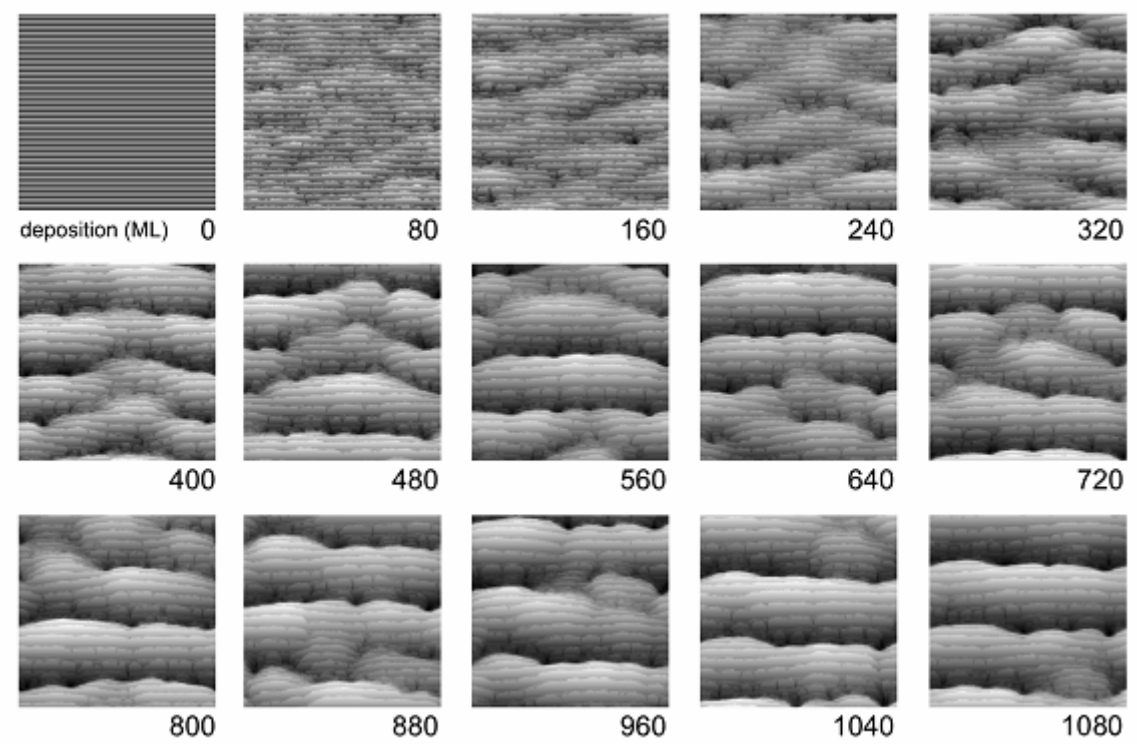

Fig. 2: Results of the two-dimensional kinetic Monte Carlo simulation showing the evolution of the surface. The number of deposited monolayers (MLs) is given for each image.

Conclusion

In conclusion, we show that for a large set of parameters strain-induced step bunching can be excluded with high probability and that the reason for ripple formation in the Si/SiGe system is only the kinetic step bunching instability found in Si homoepitaxy. We find that germanium slightly influences the step bunching in Si due to its segregation but not due to the strain introduced because of the lattice mismatch. Two-dimensional kinetic Monte Carlo simulations give close insight in the atomic mechanisms responsible for this phenomenon.

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High-Mobility Strained Si for Spintronics Applications

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We have grown modulation-doped $Si_{1-x}Ge_x$ quantum wells ($0 \leq x \leq 0.1$) on relaxed $Si_{1-xs}Ge_{xs}$ buffer layers, and have investigated this system using conduction electron spin resonance (CESR) and conventional Hall measurements. For a pure Si channel, mobilities of up to 341 000 cm²/Vs at carrier densities of $2.8 \cdot 10^{11}$ cm^{-2} were found in Hall measurements under illumination at 1.6 K. In CESR, extremely narrow line widths of down to 40 mG can be observed. In pulsed-ESR experiments, spin lifetimes T_1 and T_2 in the order of microseconds have been found. This is two orders of magnitude longer than the length of the microwave pulses used to flip the spins. The g-factor for the electrons in Si (g = 1.998) and Ge (g = 1.563) is significantly different. We grew samples with $Si_{1-x}Ge_x$ quantum wells with x = 0.05 and x = 0.1. In these samples, a clear shift of the g-factor could be observed although in this first attempt the line width of the CESR signal was significantly increased.

Introduction

Electrons in silicon are very promising for spintronics and quantum information processing. The main reasons are the extremely long spin lifetimes, which are due to silicon's weak spin-orbit coupling, and the suitability of this material system for very large scale integration (VLSI). Especially the spin properties of two-dimensional electron gases (2DEGs) in the Si/SiGe heterosystem have attracted considerable interest recently. [1]

For a quantum computer [2] it would be useful to change the g-factor and therefore the position of the resonance in an electron spin resonance (ESR) experiment. This can be accomplished by using the fact that the g-factor for the electrons in Si (g = 1.998) and Ge (g = 1.563) is significantly different.

Experiments

We have grown modulation-doped $Si_{1-x}Ge_x$ quantum wells ($0 \leq x \leq 0.1$) on relaxed $Si_{1-xs}Ge_{xs}$ buffer layers with $0.20 < x_s < 0.3$. The properties of the two-dimensional electron gases (2DEGs) have been investigated using conduction electron spin resonance (CESR) and conventional Hall measurements.

Growth was performed by solid source molecular beam epitaxy (MBE), and doping with Sb was done at the low growth temperature of 300 °C to suppress the strong segregation. On top of a relaxed buffer layer (3.4 µm linear grading + 0.6 µm constant composition part) the strained $Si_{1-x}Ge_x$ channel was deposited, followed by an undoped spacer layer, the doping layer, and $Si_{1-x}Ge_x$ and Si cap layers.

Results

For a pure Si channel, mobilities of up to 341 000 cm²/Vs at carrier densities of $2.8 \cdot 10^{11}$ cm^{-2} were found in Hall measurements under illumination at 1.6 K (see Fig. 1). In CESR, extremely narrow apparent line widths of down to 40 mG can be observed (see Fig 2).

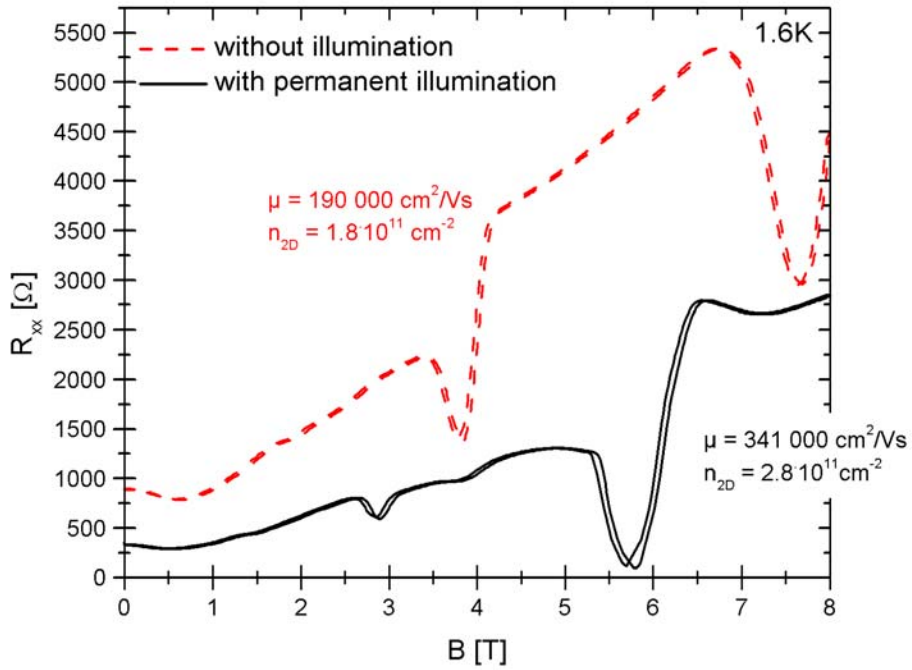

Fig. 1: SdH measured at 1.6 K with (solid line) and without permanent illumination.

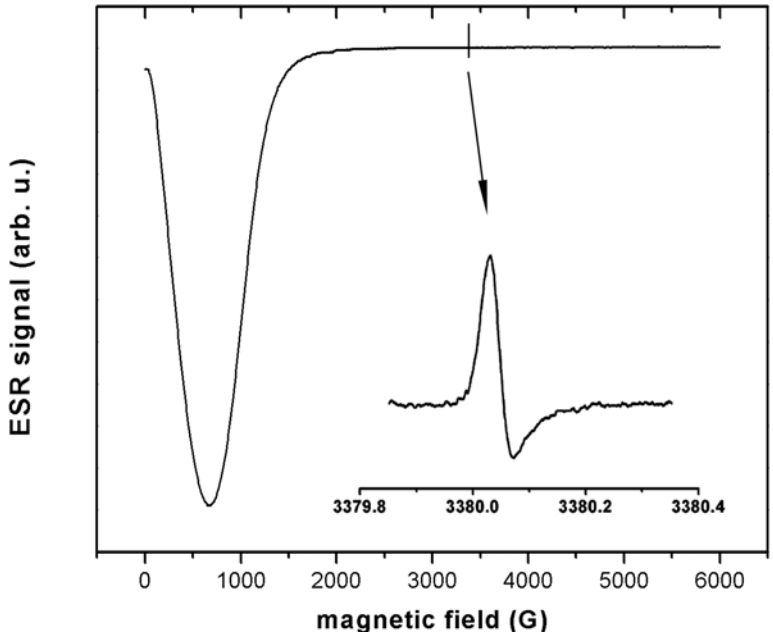

Fig. 2: Cyclotron resonance and CESR signal (inset) measured at 2.5 K. The line width of the CESR signal is only 40 mG.

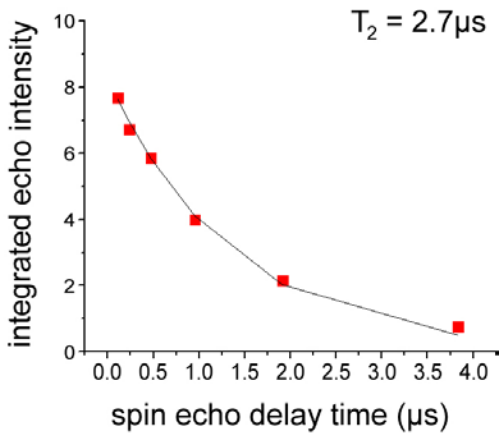

Fig. 3: Determination of T_2 from spin echo experiments [4].

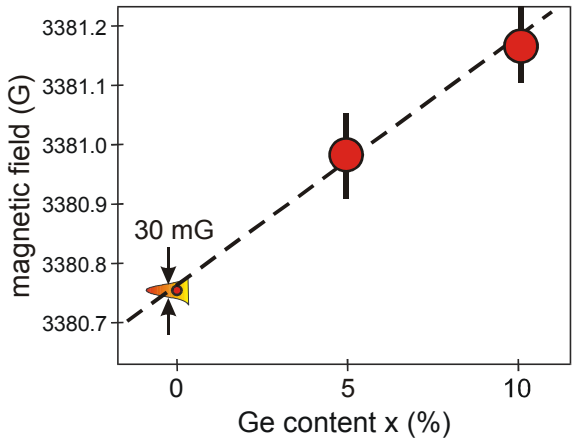

Fig. 4: Change of g-factor of the two-dimensional conduction electrons as a function of Ge-content in the quantum well.

In pulsed-ESR (spin echo) experiments in a comparable sample [3], it was found that the spin-lifetime T_1 (longitudinal relaxation time) and the phase memory time T_2 (transverse time) are both in the order of microseconds (see Fig. 3) [4]. This is two orders of magnitude longer than the length of the microwave pulses used to flip the spins. A typical π-pulse, which flips a spin by 180°, is 10 ns long. Consequently, many coherent spin operations are possible.

The g-factor for the electrons in Si (g = 1.998) and Ge (g = 1.563) is significantly different. Since for a quantum computer [2] it would be useful to change the g-factor and therefore the position of the resonance in a CESR experiment, we grew samples with $Si_{1-x}Ge_x$ quantum wells for the electrons with x = 0.05 and x = 0.1. In these samples, a clear shift of the g-factor could be observed (see Fig. 4), although in this first attempt the line width of the CESR signal was significantly increased.

Conclusion

We have demonstrated the growth of high mobility modulation-doped Si quantum wells with spin lifetimes in the range of microseconds. Furthermore, first steps towards the manipulation of these spins have been made with promising results.

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Laterally Ordered Ge Islands on the Pre-Patterned Si (001) Substrates

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Ge islands were grown on the pre-patterned Si (001) substrates by solid-source molecular beam epitaxy. The topographies of the islands samples, obtained by atomic force microscopy (AFM), demonstrated that Ge islands tend to grow in the trenches or in the holes on one- or two-dimensionally patterned substrates, respectively. Provided the periodicities of the trenches or the holes originated from the pre-patterns, laterally ordered Ge islands were obtained. The preferential positioning of Ge islands in the trench or in the holes is attributed to a net flux of ad-dimers (or ad-atoms) downwards at the sidewalls, which is related to the growth temperature and the growth rate.

Introduction

Several authors reported the combination of pre-patterning of substrates with self-organized growth to achieve long range ordering of self-assembled islands [1] – [6]. For the growth of Ge islands on (001) Si substrates, so far for their preferential positioning, mainly lithographically defined patterned oxide features have been used. In this fabrication method, the Ge islands are grown preferentially at the edge of the stripes or mesas selectively grown in pre-patterned and etched SiO_2 windows [1] – [4]. By adjusting the size of the SiO_2 windows, a controlled arrangement of the Ge islands could be realized. This local epitaxy works particularly well if gas source (GS) molecular beam epitaxy (MBE) or chemical vapor deposition (CVD) processes are used. However, the remaining SiO_2 layer induces external strain and furthermore complicates the subsequent processes to characterize the properties of Ge islands or to fabricate devices. In this presentation, we show results of ordered Ge islands grown on pre-patterned (one- or two-dimensional (1D or 2D) Si (001) substrates. Our observations demonstrate that the growth kinetics significantly affect the positioning of Ge islands on the pre-patterned substrates without use of SiO_2 windows. In particular, 1D and 2D ordered Ge islands can be realized on these pre-patterned Si (001) substrates.

Experiments

The pre-patterned substrates were fabricated by holographic lithography and reactive ion etching. The orientation of the stripes and the square pattern was chosen to be along <110> directions. Patterns with a periodicity of less or equal than 0.5 µm and a depth of about 50 nm are used. All samples were grown by solid-source MBE. The substrates were cleaned by an RCA cleaning process followed by a HF dip to form hydrogenated surfaces. After desorption of the oxide layer at 900 °C, a Si buffer layer (about 100 nm thick) was deposited at a growth rate of 0.5 Å/s while the growth temperature was ramped from 550 °C to 650 °C. For samples grown on a 1D stripe-patterned substrate, seven monolayers (ML) Ge were then deposited at 650 °C. For the sample grown on a 2D square pattered substrate, 6ML Ge were deposited at 700 °C. For the Ge island growth, a growth rate of 0.04 Å/s was used. We also investigated samples with a stack of three Ge island layers separated by 20 nm Si spacer

layers. In these samples, the upper two Ge islands layers were grown at 650 °C with only 5.7 ML Ge deposition, in order to avoid an increase of the island size. To reduce Ge-Si intermixing, the Si spacer layer was grown at 550 °C. The rather high substrate temperatures for the Ge island growth were chosen to enhance Ge adatom diffusion, which in conjunction with the low growth rates enabled us to achieve the desired ordering. The surface morphology of these samples was investigated after growth in air using a Park Scientific atomic force microscope (AFM).

Results

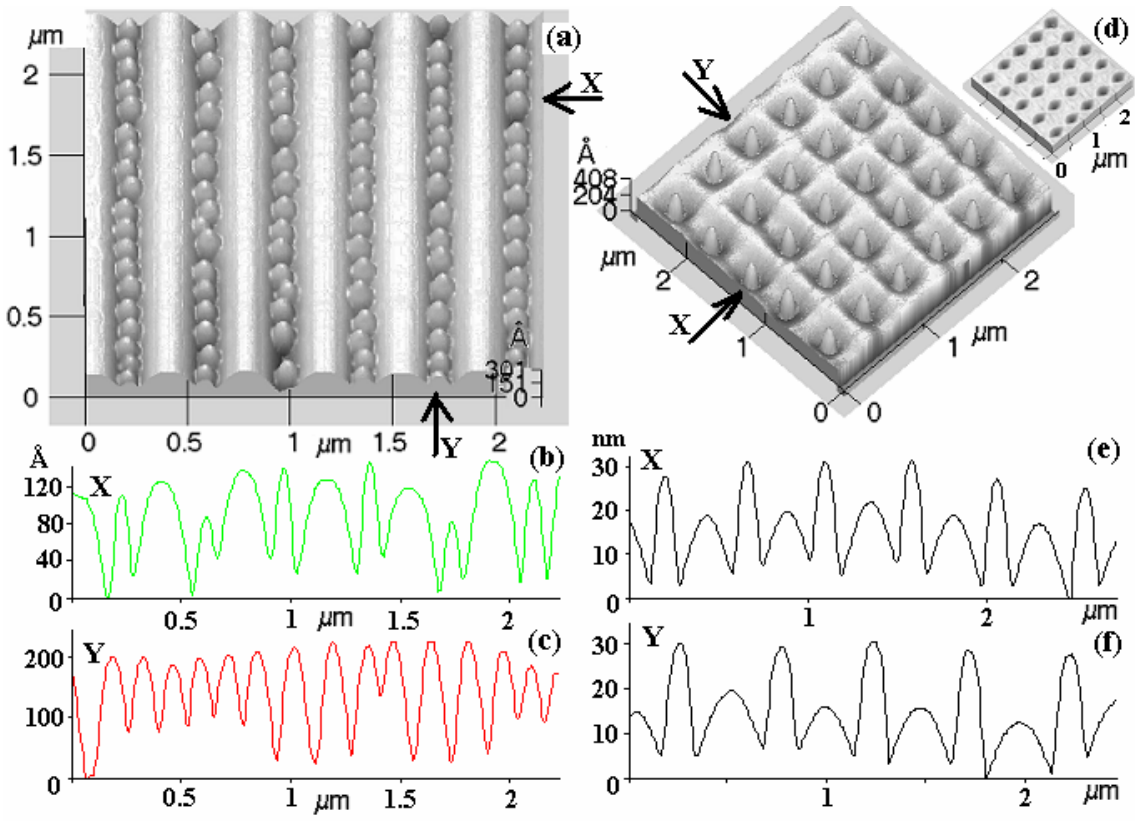

Fig. 1: AFM micrographs of 1D (a) and 2D ordered Ge islands (d), with corresponding line scans (b, c) and (e, f).

The 2D or 3D AFM images of samples A and B are shown in Figs. 1 (a), (b) and (c), respectively. For sample A, which was grown on a 1D patterned substrate, we observe an ordering of the islands along the trenches with a lateral period of 40 nm. In addition, height profiles are shown. Along the trenches (Fig. 1 (b)) and perpendicular to it (Fig. 1 (c)), we observe long range ordering of dome-shaped islands not only for the “one dimensional” sample A but also for the “two-dimensional” sample B. For the square patterned substrate, the Ge islands nucleate in the holes formed by the orthogonally etched trenches and *not* on top of the mesas. This observation differs from previously reported gas source MBE growth of islands on etched mesas [2], [3]. Figures 1 (e) and (f) show line scans, i.e. height profiles of the 2D ordered islands along two orthogonal directions. These line scans reveal both the achieved precision of the two- dimensional lateral positioning as well as size uniformity of the islands.

The nearly perfect lateral ordering of the islands can be used to stack several layers of Ge islands to form a three dimensional island crystal. We chose a Si spacer layer

thickness of 20 nm, which ensures a vertical ordering of the islands, due to the strain fields of the buried ones. Figure 2 shows the surface morphology of samples C and D which consist of a stack of three Ge island layers separated by Si spacer layers, which were grown at 550 °C, These AFM data nicely demonstrate the long range ordering and size homogeneity of the Ge islands. The line scans along two orthogonal <110> directions not only demonstrate the periodicity and the size homogeneity but also the fact that in the stacked island samples the regions in between the islands are flattened through the coverage with Si.

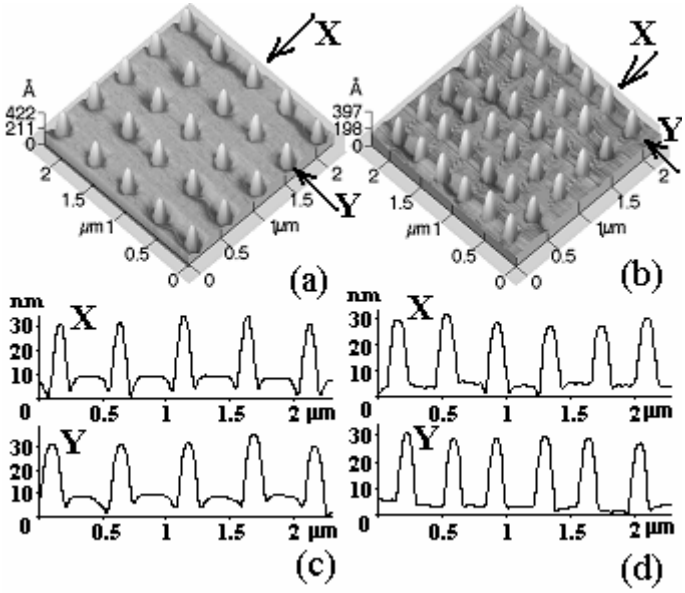

Fig. 2: Surface morphology of three period stacked Ge island samples with a lateral period of 500 nm (sample C, (a)) and 400 nm (sample D, (b)). Line scans along two orthogonal <110> directions marked by X and Y are shown in (c) (sample C) and (d) (sample D).

In samples that were capped with Si we investigated also the photoluminescence (PL). Clear PL signatures both from the islands as well as from the wetting layers were found.

Conclusions

In conclusion, we have demonstrated two-dimensional lateral ordering of Ge islands on pre-patterned Si substrates without the use of patterned oxide layers or of buried stressor layers.

We explain our observations of this two-dimensional ordering by the importance of the growth kinetics of Ge on Si, which primarily affects the preferential positioning of Ge islands on the pre-patterned Si substrates. The formation of Ge islands in the trenches or in these holes is attributed to the accumulation of Ge adatoms migrating downwards from the sidewalls of trenches or holes or even from the neighboring mesas to the bottom. The reason for this downward flux of adatoms is an asymmetry of the activation barrier at steps [7]. The Ge atoms that remain on top of the ridges or mesas form a Ge layer with a thickness less than the critical value for 2D-3D transition, resulting in the absence of islands. This kinetic origin of island formation in trenches or holes agrees with our previous results on the formation of Ge islands on 1D pre-patterned stripes [7].

The growth technique described makes a precise addressing of individual islands possible, a prerequisite for any application of these self-organized Ge nanostructures in electronic or optoelectronic applications.

Acknowledgements

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Direct Write Processes (Posters)

Scanning Capacitance Microscopy Investigations of Focused Ion Beam Damage in Silicon

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In this article, we explore the application of Scanning Capacitance Microscopy (SCM) for studying focused ion beam (FIB) induced damage in silicon. We qualitatively determine the technologically important beam shape by measuring the SCM image of FIB processed implantation spots and by comparison of topographical and SCM data. Further, we investigate the question how deep impinging ions generate measurable damage below the silicon surface. For this purpose, trenches were manufactured using FIB and analyzed by SCM in cross sectional geometry.

Introduction

Focused ion beam (FIB) techniques are among the most important tools for modification tasks below 100 nanometer. Today, FIB systems are mainly used for device modification, transmission electron microscopy (TEM) sample preparation, scanning probe microscopy (SPM) tip preparation, and deposition of different metals and insulators [1]. Unfortunately, there are mainly two effects that limit the usage of FIB modification to certain applications and areal scales [2]. Difficult to measure, the ion beam diameter and intensity profile defines the lateral resolution and the smallest possible size of a FIB made structure. The other limitation occurs due to ion beam induced damage, which extends far below the modified sample surface.

Various methods such as secondary ion mass spectroscopy (SIMS) and transmission electron microscopy (TEM) have been utilized to measure penetration depths and intensity profiles of FIBs. However, the disadvantage of these methods is their lack of 2D spatial resolution (SIMS) or difficult sample preparation (TEM). For this reason, scanning probe techniques have successfully been applied for FIB intensity profile determination and imaging in other ion beam applications [3]. Topographic atomic force microscopy (AFM) investigations can yield high resolution data from FIB implanted spots via the embossment of FIB amorphisized areas due to the slightly lower density of amorphous silicon compared to crystalline silicon. However, severe degradation of the electronic properties will occur long before the structural changes (amorphization) take place, which cannot be investigated any more with topographic AFM. In this article, we introduce Scanning Capacitance Microscopy (SCM) as a very sensitive tool to investigate the position and extent of FIB induced electronic degradation. SCM is an extension of conventional AFM and a very promising tool for semiconductor device characterization. The current state of the art of this technique can be found in the review article [4]. SCM can detect magnitudes smaller changes in material composition than any other scanning probe method and it is possible to sense as small quantities as 10 – 100 impurity atoms per cubic micron (10^{13} – 10^{14} per cm^3). Where FIB irradiation does not alter the topography of the region of interest, it is still possible to get reliable data of the FIB damaged areas via SCM. We first use this method to determine the ion beam intensity profile by investigating irradiated silicon surfaces. Then we will deal with the damage spread inside the silicon sample beneath a FIB milled trench.

Experimental

To avoid any additional difficulties in data interpretation due to the very complex electrical behavior of pn-junctions [5] we decided to use low p-doped silicon wafers, since our FIB system is equipped with a Ga^+ ion source (acceptors). The low acceptor concentration of the bulk material was an advantage, because SCM yields higher signals on low-doped semiconductors. The samples were prepared in two ways to match the different demands of FIB intensity profile and damage depth determination: For measuring the beam intensity profile, we used the very clean surfaces of freshly cleaved silicon wafers. On the cleaved surface five types of spots were made with the FIB system, which differed from each other in the deposited ion dose (0.025, 0.05, 0.1, 0.5 and 5 pC/spot). The spots were located in close vicinity (a few microns) of the wafer edge to reduce sample tip-holder overlaps and related stray capacitance, which increases the signal to noise ratio in our SCM measurements. The acceleration voltage of the Ga^+ ions was 50 kV and the aperture size was 50 µm. For the investigation of the damage depths, a trench was milled into the polished front side of a wafer. After milling, the sample was cleaved to get cross sections of the damaged area beneath the trench.

Results and Discussion

Although the SCM signal is a complicated function of the semiconductor doping concentration and the applied tip-bias voltage, it is possible to adjust the electrical parameters of the setup in a way to gain a signal that is monotonic with doping concentration [6]. Using such optimized conditions leads to good SCM contrast with big signal in low-doped regions and small signal in higher doped regions. However, besides the p-type doping by Ga^+ ion implantation, the crystalline structure of FIB irradiated samples is damaged heavily which also results in a reduction of the SCM signal. Therefore, we cannot distinguish between high doped or damaged areas. Studies show that ion beam doses magnitudes smaller than the minimum dose for surface modification (e.g. swelling due to amorphization) can already be detected via SCM. We used this fact to determine the beam intensity profile of our FIB system. Figure 1 (a) shows the resulting topographic changes of milling with a moderate dose per spot (0.5 pC/spot). The swelling and subsequent silicon removal due to sputtering can be seen very well and leads to the typical crater-like structures. Figure 1 (b) shows the simultaneously measured SCM picture. In comparison with the topographic image seen in Fig. 1 (a), the recorded SCM picture shows a significantly larger damaged region indicated by the dark circle of low SCM signal. Based on topography, we define the ion beam radius as follows: the radius R_{Topo} is the distance from the deepest milled point (highest intensity in the beam center) to the point where the outer swelling flank is half-decayed. In the case where the ion dose is so small that only swelling is observed, we take the distance between the maximum of the swelling and the point where it is half-decayed. Based on SCM we defined the beam radius R_{SCM} as half the distance between the points where the SCM-signal-flanks rise to half of their maximum.

The two radii R_{Topo} and R_{SCM} are compared in Fig. 1 (c), where cross sections of the image data are plotted along line L. The difference between topography signal and SCM signal, $\Delta R = R_{SCM} - R_{Topo}$, is 250 nm. Figure 1 (d) compares the behavior of the radii R_{Topo} and R_{SCM} with increasing dose per spot. The radii show monotonic growth, however, there are saturation effects in the high dose regime. In addition, both data sets diverge for big ion doses. Whereas for the lowest dose the structures have twice the radius in SCM mode than in topography mode, for the highest dose this ratio is almost four. Our observation that the SCM based beam radius R_{SCM} is always larger than the topographic radius R_{Topo}, and the effect that R_{Topo} and R_{SCM} diverge for big ion doses, can be explained by the following facts. First, as was already published [1], [7], the beam profile consists of (at least) two regions: The region far away from the beam

center, where the overall intensity is very small but decays slowly. The other region is close to the beam center, where the intensity is comparable with the beam center and has the steepest decay. Second, SCM is much more sensitive to ion irradiation effects than the topographic signal, since topographic changes by amorphization need very high ion doses. Because of these two properties, the SCM sensed radius grows quickly with increasing dose per spot in the outer areas of the beam profile, whereas the smaller crater-like structure in the topography grows just slowly.

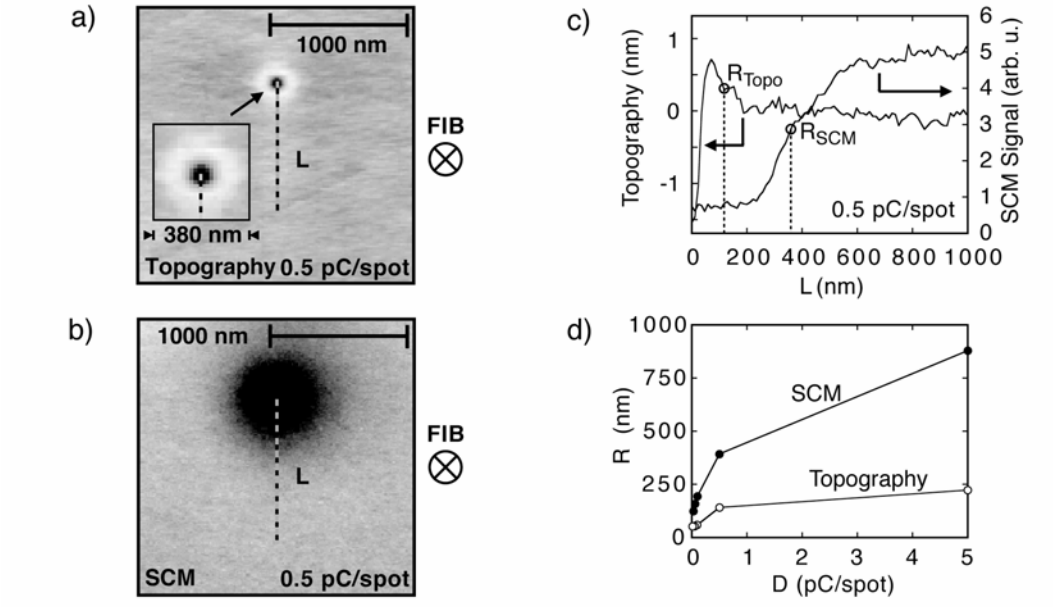

Fig. 1: (a) The topographic image of a FIB irradiated spot with an inset showing a magnification. The beam direction is indicated. (b) Corresponding SCM image. (c) Radial cross sections through the topographic and SCM images along the line L. R_{Topo} and R_{SCM} define the radius of damage as seen in the topographic and the SCM image. (d) R_{Topo} and R_{SCM} versus ion dose D.

A second important subject for FIB application is the determination of the width and depth of FIB induced damage below the sample surface. Figure 2 (a) shows the topography of the cleaved, FIB made trench. The corresponding SCM signal is shown in Fig. 2 (b). Again, we optimized the SCM bias to obtain the largest SCM signals in the unimplanted, low-doped areas. Figure 2 (c) compares the topographic and the SCM signal height plotted along line $L_{||}$ parallel to the incident beam. The distance between the trenches side walls and the SCM signal $\Delta R_{||}$ is approximately 620 nm. Previous TEM investigations of deep FIB milled polysilicon show an amorphisized region that extends about 200 nm in depth [8], which is only a third of the distance we have measured.

This can be explained by comparing the detection sensitivity of TEM and SCM. To get contrast in TEM, a crystalline substrate has to be amorphizised to a high extent, which needs relatively high ion doses. On the other hand, SCM is able to detect impurity concentrations down to 10 – 100 atoms per μm^3 (10^{13} - 10^{14} per cm^3), which is magnitudes more sensitive than TEM. Figure 2 (d) shows plots of the topographic and the SCM signal heights along line L perpendicular to the FIB direction. With a certain probability, ions can be scattered out of their incident direction. In this way, they can reach areas not covered by the beam area. The distance between the trenches sidewall and the SCM signal $\Delta R_{\perp}$ is about 310 nm. A comparison between Fig. 2 (d) and Fig. 2 (c) shows a ratio $\Delta R_{\perp}/\Delta R_{||}$ of 1/2, which is confirmed by previous TEM investigations of FIB induced damage in polysilicon-gates of MOSFETs [8].

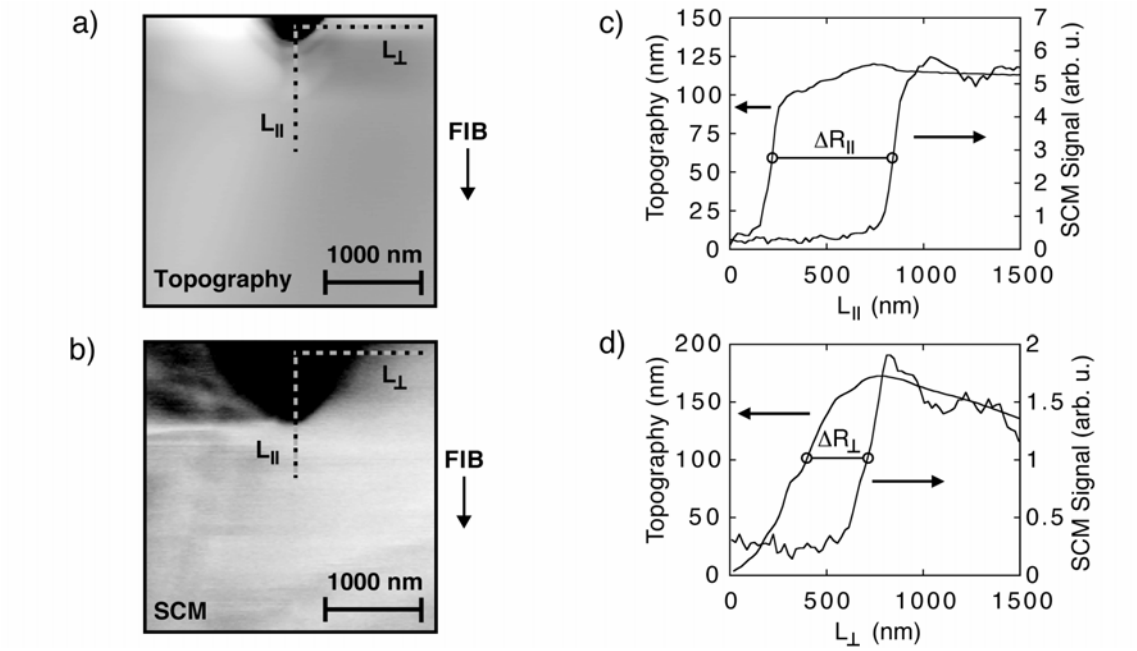

Fig. 2: (a) The topographic image of a FIB milled trench in cross sectional view. The beam direction is indicated. (b) Simultaneously recorded SCM image. (c) Comparison of topographic and SCM signal heights along the line $L_\parallel$ parallel to the ion beam. (d) Topographic and SCM signal heights along the line $L_\perp$ perpendicular to the incident beam.

Conclusion

In summary, we demonstrated the utilization of SCM for the characterization of FIB processed samples. First, the beam shape of a FIB machine was determined by taking SCM images of spots created by FIB irradiation. Our data indicate a beam shape consisting of a high intensity central region, which decays very quickly when the center is left, and vast tails where the intensity is small but declines more slowly with radial distance. Second, we investigated how deep below the FIB modified surface changes in the structural and electrical properties can be sensed. Damage was detected in much greater depths than reported by other authors, which is probably due to the increased sensitivity of SCM compared to other methods. Finally, the damage depth in the direction parallel to the incident beam and perpendicular to it has been investigated and was found to be in agreement with literature.

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Post-Process CMOS Channel Profile Tailoring With Focused Ion Beams

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This paper presents a novel approach of lateral profile engineering addressing sub-lithographic dopant spikes in the MOS channel region. In contrast to conventional approaches, our focused ion beam based method needs only one single dopant activation and damage anneal step avoiding unwanted effects like TED of the implanted species and broadening respective washout of the dopant profiles. We show the viability of this approach to engineer CMOS devices by *in situ* monitoring the impact of the ion beam on device performance, and we prove peak channel implants to gain devices with superior I_{on}/I_{off} ratios and enhanced short channel effect control.

Introduction

In order to overcome the leakage/I_{Dsat} tradeoffs and detrimental short channel effects (SCE) of MOS devices in the deep submicron regime, recent investigations focus on optimized MOSFETs incorporating sharp, sub-lithographic doping peaks, preferably at the source side of the channel [1]. As simulation studies explained [2], the I_{on}/I_{off} ratio of MOS devices can be greatly improved by the introduction of peaking channel dopings. These tripartite channel MOS devices (further on denoted TMOS) should be much less prone to hot carrier degradation due to reduced electric fields, and furthermore less affected by DIBL, thus being easier to scale into the ultra-deep submicron regime. The purpose of this work is to explore the FIB as a high resolution restructuring tool for front end prototyping.

Device Fabrication

In contrast to all work done up to now, in which the doping peaks were implanted during a baseline CMOS process [1] prior to the gate-oxide formation, we implement the doping peak at the very end of the front-end process.

By a masked through-gate implantation, thermal cycling can be reduced to the minimum necessary to eliminate damage and to guarantee dopant activation. The implantation peaks are located at the center of the channel (symmetric device indexed by s) and one quarter off the center (asymmetric device indexed by a) (Fig. 1).

The devices are fabricated relying on preprocessed, fully featured MOS devices with planar silicon gate technology, LDD structure incorporating n^+ polysilicon gates and 9 nm gate oxides. The effective channel length is 0.6 µm for p-MOS and 0.75 µm for n-MOS devices. These n/p-MOS devices are subjected to gallium and phosphorus implants via hard masks, yielding narrow p^+, respectively n^+ regions, dividing the channel into three sections (Fig. 1).

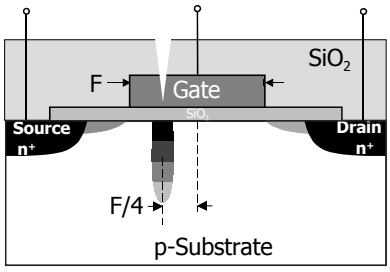

Fig. 1: Schematic of a tripartite n-channel MOSFET (n-TMOS) device with implantation hard mask in an asymmetric configuration.

The implantation windows are formed on top of the gate stack by means of a focused ion beam scheme. The TEM image in Fig. 2 shows a cross section of the implantation trench. All implantation windows for the devices have footprints below 30 nm, thus addressing a sufficiently small aspect ratio respective to the gate related feature sizes.

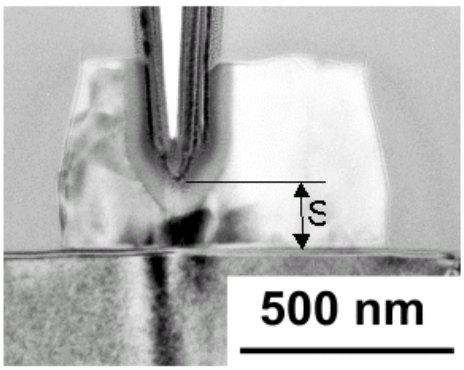

Fig. 2: TEM image of the TMOS with remaining gate seat S

The milling of the implantation trench with Focused Ion Beam is controlled by *in situ* electrical testing. Figure 3 exhibits the drain and gate current during FIB milling of the implantation trench.

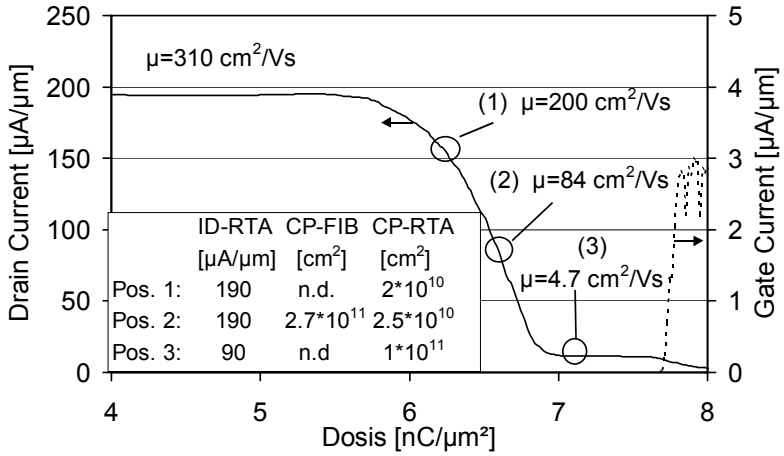

Fig. 3: MOSFET degradation due to FIB milling ($V_G = V_{DS} = 3$ V).

Despite of the fact that the extension of the amorphous region is kept fairly distant to the interface, the transistor begins to degrade due to the decreases of the electron mobility in the disturbed channel region. Charge pumping measurements indicate the formation of interface traps as far as the gate seat approaches 300 nm. Position (2) in Fig. 3 marks the final milling depth with a minimum gate seat of 220 nm. Up to that point, the entire FIB induced damage could be annealed out by an RTA process, and all substantial transistor characteristics could be completely recovered.

Device (dopant)	D[ions/cm^2] E [keV]	V_{th} [mV]	I_{leak} [A/µm]	I_{Dsat} [µA/µm]	SS [mV/dec]
conv. n-MOS	none	509	$1x10^{-13}$	402	82
n-TMOS$_a$ (Ga)	$2x10^{13}$/300	1018	$3x10^{-15}$	319	98
n-TMOS$_s$ (Ga)	$2x10^{13}$/300	1025	$7x10^{-16}$	59	99
n-TMOS$_s$*) (Ga)	5e12/300	842	$5x10^{-14}$	318	103
conv. p-MOS	None	-729	$2x10^{-16}$	196	85,7
p-TMOS$_a$ (P)	$2x10^{13}$/180	-876	$4x10^{-18}$	163	84.6

*) n-TMOS with low dose peak implantation

Tab. 1: Device parameters: implantation dose and energy, threshold voltage, leakage and saturation currents, and the sub-threshold swing.

Electrical Results

Charge pumping was used to determine the interface state density and the residual damage after through-gate implantation and proper post-treatment. Figure 4 exhibits the efficiency of the RTA process for damage anneal.

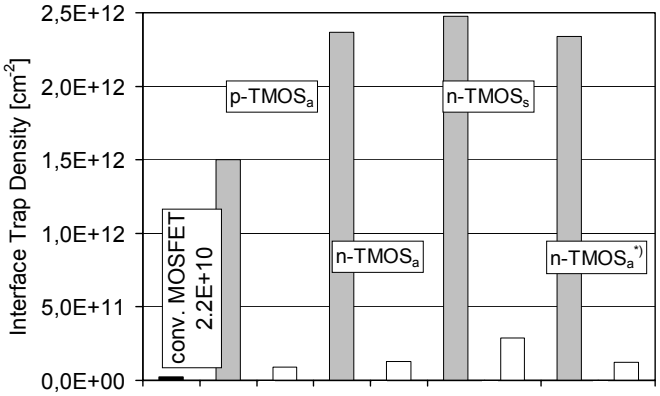

Fig. 4: Interface trap density of MOSFET and TMOS devices after through gate implantation (grey bars) and after RTA processing (white bars).

As expected, the interface trap densities correlate with implantation doses and with ion species, but depend evidently much stronger on the doping peak positioning within the channel. In the asymmetric case the damage cascades overlap with the highly doped S/D region, therefore part of the defects are electrically not detectable. The sub-threshold characteristics shown in Fig. 5 exhibit regular behavior and show off-state leakage currents one to two orders of magnitude lower compared to the conventional MOS devices.

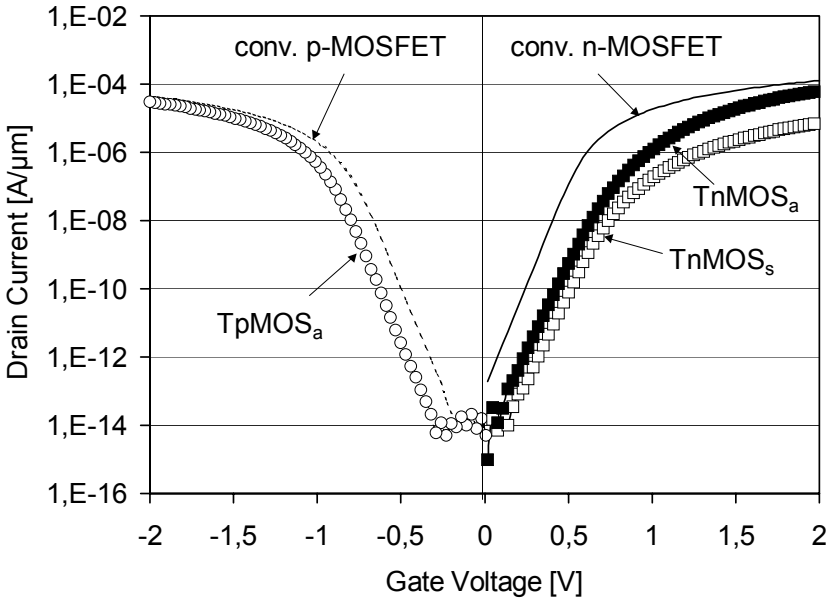

Fig. 5: Comparison of the sub-threshold characteristics for conventional MOSFET and TMOS devices (U_{DS} = 2 V).

The increase of threshold voltage is shown in Tab. 1. The gate drive characteristic in Fig. 6 exhibits the expected improve of the output resistance [1] of the TMOS device with even higher output currents for low gate voltages.

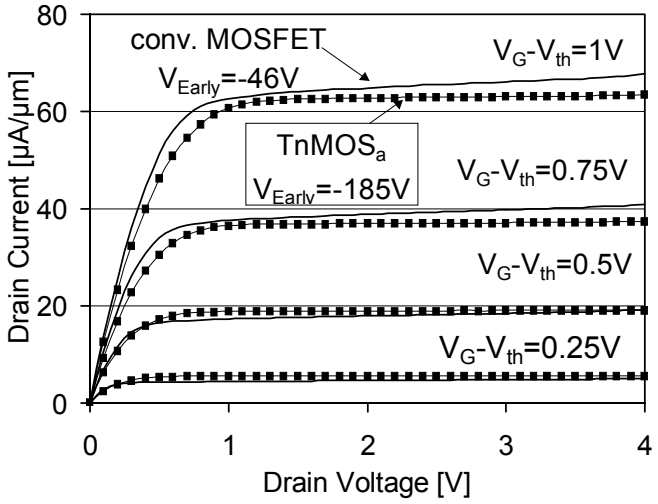

Fig. 6: Gate drive characteristic for the asymmetric n-channel TMOS$_a$ and conventional n-MOSFET device.

Beside the improved device performance, TMOS devices also exhibit enhanced SCE resistance, whereby the placement of the doping peak relative to the LDD extension junction is critical. Figure 7 exhibits the improved DIBL tendency of TMOS. Under reverse biasing conditions, the improved DIBL resistance is kept for the symmetric TMOS devices whereas for the asymmetric device the DIBL gets even worse.

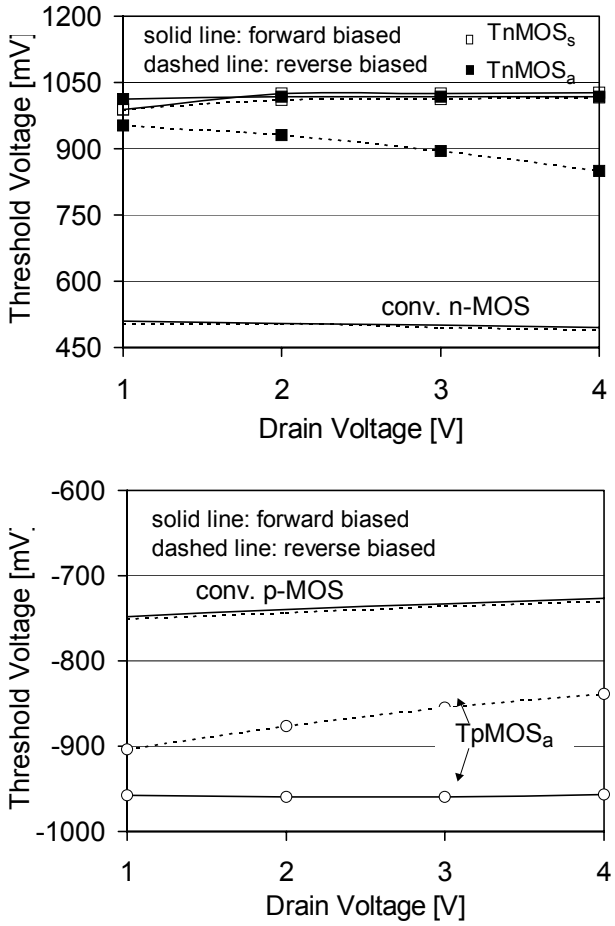

Fig. 7: V_{th}-V_D characteristics of n- and p-MOS devices.

According to the exponential dependence of hot electron degradation on the magnitude of the lateral drain electric field as predicted by simulation results [2] the I_{SUB}/I_{DS} ratio of n- as well as p-channel TMOS devices is 30% lower than that of the conventional MOSFET. The improved resistance to punchthrough of n- and p-TMOS devices is shown in Fig. 8.

Summary

This paper presents a novel technology of lateral profile engineering addressing tripartite channel MOS devices. For the first time MOS devices with highly nonuniform 2-D doping profiles are achieved by post-process implantation of channel doping peaks. In contrast to the conventional approach our focused ion beam based method needs only one moderate dopant activation and damage anneal avoiding unwanted effects like TED of the implanted species and broadening respective washout of the dopant profiles. We have shown, that post implantation can be successfully implemented to form TMOS devices with excellent I_{on}/I_{off} ratios and short channel effect control.

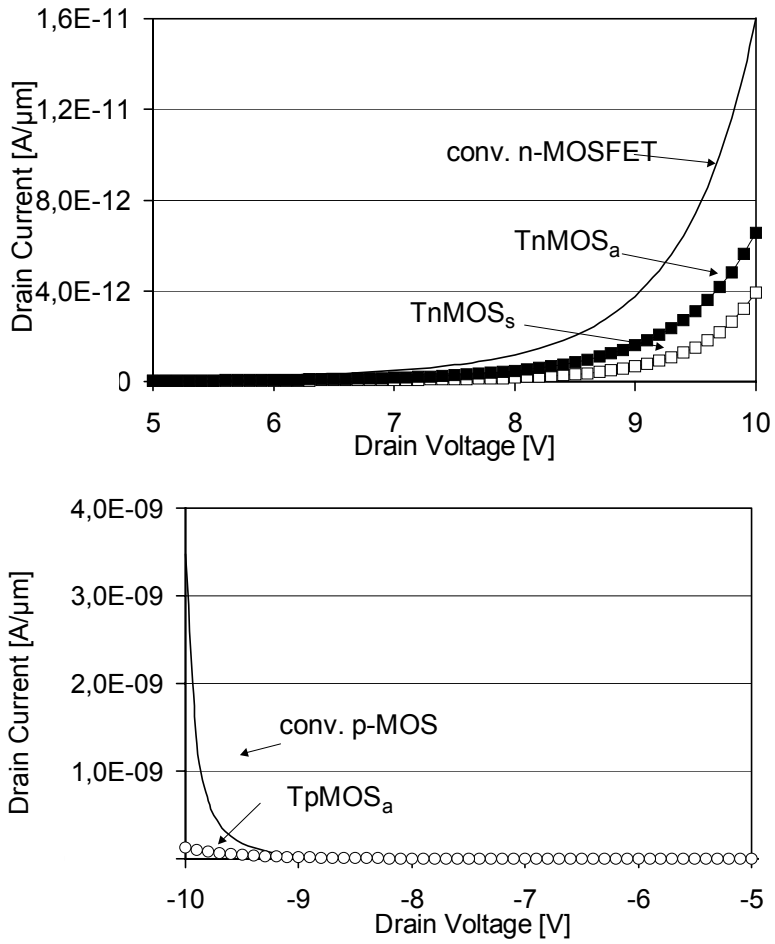

Fig. 8: Punchthrough characteristics of n-MOS devices.

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Deposition Mechanism of Direct-Write Processes – An Application-Oriented Approach to Custom-Tailored Material Properties

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Chemical vapor deposition (CVD) utilizes the adsorption and decomposition of a volatile gaseous species on a sample surface. For coating of large areas thermal CVD or plasma enhanced CVD has been established as versatile deposition technique for dielectrics and metals. In contrast to large area coating techniques, a local direct-write technique is introduced using a focused energetic beam to provide the necessary activation energy for CVD. With a focused ion beam, material has been locally deposited within a strictly confined area down to the nanometer range. For this direct-write nanodeposition of silicon oxide, two precursor gases – siloxane and oxygen – have to be added simultaneously. For this local CVD process, an exposure by a scanning beam (FIB) followed by a waiting time allowing for new re-adsorption of the precursor is required. An influence of the different ion exposure times per scan and an effect of the mixture ratio of precursors in the gas phase have been observed. The chemical composition of the solid silicon oxide and the physical properties can be tailored to demand by deliberate changes of process parameters. The beneficial aspects of the process versatility are demonstrated by deposition of insulating layers, structures with smooth surfaces, and 3-dimensional structures.

Introduction

Chemical vapor deposition (CVD) has become extremely popular in microelectronic manufacturing. Due to the versatility of the process CVD is the preferred deposition technique for a wide range of materials – especially for dielectric compound materials. [1]. The requirement for specific shapes of dielectric material in specific functional units has led to the fact that structuring the layer fabricated by CVD is as crucial as the deposition process itself. Multiple process steps including optical lithography followed by chemical etching are the predominantly used approach for structuring. Not only that etching raises the critical issues of material selectivity and etch stop layers, the lithographic approach requiring a specific photomask for every design is very inflexible and time consuming before the first device can be produced. For mass production, the lithographic approach remains unmatched in high throughput and economical value. For rapid prototyping and for 3-dimensional devices an alternative strategy has been sought for a long time.

Recently, direct-write processes utilizing a focused beam of ions, photons or electrons have shifted in the focus of increased interest, as they combine deposition and patterning in a single step [2]. A local gas atmosphere is maintained by introducing the precursor components via a micro-nozzle system [3]. The reaction energy is brought in by energetic ions so that the deposition only occurs in the confined area where the incident ions strike the sample surface [4]. In contrast to large area CVD that needs subsequent lithographic structuring, FIB-CVD allows depositing material while simultaneously obtaining the required structures [5], [6]. This sophisticated technique finally closes the long endured gap between the demand for high-qualitative dielectric material on one hand and a quick prototyping technique for device development on the other hand.

However, the multitude of process parameters with FIB-CVD does not allow a straightforward control of the deposition process, but requires extensive knowledge of the process and the chemical reaction. In this study, both the chemical parameters such as gas phase composition and the beam-related parameters such as pixel spacing have been investigated. The gained process knowledge allows selecting in advance material quality, the deposition rate, and the surface roughness of the deposited layers. An optimum process range has been identified yielding silicon oxide with low contamination and high electrical resistivity [7]. This technique will facilitate the application for fabrication of nanostructured materials in micromachining, MEMS, and for modification of interconnects of microelectronic circuits [8] – [10].

Experimental

Focused beam induced CVD utilizes a focused ion beam with a spot size in the nm regime to initiate the deposition reaction on an arbitrary surface. This maskless direct-write technology facilitates the additive fabrication of dielectric material and structuring towards functional units within a single process step. By guiding the scanned beam, the CVD can be used to deposit pattern designs. Due to the small spot diameter, material deposition can be restricted to the nanometer range so that 3-dimensional nanostructures can be fabricated.

A gas mixture of siloxane (tetramethylcyclotetrasiloxane) and oxygen has been used as chemical precursors to facilitate the deposition of silicon oxide. A focused ion beam of Ga^+ ions has been employed to induce the chemical reaction of the components adsorbed on the substrate surface. As the maintenance of a focused particle beam requires vacuum condition (base pressure 10^{-6} mbar), the chemical precursor compounds were introduced via a micro-nozzle system positioned in close vicinity to the deposition area. The co-adsorbed components are decomposed under formation of silicon oxide by the secondary ions and secondary electrons generated by the impact of the 50 kV Ga^+ ions.

The visual inspection of the deposited structures was performed *in situ* by FIB-imaging recording the secondary electron signal during the beam scan. For purposes of illustration of 3-dimensional structures, the sample surface was tilted during imaging to yield an advantageous view angle. Deposited pads (100 x 100 µm) were used for chemical characterization of the material by secondary ion mass spectroscopy (SIMS) and by Auger electron spectroscopy. The sample surface was pre-cleaned by *in situ* ion milling to remove adsorbed surface species. The characterization of the surface roughness was determined by high resolution transmission electron microscopy (HRTEM) imaging of cross-sections of the deposited layers or by atomic force microscopy (AFM) using tapping mode scans.

Results

With direct-write deposition techniques, arbitrary structures were grown by defining the scan area of the focused beam with a pattern generator. Three-dimensional structures and large layers covering areas up to 1 x 1 µm were deposited without stitching. The dwell time of the beam on a single pixel of the scan was kept short enough to provide a sufficient surface adsorption of precursor for the deposition process. A long exposure of a single spot leads to complete consumption of the adsorbed precursor. This results in increased ion milling and high contamination by Ga and C. The control of the scan area and the scan parameters were shown to be suitable parameters for the custom tailoring of structural features and the surface topology.

Custom-tailoring of structural features

The repetition of the exposure with the energetic beam primarily defines the thickness of the deposited layer. The chemical reaction to deposit material locally is triggered by the energy of the focused energetic beam. By restricting the exposure area on a 2 x 2 µm area and choosing a high repetition of the exposures, pillars with a high aspect ratio of 15:1 could be fabricated (Fig. 1) The efficiency of the deposition was found to depend on the dwell time per exposure cycle and the pixel spacing. By tilting the surface plane during deposition, inclined structures could be deposited (Fig. 1).

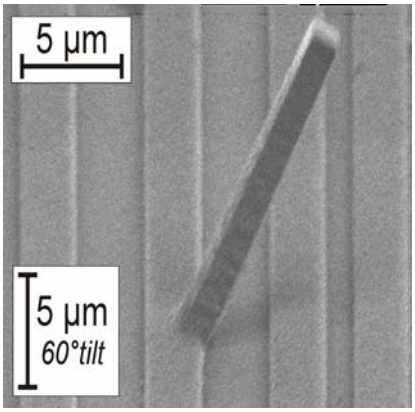

Fig. 1. FIB-deposited 2 x 2 µm pillar made of dielectric material with a total height of 30 µm total. The pillar is deposited with a controlled 30° tilt to the sample surface.

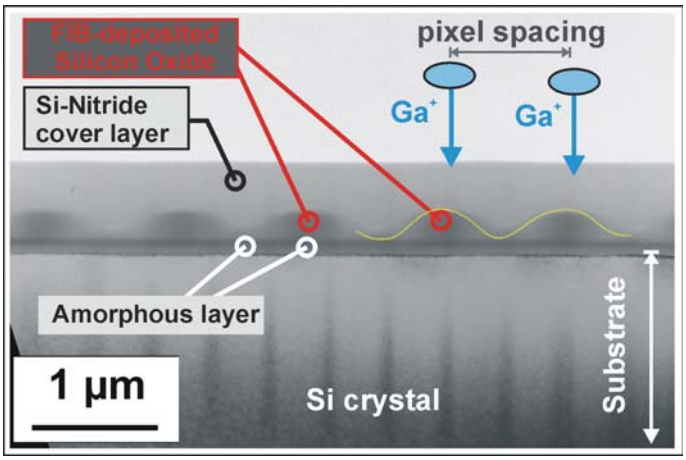

Fig. 2. TEM - cross section (left) Silicon oxide was deposited with a 1 µm pixel spacing of a 300 nm beam. A pattern of deposited bumps was obtained allowing to generate a predefined surface roughness.

In previous studies, the influence of the pixel spacing on the chemical composition of the deposited silicon oxide was confirmed. By choosing a large pixel spacing exceeding the diameter of the focused beam also the morphology can be influenced deliberately. By adjusting the pixel spacing during the deposition scans larger than the beam diameter, an intentional surface roughness can be generated. By depositing silicon oxide with a pixel spacing of 1 µm, a repeated pattern of depositions could be produced. The cross-section of this layer shows distinguishable bumps of silicon oxide

with a periodicity of the pixel spacing and a height of 200 nm (Fig. 2). The FIB-deposited material was covered with a protective layer of silicon nitride to inhibit artifacts during polishing of the ultrathin cross-section for HRTEM-imaging. By adjusting the pixel spacing small enough to produce a beam overlap, smooth surfaces with a RMS roughness of 3.2 nm were obtained according to AFM measurements. However, the deposition efficiency was observed to decrease with narrow pixel spacing. It is assumed that the consumption of precursor in overlapping beam spots exceeds the re-adsorption rate from the gas phase, so that the sufficient precursor coverage is not assured any longer.

Chemical Composition

The gas composition was observed to have a fundamental influence on the deposited material. As mentioned before, refresh times between the single scans were chosen long enough to work under steady-state conditions excluding diffusion-limited kinetics. With two precursor components silicon and oxygen, those substances are undergoing permanent competitive co-adsorption on surface sites. Their mixture ratio in the gas phase and the total gas pressure above the sample is decisive for the adsorption status. The surface concentrations of every precursor species are influencing for the chemical composition of the deposited dielectric (Fig. 3). Using only pure tetramethylcyclotetrasiloxane $Si_4O_4C_4H_{16}$, an atomic ratio of Si:O = 1:1 is already given. Adding molecular oxygen O_2 shifts the ratio towards higher oxide contents.

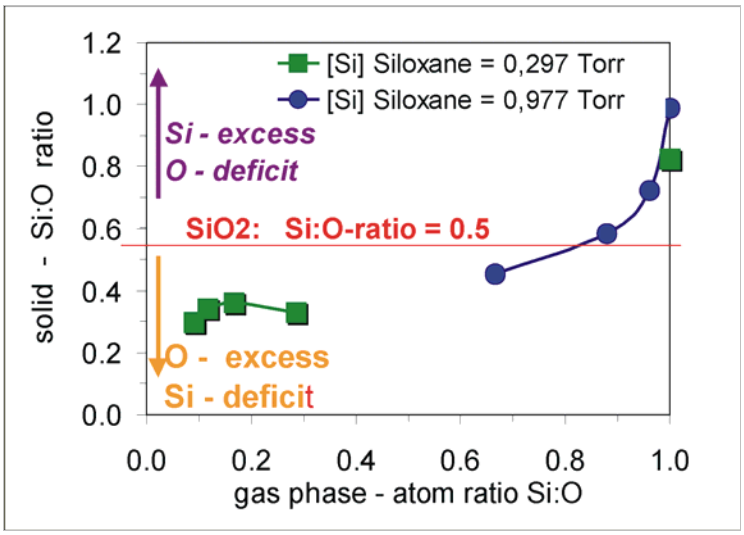

Fig. 3: Si:O atom ratio in deposited solid silicon oxide in correlation to the Si:O atom ratio in the precursor gas mixture. (The siloxane (TMCTS) has a Si:O atom ratio of 1:1. The addition of O_2 changes this ratio.)

The highest purity of deposited silicon oxide could be obtained at a ratio of TMCTS:O_2 = 1:10, reflecting an atomic ratio of Si:O = 1:6. At this mixture ratio, carbon contaminations have dropped below the detection limits of Auger electron spectroscopy, and the Ga implantation is in the range of 10%. In addition, the total pressure of the gas mixture has a significant influence on the deposited material (Fig. 3). A high total pressure was found to be beneficial for the deposition of silicon oxide close to the stoichiometric 1:2 composition of SiO_2. Selecting a precursor gas mixture with a high total pressure and an excess of oxygen, a silicon oxide with low contaminations and a composition close to silicon dioxide was deposited.

Conclusions

Direct-write deposition by a focused energetic beam allows local deposition of dielectric material with a feature size down to the deep sub-µm range. In this work, utilization of a focused ion beam (FIB) for deposition is described as an unorthodox type of chemical vapor deposition (CVD) using the energy of the energetic beam to initiate the chemical reaction only in a confined region.

Experimental results demonstrate the versatility of this method. Direct write deposition allows for custom tailoring of 3-dimensional structures by scanning the beam in a pre-defined pattern. FIB-CVD allows fine-tuning the chemical composition of the deposited material by controlling the gas atmosphere. Furthermore it has been shown that the surface roughness can be modified by deliberate control of the process parameters.

This unmatched flexibility of direct-write deposition of dielectrics bears the potential of becoming a key technology for rapid prototyping of electronic devices as well as for the development of micromechanical systems and for the repair of optical components and photomasks.

Acknowledgement

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Insulating Films (Posters)

Zirconium Dioxide Thin Films for Microelectronics Deposited by Metal Organic Chemical Vapor Deposition

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The metal-organic chemical vapor deposition (MOCVD) of ultrathin zirconium dioxide from $Zr(tfacac)_4$ on (100) silicon is thoroughly investigated. Physical characterization addresses the evolution of surface topography and the impact of processing parameters on the chemical composition of the films to provide a sound basis for the discussion of electrical properties. Electrical investigation by means of MOS structures has been performed to assess the interface quality and the dielectric properties of the layers. Interface trap density is observed to be around 5.10^{11} $cm^{-2}.eV^{-1}$ at midgap for (100)-oriented substrates. Leakage currents in the ultrathin regime are significantly reduced compared to equivalent SiO_2-layers. The temperatures throughout the gate insulator formation process do not need to exceed 650 °C, and thus allow keeping the thermal budget low.

Introduction

Currently the search for a suitable high permittivity dielectric for the forthcoming replacement of SiO_2 as gate dielectric in leading-edge complementary MOS (CMOS) devices provides enormous impetus in this field of materials science. Yet, the identification of a suitable material may only be considered a partial success, since besides the material's properties themselves the entity of material and deposition method must meet the requirements for compatibility with CMOS technology.

While the various methods based on physical vapor deposition (PVD) provide a convenient means for the evaluation of materials systems for alternate dielectric applications, technological considerations concerning device morphology in general rule out such line-of-sight PVD processes as stated by G.D. Wilk *et al.* [1]. On the other hand, different methods of chemical vapor deposition (CVD) have proven quite successful in providing uniform coverage over complicated device topologies. Therefore, our approach utilizes MOCVD, which in general allows processing at lower temperatures than CVD from inorganic precursors.

Group IVB oxides and materials based on these oxides are among the most promising candidates for the succession of SiO_2 as gate dielectric. This is mainly due to their dielectric constants around 20 and – maybe of even higher importance – the sufficient band-offsets provided towards silicon (as displayed in Fig. 1) to suppress tunneling.

We evaluate the properties of thin films of zirconium dioxide with equivalent oxide thicknesses (EOTs) down to the 2 nm range. Chemical composition, surface topography and electrical properties are examined in dependence on thin film processing.

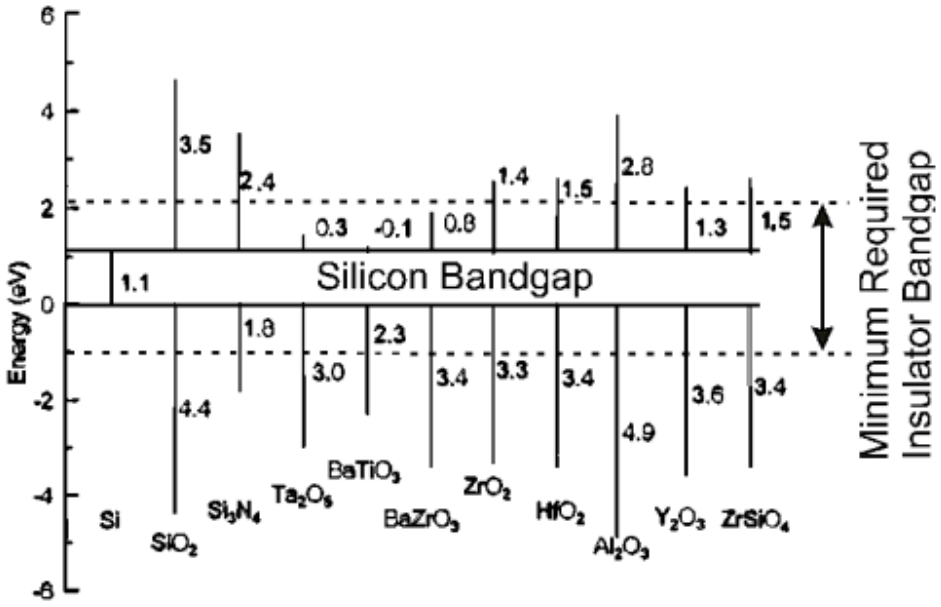

Fig. 1: Band-offsets in respect to silicon provided by several high-k materials. Minimum requirements are indicated (adapted from [2]).

Experimental

Thin films were deposited on p-type silicon (100). The deposition apparatus consisted of a horizontal hot wall reactor with a bubbler system for the delivery of the metal-organic precursor substance. Zirconiumtetrakistrifluoroacetylacetonate was used as precursor due to the favorable properties of this substance in terms of stability and volatility. A detailed description of the deposition process is given in [3]. In order to improve thin film properties different annealing procedures were tested. Oxidizing (20% oxygen in nitrogen) as well as reducing (forming gas, 10% hydrogen in nitrogen) atmospheres were used during annealing at 650 °C. The chemical composition of the films was analyzed by Auger electron spectroscopy (AES) before and after annealing. Surface topography of the deposited films was examined by atomic force microscopy (AFM). For the evaluation of the electrical properties of the thin films, MOS capacitors were constructed. Capacitance-voltage (C-V) and current-voltage (I-V) measurements provided information about EOT, trap and charge densities as well as leakage currents.

Results and Discussion

Topography of the deposited films was evaluated by AFM. The relative roughness ($R_{a,\,rel}$) as the ratio of absolute roughness R_a and total film thickness was used for comparison of the results. This evaluation shows a deposition at 450 °C to result in minimum surface roughness. The graph on the left in Fig. 2 presents the evolution of the relative surface roughness for films with thicknesses up to about 400 nm. The AFM surface plot to the right of Fig. 2 shows that for very low film thicknesses much smoother films – on absolute and relative scale – are obtained. The roughness of the 15 nm thick film amounts to only R_a = 0.135 nm, equaling less than 1 % relative roughness.

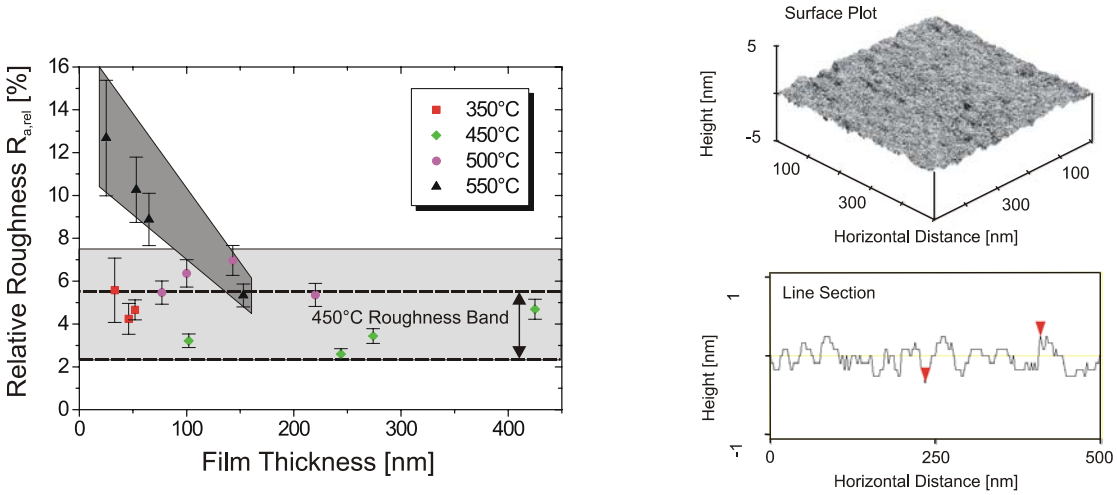

Fig. 2: Left: The evolution of surface roughness with film thickness for thicknesses up to 400 nm. 450 °C deposition temperature leads to smoothest films. Right: AFM surface plot of a 15 nm ZrO_2 thin film deposited at 450 °C. A surface roughness of R_a = 0.135 nm is observed with a peak-to-peak roughness of 0.58 nm in the displayed line section.

This improvement of the film smoothness in the ultrathin film region may be connected to a change in the crystallinity of the films. While transmission electron microscopy (TEM) showed thicker films to be polycrystalline, the smoother surface of the thinnest films possibly points to an amorphous state of these films. However, definitive results are not available by now, and the issue deserves closer attention and clarification by high-resolution TEM examination.

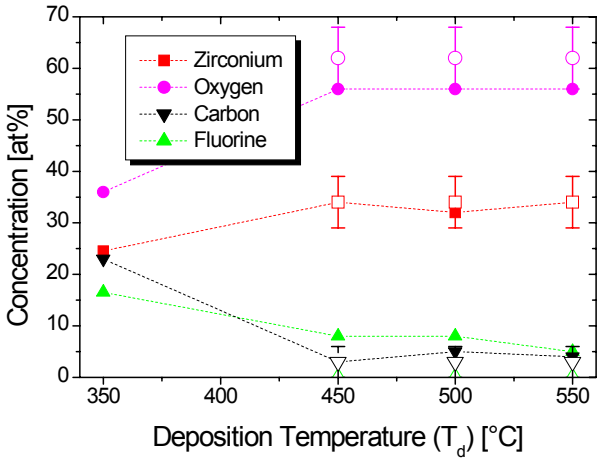

Fig. 3: Chemical composition of thin films deposited at various temperatures (full symbols) and composition achieved after post-deposition annealing (open symbols). For reasons of clarity, the estimated error is indicated for the composition after annealing only.

Figure 3 shows the chemical composition of the films in dependence on the deposition temperature. The unfavorable effect of a too low deposition temperature is clearly discernable, while for medium temperatures a constant film composition is observed only suffering a slight oxygen deficiency. After annealing in either diluted oxygen or forming gas at temperatures of 650 °C or above, the film composition closely approaches the stoichiometric composition ZrO_2. After temperature treatment, the remaining carbon impurities are at a negligible level at the limit of detection.

Al-ZrO_2-p^+Si capacitor structures served as test vehicles for the evaluation of the electrical characteristics of the processed thin films. EOTs down to the 2 nm range have been realized sustaining favorable dielectric and interface properties. Figure 4 displays on the left the C-V curve of a MOSCAP featuring a dielectric with 2 nm EOT of zirconium dioxide as obtained after annealing in diluted oxygen. A flatband voltage shift (ΔV_{FB}) of about –600 mV and minor distortion near midgap is observed in a generally well-behaved curve. The C-V plot on the right side shows that ΔV_{FB} as well as the distortion near midgap are minimized if forming gas is used as annealing atmosphere. However, in this case only EOTs down to about 3 nm are accessible, while post-deposition annealing in an oxidizing atmosphere was found to further reduce EOT.

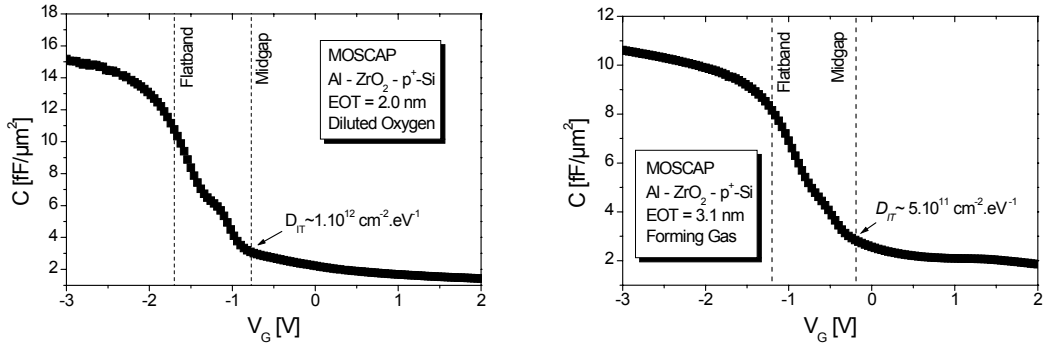

Fig. 4: C-V curves of MOSCAPs with ZrO_2 dielectrics annealed either in diluted oxygen (left) or forming gas (right). Lower EOTs are observed after annealing in oxygen, while electrical characteristics are more favorable after annealing in forming gas.

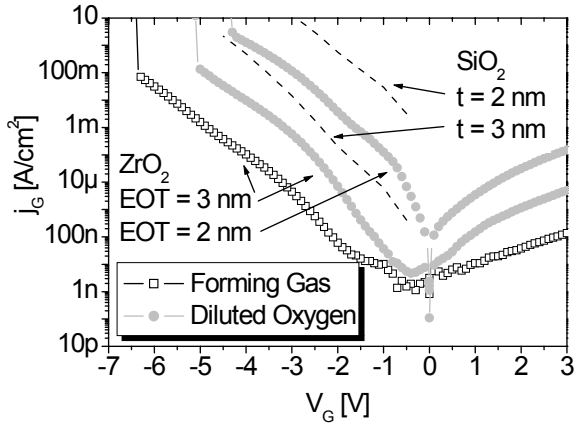

Fig. 5: I-V properties of Al-ZrO_2-p^+Si MOSCAPs. A more than three decades lower leakage than in SiO_2 is observed for ZrO_2 after annealing in forming gas. SiO_2 leakage characteristics are extracted from [4], [5].

Using Terman's method, interface trap densities (D_{IT}) of differently annealed samples were computed. For samples annealed in forming gas, D_{IT} values around 5.10^{11} $cm^{-2}.eV^{-1}$ are usually obtained. Comparable samples annealed in diluted oxygen displayed a higher D_{IT} in all cases. The I-V properties of the thin films are depicted in Fig. 5. For both kinds of anneal ZrO_2 provides a significant decrease in gate leakage compared to SiO_2. A reduction of leakage by more than a factor of 10^3 can be accomplished for 3 nm EOT. Again a forming gas anneal proves advantageous for optimization of the material's performance, suggesting the formation of a large amount of additional charges and traps during annealing in the oxidizing atmosphere. Overall, the impact of the annealing atmosphere on the electrical properties of the films is much stronger than expected from compositional analysis.

Conclusion

The formation of high-quality ZrO_2 thin films on silicon by MOCVD has been successfully demonstrated. Compositional as well as electrical characterization unveils promising properties of the thin films down to the 2 nm EOT range. Throughout the gate insulator formation, processing temperatures do not require to exceed 650 °C, keeping the thermal budget low. Owing to these circumstances, further research to establish film deposition from metal-organic precursor substances in silicon technology is encouraged.

Acknowledgements

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Transport Phenomena (Posters)

Transport through Wannier-Stark States in Biased Finite Superlattices

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Individual Wannier-Stark states are resolved in a direct current experiment over a wide electric field range for a 5 and 4 period finite superlattice. A hot-electron transistor is used to probe the transmittance of the superlattices at different bias conditions. The energy level positions are used to determine superlattice parameters with high accuracy. The basic transport through Wannier-Stark states is identified to be coherent. Individual transport channels induced by LO-phonon scattering are observed when the Wannier-Stark states spacing tunes into the optical phonon energy.

Introduction

In an unperturbed superlattice, the strong coupling of the electronic eigenstates of adjacent wells leads to the formation of minibands that are separated by minigaps. In superlattices with a finite number N of periods, each single miniband is formed by N eigenstates, which are delocalized over the whole superlattice length. Applying an external electric field perpendicular to the layer planes alters the quantum mechanical confinement between the neighbouring wells and leads to a splitting and a localization of the states, which are then given by the Wannier-Stark states. In transport experiments, there are two main problems to determine the Wannier-Stark splitting in a semiconductor superlattice: one is the presence of an inhomogeneous electric field unavoidable in two-terminal superlattice structures; the second is the electric field induced localization of the Wannier-Stark states. The localization length inside the superlattice is inversely proportional to the applied electric field, which leads to a quenching of the coherent hot electron transport through the individual Wannier-Stark states.

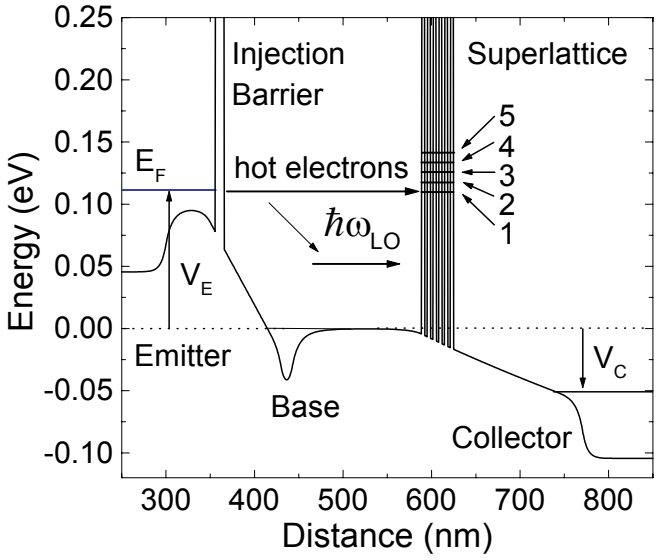

Fig. 1: Conduction band diagram of a hot-electron transistor in growth direction.

In this work, we use the concept of a hot-electron transistor [1] – [4] to study hot electron transport in undoped biased superlattices. The conduction band structure of the device is shown in Fig. 1. An energy tunable electron beam is generated at the tunneling barrier and reaches the superlattice after traversing a highly doped n-GaAs base layer and a slightly n-doped drift region. The static transfer ratio ($\alpha = I_c/I_e$) directly represents the probability of an injected electron to be transmitted through the superlattice. The three terminal device used in this work allows a tuning of the energy of the injected electron distribution independent of the electric field applied to the superlattice.

Experimental

Hot-electron transistors were designed with different undoped superlattice structures between base and collector. The first superlattice consists of 5 periods of 3.5 nm $Al_{0.3}Ga_{0.7}As$ barriers and 3 nm GaAs wells, the second superlattice consists of 4 periods of 4 nm $Al_{0.3}Ga_{0.7}As$ barriers and 3.2 nm GaAs wells. For these superlattice parameters, the lowest miniband is positioned between 122 meV and 158 meV for the 5 period SL and between 120 meV and 143 meV for the 4 period SL. The devices were grown by molecular beam epitaxy and were fabricated by standard photolithographic and wet etching techniques in 30 x 30 μm^2-MESA structures. Standard AuGe/Ni metallization was used to form ohmic contacts. Finally, CrAu pads were evaporated, serving as bonding pads. The emitter and collector currents were measured as a function of negative emitter bias at 4.2 K in a common base configuration using a parameter analyzer.

Results

Figure 2 shows the transfer ratio of the 5 period superlattice in the range of the first miniband as a function of the emitter bias. Below the energy of the first state, we observe no collector current, since the electrons that are injected into the drift region are reflected by the superlattice. This also indicates that no significant leakage current occurs between base and collector. The transfer ratio shows an onset at $V_E = -130$ mV, which indicates electron tunneling through the first resonant state of the miniband. Increasing the emitter bias leads to electron tunneling through the individual resonant states of the miniband. At energies above the first miniband, the ballistic electrons are reflected at the superlattice due to the minigap. In contrast to this behavior, the measured transfer ratio does not drop to zero in this energy range. This is due to the formation of phonon replicas in the drift region and their contribution to the shape of the transfer ratio. To get the energetic positions of the peaks out of the transfer ratios we calculate the second derivatives of the transfer ratios of both samples and take the positions of the corresponding minima. The energetic positions of the 5 (4) individual peaks in the transfer ratio at $V_c = 0$ V fit best to calculated subband energies using superlattice parameters of 3.3 nm AlGaAs barriers and 2.9 nm GaAs wells for the 5 period superlattice and 3.7 nm AlGaAs barriers and 3 nm GaAs wells for the 4 period superlattice. The deviation to the nominal superlattice parameters lies within one monolayer for GaAs and AlGaAs.

Hot electron transport in biased superlattices is investigated as a function of the collector bias up to V_C=400 mV. Figure 3 shows the measured peak positions (symbols) relative to the position of peak 3 for both superlattices as a function of the electric field. The experimental results are in excellent agreement to the theoretical Wannier-Stark splitting (solid lines) up to electric fields of F = 25.9 kV/cm for the 5 period superlattice and F = 27.6 kV/cm for the 4 period superlattice, respectively.

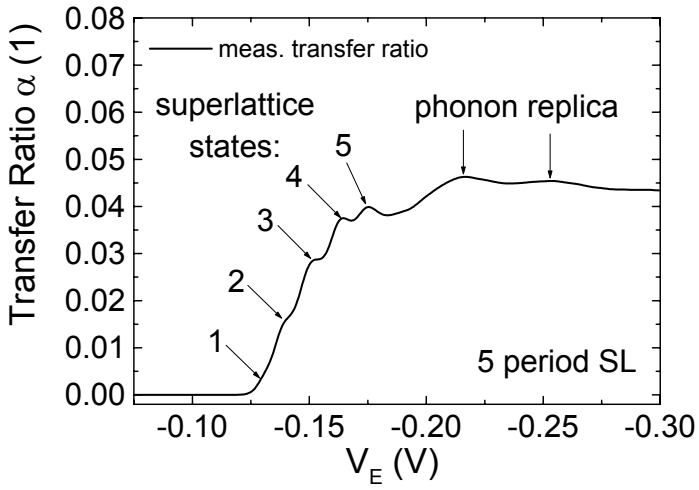

Fig. 2: Measured transfer ratio of the 5 period superlattice as a function of the applied emitter bias V_E.

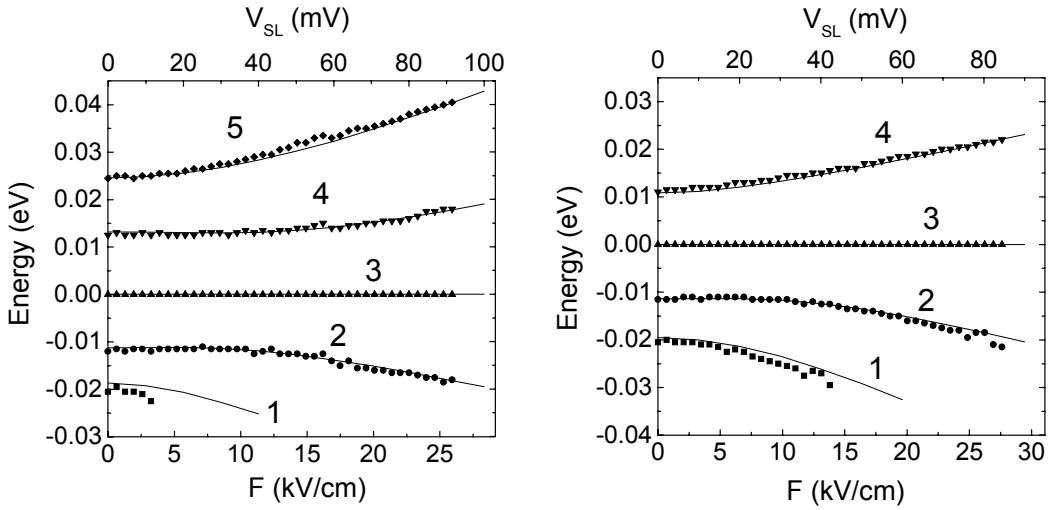

Fig. 3: Measured Wannier-Stark states (symbols) vs. superlattice bias V_{SL} of the 5 (left) and 4 (right) period superlattice compared to the calculated Wannier-Stark splitting (solid lines) vs. electric field F.

In transport experiments, the amplitudes of the current resonances directly resemble the quantum mechanical transmission of the individual states. A comparison of the electric field dependence of the normalized peak amplitudes in the transfer ratios with the expected Wannier-Stark localization amplitudes for the 4 period superlattice is shown in Fig. 4, which directly provides information about the transport mechanisms through each single state. For states 1 and 2, an excellent agreement between measured and calculated transmission is found. For peaks 3 and 4, the experimental findings exceed the coherent predictions: while peak 3 first shows a transmission according to the coherent path an additional contribution to the current starts at 10 kV/cm and becomes larger than the coherent part, passes through a maximum until it decreases at fields above 20 kV/cm. Peak 4 increases above the coherent part already at zero bias and increases in two steps.

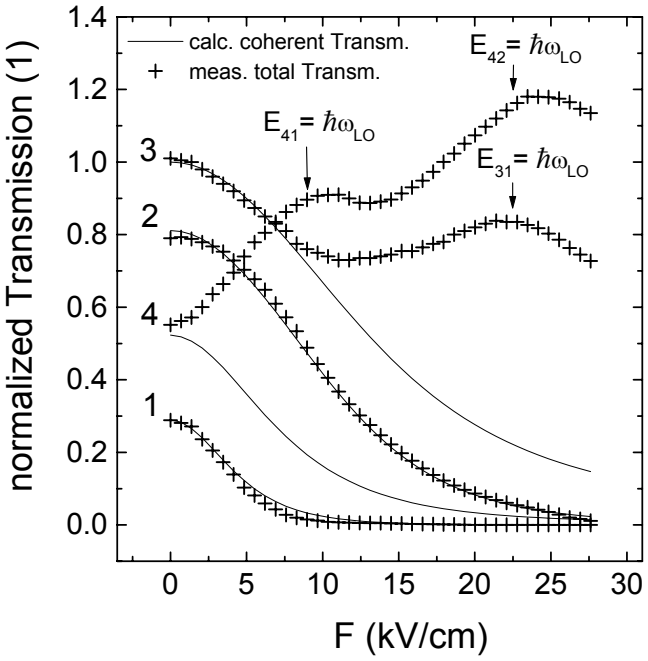

Fig. 4: Measured normalized transmission per states as a function of the electric field (crosses) compared to the calculated normalized coherent transmissions of the individual Wannier-Stark states for the 4 period superlattice (solid lines).

We have previously ruled out interface roughness scattering for a 5 period superlattice [2] as scattering always induces a current component proportional to the electric field which is not observed. Electron-electron scattering can be ruled out due to an extremely low carrier concentration in the device. The only incoherent transmission channel is LO-phonon scattering, which only occurs for transition energies E_{ij} exceeding $\hbar\omega_{LO}$. For the first and second Wannier-Stark state (WSS1, WSS2), LO-phonon scattering can be neglected because the transition energy is much smaller than $\hbar\omega_{LO}$ over the entire bias range. Consequently, transport through these states is purely coherent.

For WSS3 and WSS4, additional current is observed at electric fields where transition energies E_{31}, E_{41} and E_{42} exceed $\hbar\omega_{LO}$ at F_{31} = 21 kV/cm, F_{41} = 9 kV/cm and F_{42} = 22 kV/cm. The increase in the peak amplitude resembles the tuning of the Stark ladder with increasing electric field until the peak of the distribution is resonant with the Stark state splitting of $\hbar\omega_{LO}$. The results clearly show that incoherent transmission channels induced by optical phonons add additional current.

Conclusions

Individual Wannier-Stark states in the first miniband of a 5 (4) period superlattice are resolved up to electric fields of F = 25.9 kV/cm (F = 27.6 kV/cm) in a direct current experiment. From the measured transfer ratios, the exact superlattice parameters are determined. The basic transport through Wannier-Stark states is identified to be coherent. The transport mechanism through higher lying localized states is found to result from an interplay between coherent and incoherent transport as a function of the applied electric field. LO-phonon induced individual channels are found to contribute to the transmitted current. This way we have a method at hand that enables a systematic study of transition rates for different scattering processes in semiconductor heterostructures.

Acknowledgement

This work was supported by the Austrian Science Fund (FWF) Grant No. SFB F016 and Z24.

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Sensors (Posters)

Simulated and Measured Characteristic of a Micromachined Cantilever Sensor

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The miniaturized sensor is designed for measuring high magnetic flux densities. A micro machined U-shaped cantilever, which is moved by the Lorentz force, acts as deflecting mirror in an optical readout system. The ratio of the intensity of the light reflected by the front side of the cantilever to the intensity of the incident light is analyzed. Simulated and measured signals generated by the oscillating cantilever and their dependence on the exciting force are shown.

Introduction

High magnetic fields in the range up to 50 T are usually produced with cylinder coils placed in liquid nitrogen [1]. During the magnetic pulse, the Joule heat raises the temperature from 77 K up to room temperature. These ambient conditions make the measurement of high magnetic fields a highly sophisticated task. The presented sensor should be used to improve the control of the thyristor rectifier of the power source to get constant magnetic fields during the pulse. Due to the quasi-static conditions, induction coils are not applicable because they mainly detect the higher harmonics and have zero sensitivity at DC-field.

Sensor

For measuring the magnetic flux density, the bending of a U-shaped Si-cantilever is used. This deformation is caused by the Lorentz force (Fig. 1, left) on an electrical lead which is placed on top of the cantilever structure (Fig. 1, right). Neglecting the base of the U-shaped cantilever and the influence of the lead on the mechanical behavior the deflection d is given by

$$d = F_L \frac{2l^3}{Ebh^3} \qquad (1),$$

where h, b, l and E denote the thickness, width, length and Young's modulus of the cantilever and F_L the Lorentz force, respectively. The bending in Eq. (1) is a linear measure of the force assuming the length of the cantilever is much larger than its deflection.

Because the Lorentz force is proportional to the magnetic flux density and to the electrical current, the same deflection is produced if the field is reduced and the current is increased by the same factor. This enables the sensor development and calibration without high field equipment.

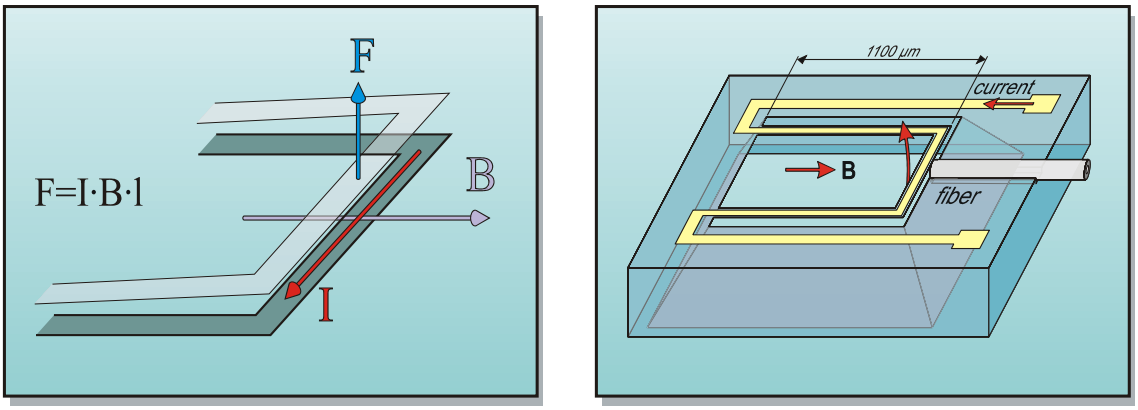

Fig. 1: Transducer principle (left) and sensor setup (right).

Many methods in detecting the position of a cantilever use capacitive sensing [2], [3] or strain gauges situated at the clamped ends of the suspension arms [4]. These methods work well when the electronic amplifier can be placed in the close vicinity of the moving part. Due to the low temperatures and high field change rates in the target application, the electronic parts have to be distant from the sensor.

Optical Readout [5]

Thus, the deflection of the cantilever is detected optically by measuring the light that is reflected by the front side of the cantilever. The light (IR-LED) is emitted and captured by the same optical fiber, which makes the mechanical setup as simple as possible.

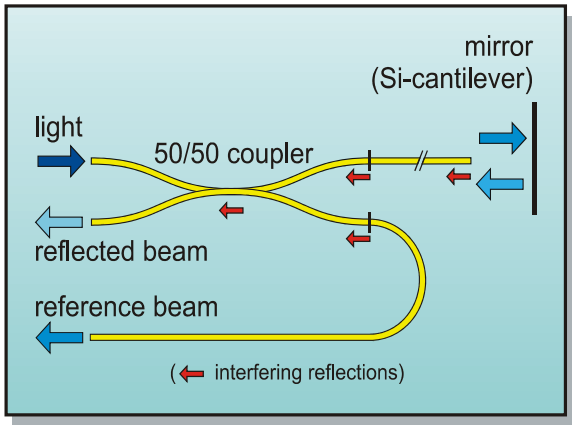

Fig. 2: Schematic drawing of the optical readout of the cantilever position.

To obtain ratiometric results, the light was split up into a reference beam and a measurement beam using an optical coupler (Fig. 2). The measurement beam is guided by a multi mode fiber (Corning 50/125) to the front side of the cantilever. The amount of reflected light depends on the cantilever position according to the section of the fiber that is opposite to the cantilever.

Initially, an infrared laser was used as light source, which offers intensity in the mW-range. However, due to the small number of modes propagating in the multimode fiber and to the reflected light back to the laser, the stability of the signal was low and the measurement setup became extremely sensitive to mechanical vibrations of the fiber.

For the simulation, a simple model was applied, assuming that only near field phenomena are of relevance. The reflecting front side of the cantilever, which acts as a moving mirror, was replaced by a moving slit in a non-transparent screen. Its width is equal to the cantilever thickness. The fiber is virtually split up into an emitting fiber and a capturing fiber that is situated at the mirror image of the emitting one.

To get a measured characteristic of the optical readout a piece of silicon was attached to the membrane of a loudspeaker and actuated at a frequency of 500 Hz. With a micromanipulator, the position of the fiber in respect to the cantilever has been varied. The measured characteristic (Fig. 3 left, circles) is nearly perfectly fitted by the simulated one. The differences indicate that the effective cantilever thickness is a little bit higher than in the simulation. The assumed Gaussian light distribution seems to be a suitable approximation (Fig. 3 left, solid line).

Sensor Characteristic

If we assume an ideal alignment of the fiber with respect to the cantilever, the cantilever faces the center of the fiber. We get a constant amount of the light for the still standing cantilever. For small oscillation amplitudes, the output signal is almost sinusoidal (Fig. 3 right). If the amplitude increases further, the cantilever gets out of sight of the fiber for a section of the oscillation period. The signal shows two peaks. The higher the amplitude becomes the more the peaks width shrinks.

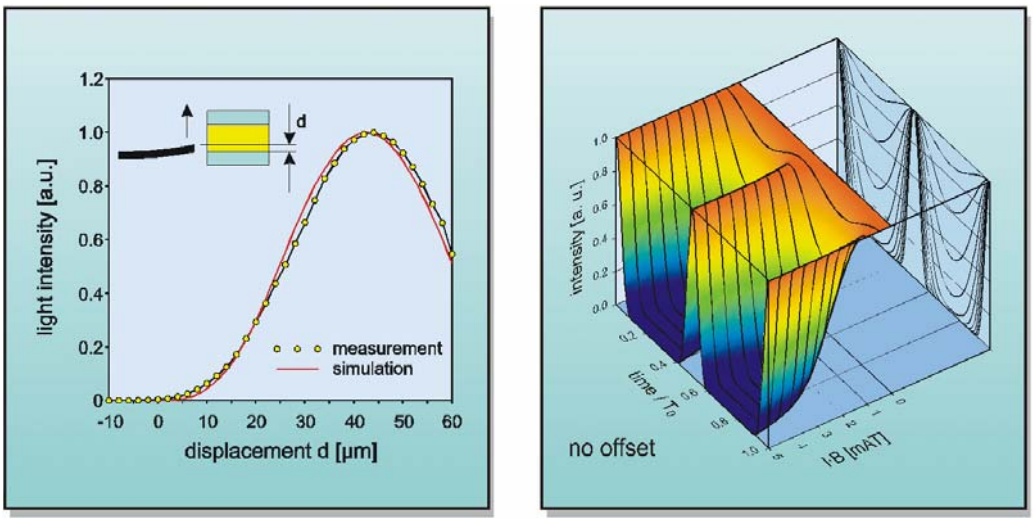

Fig. 3: left: Numerically modeled and measured characteristic of the optical readout. Both curves were scaled to unity.
right: Simulated Signals generated by an oscillating cantilever assuming ideal alignment.

For a real device, the center of the fiber cannot be aligned exactly with the zero position of the cantilever. The stress in the multilayer structure is bending the cantilever and the depth of the groove for guiding the optical fiber cannot be properly adjusted. The resulting offset changes the characteristic of the optical readout (Fig. 4 left). The varying peak height is a consequence of the limited resolution of the readout simulation. This effect increases the more the peaks width decreases.

The sensor signals (Fig. 4 right) were measured at 4800 Hz, which is 200 Hz below the resonant frequency. This frequency was chosen to get a suitable current range for the sensor characterization. The agreement with the measurements confirms the model

underlying the simulation. The differences occur from system properties that are not taken into consideration yet. The decreasing maximum amplitude of the measured signals with increasing I·B (corresponds to oscillation amplitude) is caused by the electronic amplifier which has a small bandwidth to reduce the noise.

With the available current load of the lead which is about 100 mA we expect a measurement range from of 40 mT to >40 T.

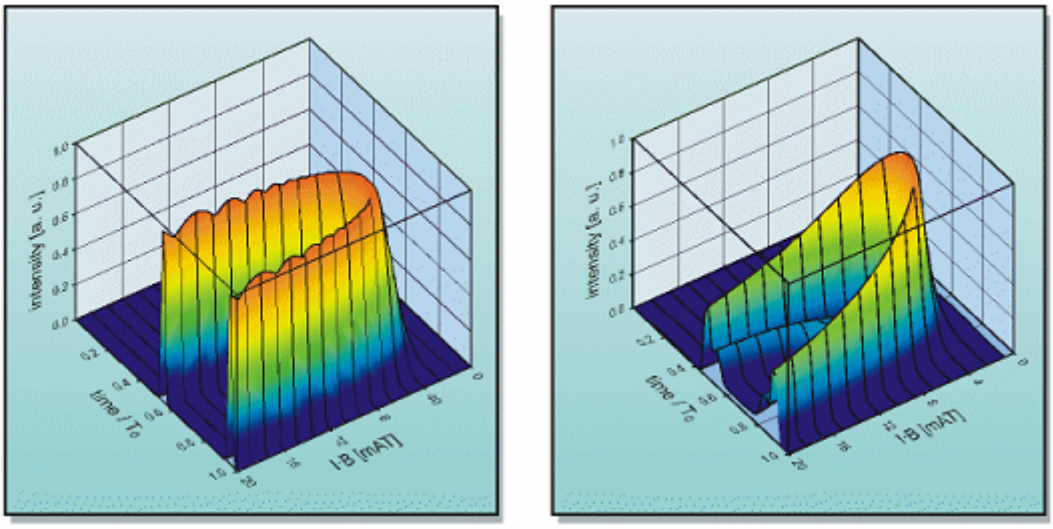

Fig. 4: left: Simulated signals generated by an oscillating cantilever assuming an offset of 40 µ.
right: Measured intensity signals depending on the amplitude ($\propto I \cdot B$)

Acknowledgements

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Novel Flow-Cell to Create a Sheath Flow with Adaptable Sample Flow Dimensions

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In this paper, a novel flow-cell is presented with a non-coaxial adaptable sheath flow for application in micro-fluidics systems. By two orthogonal control mechanisms, the vertical and horizontal dimensions of the sample flow can dynamically be adapted over a wide range. Experimental results are compared with the results from finite element simulations and show a good match.

Introduction

In this paper a novel flow-cell is presented in which the horizontal and vertical dimensions of the sample flow can be controlled dynamically, which allows application of many different sensing systems. The system has a non-coaxial sheath flow in which the sample flow touches one side of the channel (see Fig. 1); this assures a good contact with any sensor interface located on the channel bottom. Due to the limited interaction between sample flow and sheath flow, the sample flow can be considered as a virtual flow channel with adaptable dimensions (e.g. diameter 5% of physical flow-channel). As a result the presented system combines the advantages of a large diameter channel with those of a small diameter channel. Due to the small dimensions of the sample flow, the low detection limits of a small channel device can be achieved; at the same time, the large physical dimensions of the channel alleviate many problems such as clogging, air bubbles and fabrication tolerances.

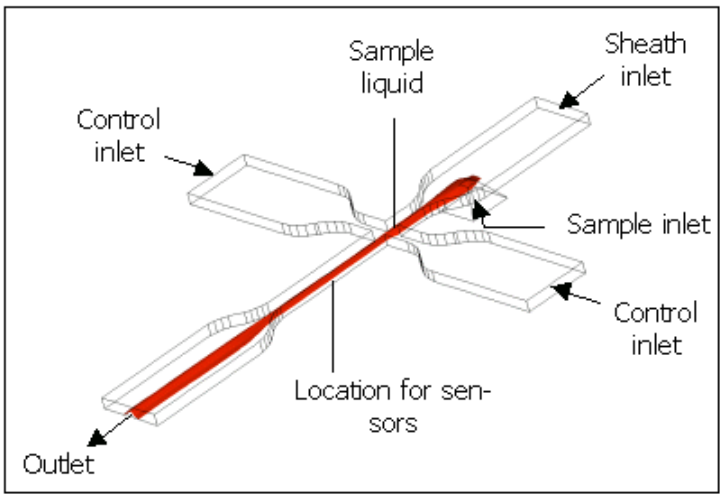

Fig. 1: Flow-cell to create the non-coaxial sheath flow; the relative flow-rate of the sample liquid (red) determines the height of the sample flow, adding or removing liquid through the control inlets controls the width.

One of the first realizations of sheath flow on a chip was achieved using with a 5-layer device [1]; recently less complicated devices were demonstrated [2], [3]. These devices do not offer dynamic, orthogonal control of the sample flow dimensions as presented in this paper. What is even more important: those devices were aimed at a traditional co-axial sheath-flow, which limits the possible sensors mainly to optical detectors, whereas the presented device is much more flexible.

Vertical Control of Sample Flow Dimensions

The sheath flow is formed by injecting the sample liquid vertically into the channel through which the sheath liquid is flowing; this forms a hydro-dynamically focused sample flow that still contacts the bottom of the flow channel (see Fig. 1). The vertical sample flow dimensions are controlled by the relative flow-rate of the sample liquid in relation to the flow-rate of the sheath flow in which it is injected. At higher relative flow-rates, the sample liquid penetrates further into the sheath liquid thereby increasing the sample flow height.

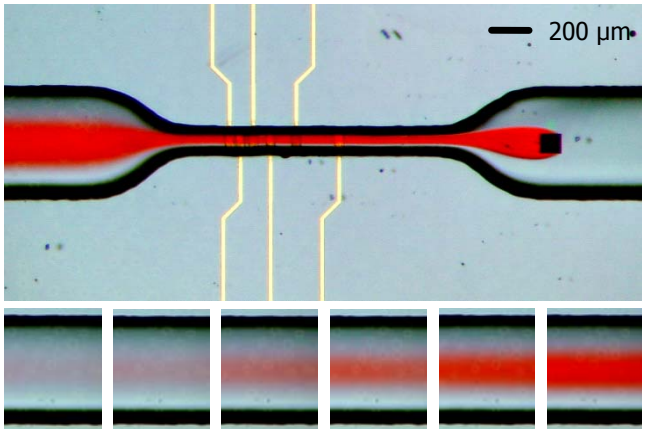

Fig. 2: Photographs illustrating vertical sample control; for increased sample flow-rates, the sample flow gets higher and the dye becomes more visible.

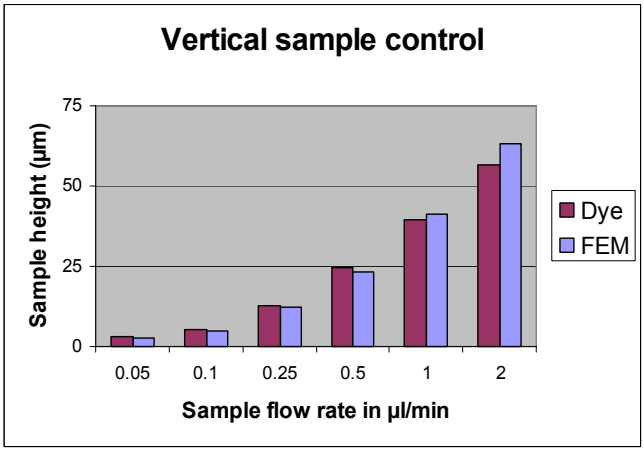

Fig. 3: Numerical data from measurements (dye) and simulation (FEM) for vertical sample flow control (sheath flow-rate constant at 10 µl/min).

The system was designed with help of simulations using the FEM-software package Coventorware. A series of measurements with a red dye was carried out to verify the simulation results. In the physical experiments, numerical data was obtained from the color information of photographs that were taken with a digital camera.

Some illustrative results are depicted in Fig. 2, and an overview of simulation and experimental results is depicted in Fig. 3. There is a very good match between both results. Fig. 4 demonstrates that not only the height, but also the complete distribution of sample matches very well.

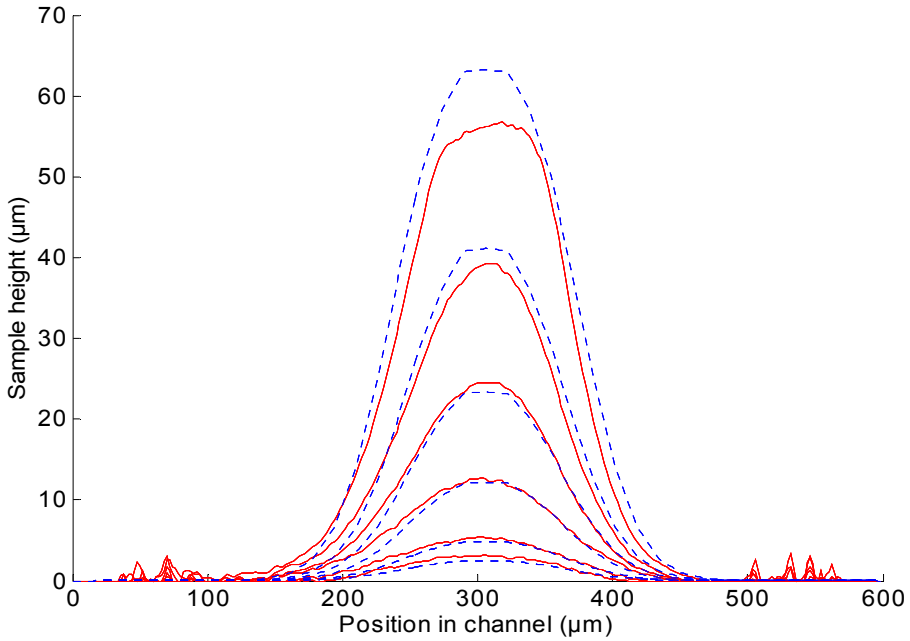

Fig. 4: Complete sample profiles for the same vertical sample flow control experiments as in Fig. 3 (dye: solid lines, FEM: dotted lines) demonstrating the good correspondence.

Horizontal Control of the Sample Flow Dimensions

The horizontal sample control is achieved by adding or removing liquid through two control inlets (see Fig. 1), located just down-stream of the sample inlet. Again, experimental results are compared with FEM-simulations. Some photographical results are depicted in Fig. 5. In Fig. 6, an overview of FEM and experimental results is depicted. The experimental and simulation results for the control of the horizontal dimensions show good correspondence.

Conclusions

A novel flow-cell with dynamic, orthogonal control of the sample flow dimensions has been presented that combines the advantages of large diameter and small diameter micro-channels. Experimental results on both vertical and horizontal control match very well with FEM-simulations. This allows predicting and controlling sample flow dimensions over a broad range of sizes and height-width ratios.

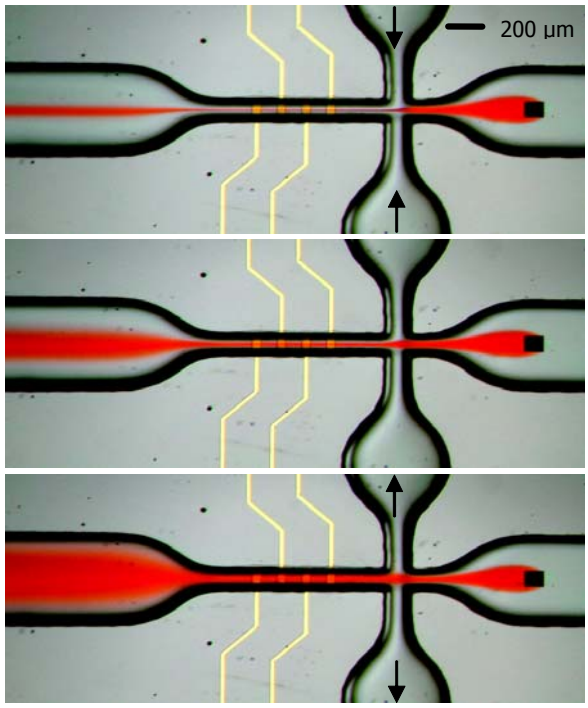

Fig. 5: Photographs illustrating horizontal control; adding liquid through the control inlets makes the sample flow less wide (top); removing liquid through the control inlets makes the sample flow wider (bottom).

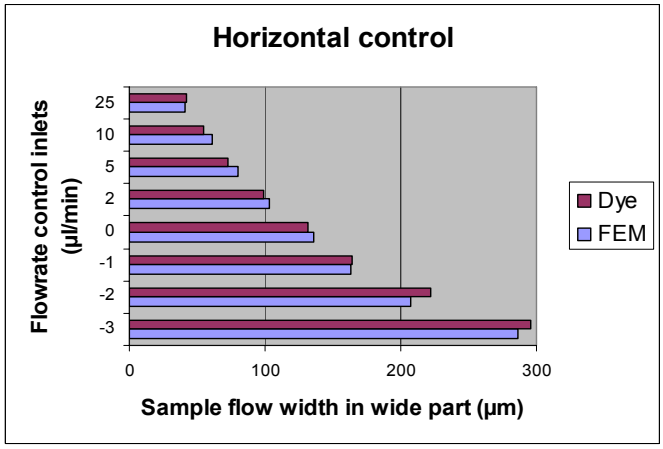

Fig. 6: Numerical data from measurements (dye) and simulation (FEM) for horizontal sample flow control (sheath and sample flow-rates constant at 1 and 10 µl/min, respectively).

Acknowledgements

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Micromachined Mixing Device for FTIR-Spectroscopy

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Time-resolved FTIR-spectroscopy is a powerful method for the investigation of chemical reactions, especially in the field of biochemistry. It allows obtaining structural information of molecular dynamics. This method requires fast mixing of at least two reactants as well as a very short optical pathlenght because of the strong IR-absorption of water and organic solvents. To meet these requirements a micromachined mixing device was developed which combines fast diffusion-based mixing and an optical pathlenght of less than 20 µm. The devices are batch fabricated on 4" CaF_2 wafers.

Introduction

Time-resolved Fourier transform infrared spectroscopy is an efficient technique to study chemical reactions and obtain structural information of molecular dynamics [1], [2]. This method requires fast mixing of the reactants. Additionally, the event under study must be precisely repeatable to provide a good signal/noise ratio. Water and organic solvents show a very high absorption in the mid-IR range, therefore the optical pathlenght of the device has to be very short, typically less than 20 µm. The principle of the mixing device is shown in Fig. 1.

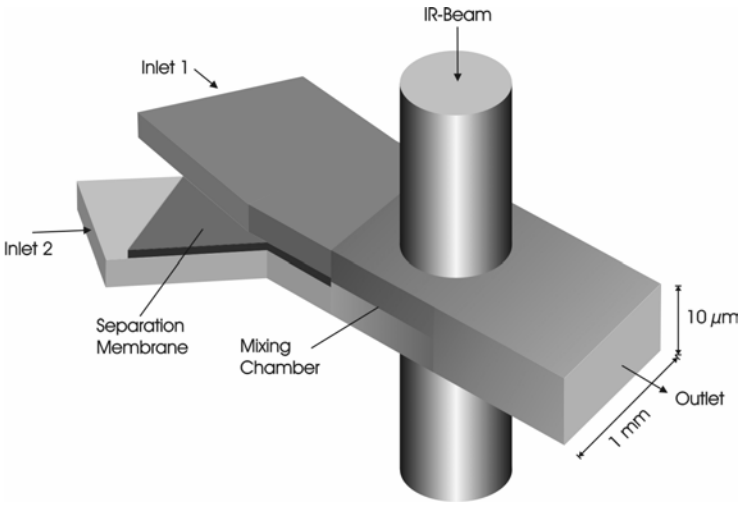

Fig. 1: Schematic drawing of the micromixer (drawing not to scale).

The mixer is operated in the “stopped flow” mode. Two liquids are injected by means of a double piston syringe pump into inlet 1 and inlet 2. These two streams are separated by a metal separation membrane until they enter the mixing chamber. Inside this chamber the liquids form two thin sheets which are superimposed. While the flow is on there is hardly any mixing due to laminar flow conditions in microfluidic devices. As soon as the flow is stopped, which is done by means of a dedicated fluidic setup [2], the liquids are mixed by diffusion. Diffusion is a rather slow process; therefore, the distances have to be kept as short as possible. Fluid dynamic simulations performed with FLUENT V5.5 showed as a result a mixing time of 100 ms for water based solutions. The height of the mixing chamber was 20 µm [1]. The mixing chamber of the latest device is 10 µm high, therefore one can assume a mixing time of ~25 ms.

Preparation of the Mixing Device

The devices are fabricated using micromachining methods like photolithography and waferbonding. As a substrate material, we use CaF_2 because of its superior optical properties. The fluid channels are formed by two layers of the negative-working epoxy based photoresist SU-8. During the last years, this material has been widely used because of its very good mechanical and chemical properties.

The devices are built up as follows: A 4 µm thick layer of SU-8 is deposited by spin coating, softbaked, exposed, post-exposure-baked, but not developed. On top of this layer, a 2 µm thick layer of Ag is deposited by evaporation. This metal layer is then covered by positive photoresist AZ 1512 HS. The photoresist is patterned as usual and the Ag-layer is etched to obtain the structure of the “separation membrane” (see Fig. 1). As an etchant a 45 % (WT) solution of $Fe(NO_3)_3$ in water is used. This solution does not attack the SU-8. Finally, the SU-8 is developed with PGMEA. To dissolve unexposed SU-8 under the metal structure takes quite some time (approx. 2 hours for channels of 1 mm length). Wafer #1 (the “bottom” wafer) now carries the structures of Inlet 2 and the separation membrane.

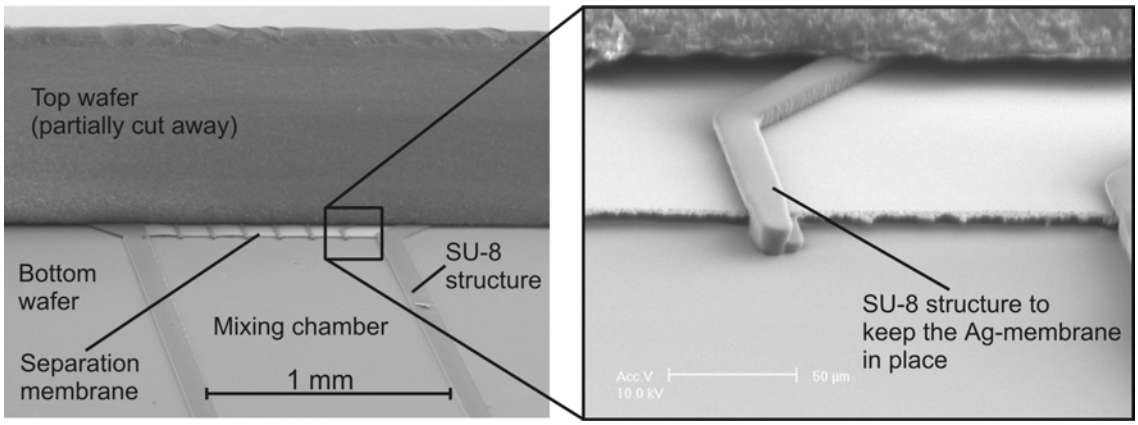

Fig. 2: SEM-micrograph of the mixing device. The top wafer is partially cut away to show the SU-8-structures and the separation membrane.

On wafer #2 (the “top” wafer) the structure of inlet 1 is fabricated as usual from a 4 µm thick layer of SU-8. This wafer contains the holes for two inlets and one outlet per mixer. These holes are conventionally drilled by means of a high-speed spindle attached to a computer-controlled mill. So far, the SU-8 on both wafers is not hardbaked and therefore the polymer is not completely crosslinked. Both wafers are superimposed face to face, and aligned. Hardbaking is done in an EVG 501 wafer bonder. A force of

1700 N is applied and the wafers are heated to 200 °C for 1 hour. Because of this high temperature, the polymer is completely crosslinked and a bond is established between SU-8 and the opposite Ag structure (see Fig. 2).

The stream of liquid from inlet 1 flows between the top wafer and the separation membrane, the stream from inlet 2 flows between the separation membrane and the bottom wafer. At the edge of the membrane the streams meet and enter the mixing chamber (see Fig. 3).

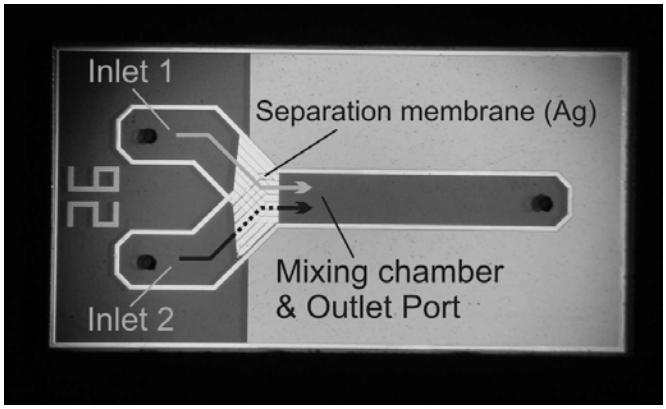

Fig. 3: Micrograph of the mixing device after dicing. The dimension of the device is 6 x 12 x 2 mm^3.

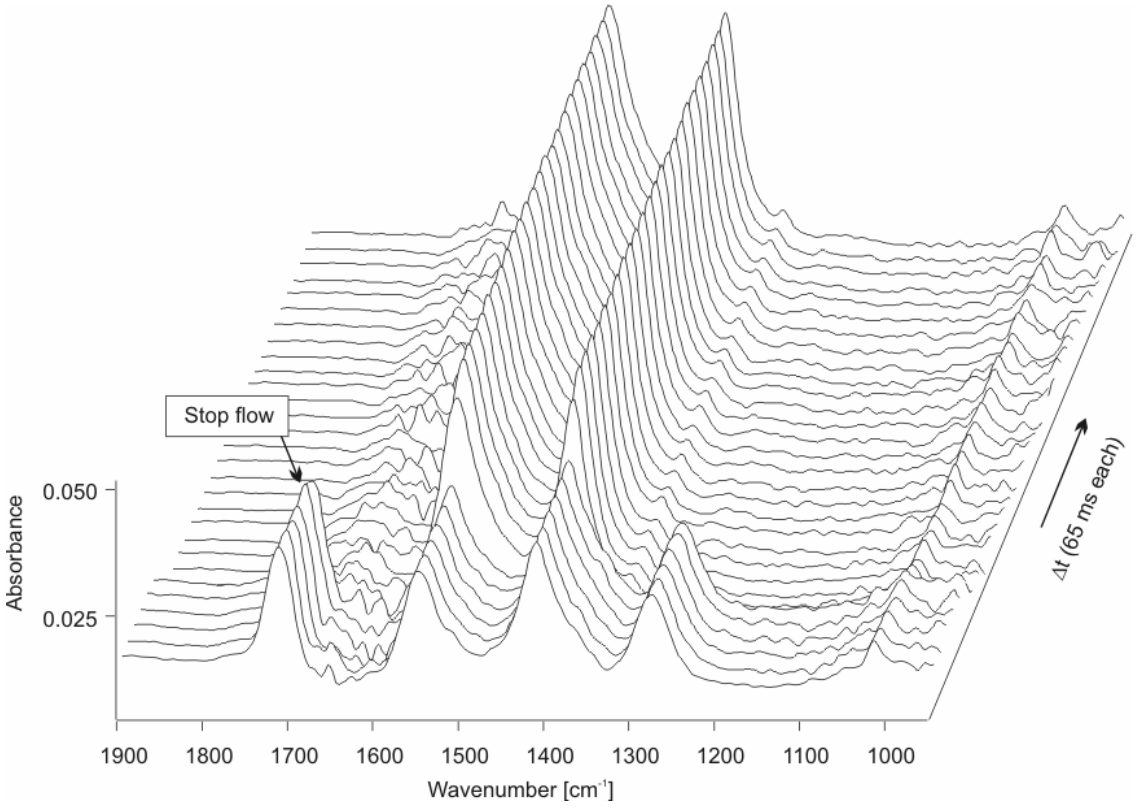

Fig. 4: Stack plot of FTIR spectra obtained from the reaction of CH_3COOH and NaOH. Time delay between subsequent spectra is 65 ms.

Results Obtained from Model Reactions

If reactants are used which react very fast, the reaction is limited by diffusion only. Consequently, in this case the experiment is actually a test of the mixer performance (see Fig. 4). It can be observed clearly that the mixing time meets the result of the CFD simulation. Some premixing (i.e. formation of reaction product) can be observed while the flow is on. Premixing cannot be neglected in case of very fast reactions [1]. In case of a slow reaction no formation of the reaction product can be observed, as shown in Fig. 5. This reaction is completed after a few hundred milliseconds.

Conclusion

The micromachined mixing device presented in this paper offers the opportunity to investigate the dynamics of chemical reactions, especially in the field of biochemistry [3]. The results of the CFD simulations were confirmed by experiments. To realize this device a special technique was developed that combines 2 layers of SU-8 photoresist and 1 layer of metal. This technique is useful for the fabrication of other microfluidic devices as well. The devices are produced in a batch process using 4-inch wafers of Calcium Fluoride, a material that shows very good optical properties.

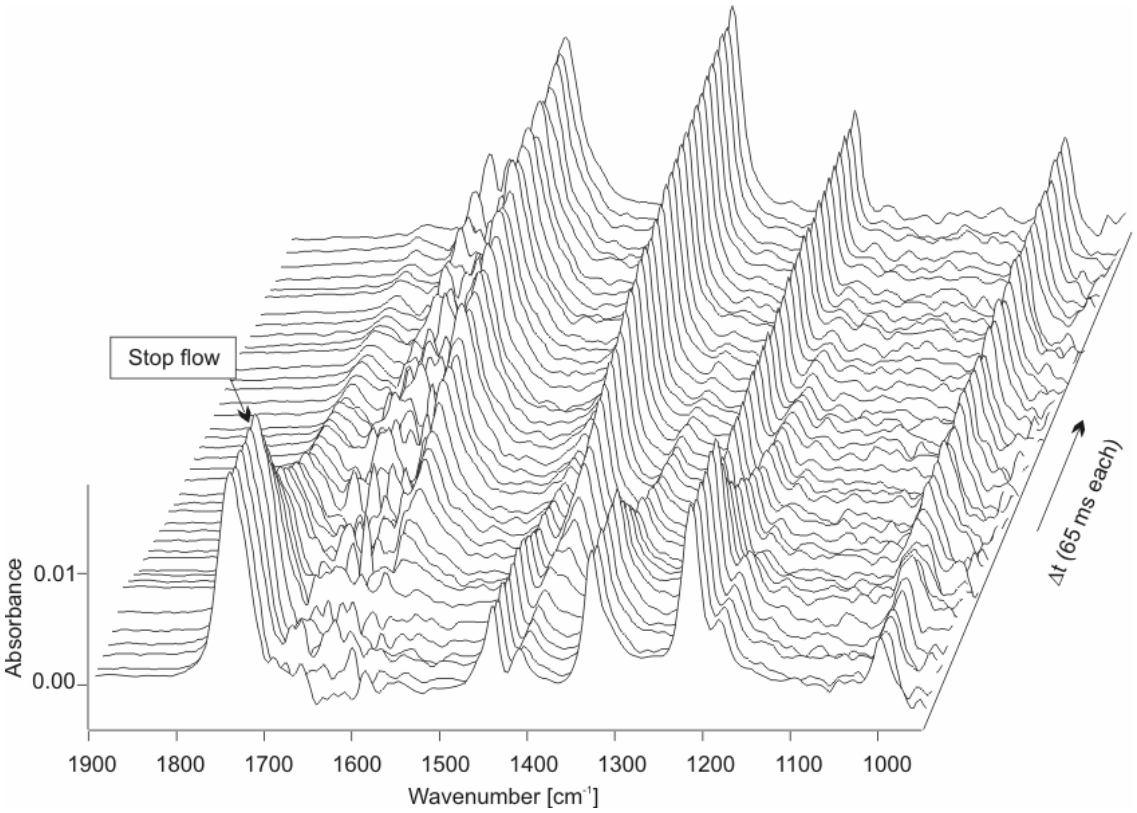

Fig. 5: Spectra obtained from the reaction of methyl monochloroacetate and sodium hydroxyde. Time delay between subsequent spectra is 65 ms.

Acknowledgement

This work was supported by the Ludwig Boltzmann Institute of Biomedical Microtechnology, Vienna.

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ESD Protection Devices (Posters)

Study of Internal Behavior of BCD ESD Protection Devices under TLP and Very-Fast TLP Stress

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The internal behavior of BCD npn electrostatic discharge (ESD) protection devices is analyzed experimentally and by simulation. The device internal thermal and free carrier density distributions during TLP and vf-TLP stresses are studied by a backside transient interferometric mapping technique. Two current paths, one through a lateral npn transistor and one through a vertical npn transistor, are identified. The current flow along the width of the devices is homogeneous. This explains their high ESD ruggedness.

Introduction

The automotive industry requires protection against both the human body model (HBM) and the charged device model (CDM) electrostatic discharge stresses [1, 2]. Monitoring of the internal thermal behavior in such devices is significant for the understanding of device reliability and failure mechanisms [3, 4].

The transient interferometric mapping (TIM) technique is a powerful tool for the investigation of internal device behavior and provides information on thermal and free-carrier concentration dynamics and spatial distribution during an ESD event.

In this paper we investigate the internal device behavior of a bipolar-CMOS-DMOS (BCD) technology ESD protection device under 100 ns TLP and 10 ns vf-TLP stresses.

Device and Measurement Technique

Lateral npn ESD protection devices implemented in an 0.8 µm smart power process (BCD4) are studied. A simplified cross section of the device is shown in Fig. 1. The emitter/body contact was grounded and positive polarity pulses were applied to the collector contact during the investigations.

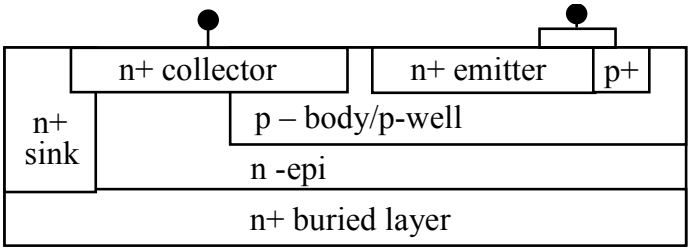

Fig. 1: Simplified cross sections of the studied device.

The high current IV characteristics were measured using 100 ns TLP and 10 ns vf-TLP pulsers.

The backside TIM is carried out by a scanning heterodyne interferometer setup [5]. An infrared laser beam of 1.3 µm wavelength is focused from the backside on a device and scans the device. The temperature and free-carrier induced phase shift of the reflected beam is then interferometrically detected. If the thermal effect dominates the measured phase shift $\Delta\varphi$ can be directly related to the two-dimensional thermal energy density E_{2D} in the device via the relation: $E_{2D}(x,y,t) = 0.88\ \Delta\varphi(x,y,t)$ (nJ/µm^2, rad) [6]. The phase shift is measured with 1.5 µm space and 3 ns time resolution.

Experimental Results

Figure 2 shows the high current IV characteristics of the device of width 100 µm measured by 100 ns TLP and 10 ns vf-TLP. The IV curve obtained by TLP bends from the IV obtained by vf-TLP at currents above 2 A, i.e., the differential resistance (R_{diff}) is higher for TLP stress. This can be attributed to a self-heating effect. The R_{diff} of the device at current levels below 2 A is the same for both TLP and vf-TLP types of stress. The $1/R_{diff}$ scales nearly linearly as a function of the device width in this range as can be seen in Fig. 3.

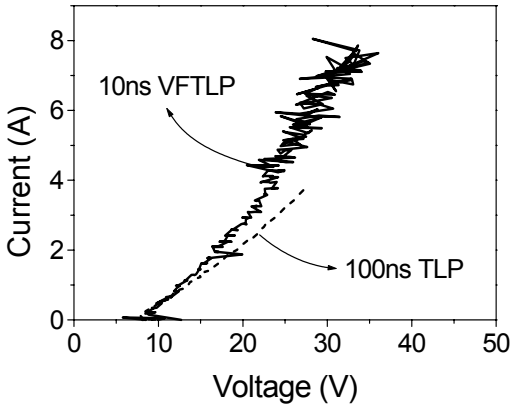

Fig. 2: High current IV characteristics of the device of width 100 µm measured by 10 ns vf-TLP and 100 ns TLP (after [4]).

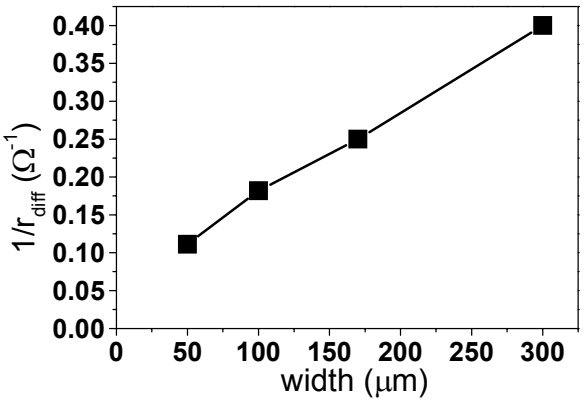

Fig. 3: Inverse differential resistance $1/R_{diff}$ as a function of device width (after [4]).

The ESD ruggedness of the device is high. The 170 µm wide device can sustain 4 A of TLP and 18 A of vf-TLP stress levels. These are the measurement setup limits.

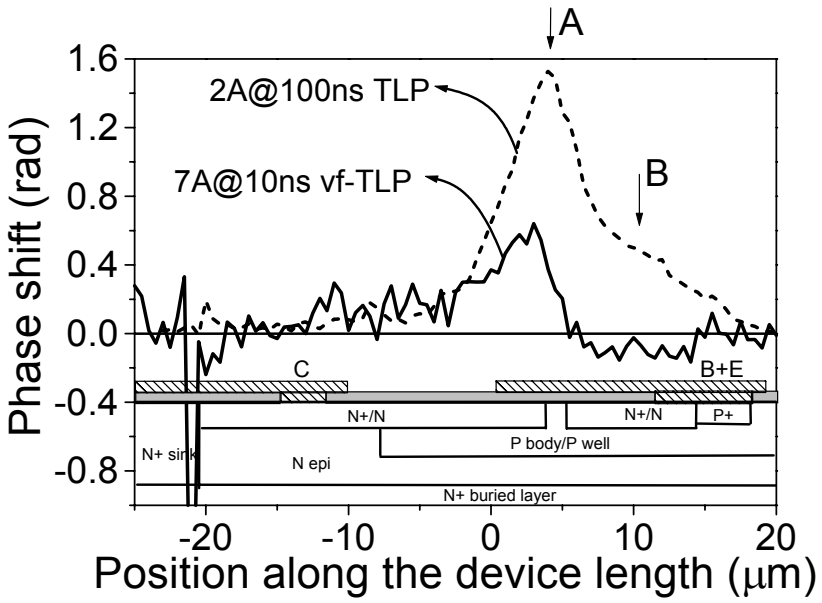

Fig. 4: Phase shift distribution along the device length measured at the pulse end of stresses of 2 A @ 100 ns (TLP) and 7 A @ 10 ns (vf-TLP). Aligned simplified cross section is also indicated (after [4]).

Figure 4 shows the phase shift distribution along the device length at the pulse end of two stress conditions: 100 ns TLP pulse with amplitude of 2 A and 10 ns vf-TLP pulses with amplitude of 7 A. An aligned simplified cross section of the device is also shown in Fig. 4. A dominant positive phase shift peak is located at the collector edge of the lateral npn transistor during both TLP and vf-TLP stresses (see A in Fig. 4). This peak arises from the heat dissipation in the reverse biased n^+-collector/p-body pn junction, which undergoes impact ionization. Another important area is located at the position of the n^+-emitter (see B in Fig. 4). The phase shift at the end of short vf-TLP stress is negative there. It arises from the increased free carrier concentration due to injection in the forward biased n^+-emitter/p-body junction, when the npn transistor is turned on. One can therefore expect also a positive phase shift due to heating related to the activity of a vertical npn transistor being present under the n^+-emitter. However, the temperature rise at pulse duration of 10 ns is insufficient to make the total phase signal positive. A positive thermal side-hump related to the heating in the vertical npn transistor can only be observed under longer pulses, as it can be seen on the phase shift profile measured at the end of a 100 ns long TLP stress pulse (see B in Fig. 4).

The activity of the vertical npn transistor depends on the stress current level. The phase shift distributions along the device length at three different TLP stress current levels are shown in Fig. 5. Let us concentrate on side hump (peak B in Fig. 5). It can be observed only at higher stress levels (I > 2 A). The phase shift peak B is more pronounced at the device corners, compared to the middle of the device. This can be seen on the measurements at I = 4 A, where the phase shift distribution is taken in the device middle (curve “M” in Fig. 5) and at one corner of the device (curve “C” in Fig. 5).

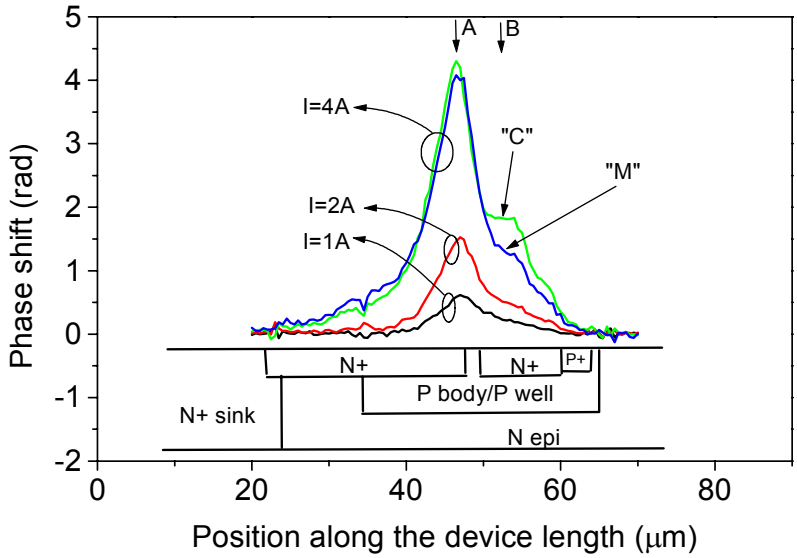

Fig. 5: Phase shift distribution along the device length as a function of TLP stress current. The inset shows a simplified device cross section (after [3]).

Homogeneity of the current flow along the width of the devices stressed by 10 ns vf-TLP pulses was also investigated. Figure 6 shows the phase shift distribution along the dominant hot spot (peak A in Fig. 4) in the devices of different widths stressed by the same current per device width. The optical mapping reveals very homogeneous current flow thus explaining linear scaling of the inverse differential resistance $1/R_{diff}$ as a function of the device width (see Fig. 3) and the high ESD ruggedness of the devices.

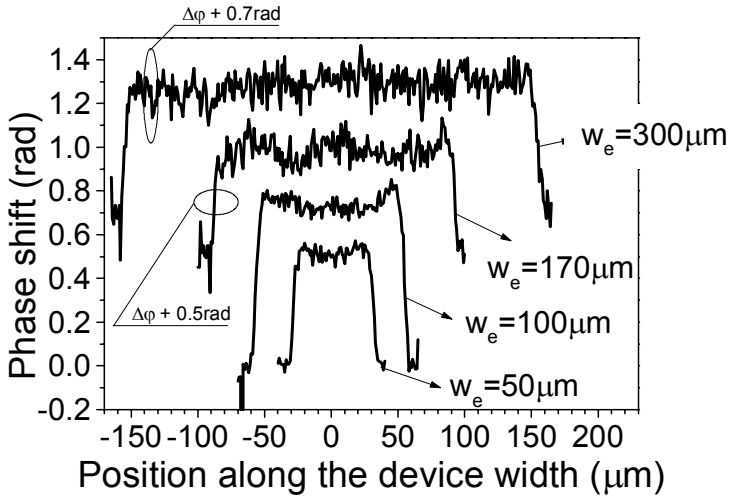

Fig. 6: Phase shift distribution at the end of stress 10 ns vf-TLP along the device width. The current density (current/width) was the same for all devices (after [4]).

Figure 7 shows the simulated heat dissipation in the device at t = 100 ns for the stress current pulse of 2.5 A. The main heat dissipation region is located at the lateral n^+-collector/p-body junction. This agrees with the experiment, because the dominant phase shift peak was observed at this place (see A in Fig. 4). The heat dissipating re-

gion is also observed at the n-epi/p-body junction under the n^+-emitter, which explains the existence of the side-hump observed experimentally at the end of 100 ns TLP pulses in this structure (see B in Fig. 4). This is the second region where the impact ionization takes place.

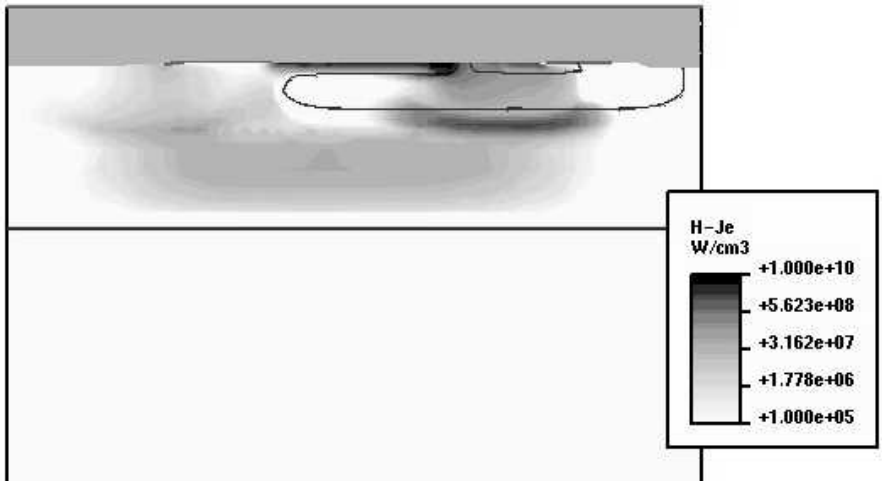

Fig. 7: Simulated heat dissipation due to electron current flow in the device at the end of 2.5 A @ 100 ns stress (after [4]).

Conclusions

The internal behavior of BCD ESD protection devices under TLP and vf-TLP stress was studied and compared. The device operation is dominated by the action of the lateral npn transistor. The n^+-collector/p-base junction of this transistor where impact ionization takes place was identified as the main heat-dissipating source. The activity of the vertical npn transistor is also identified in the device. The optical mapping along the device width has revealed homogeneous current flow. This is consistent with the scaling of the inverse differential resistance of the devices with their width. Thanks to the homogeneous current flow, devices also exhibit excellent ESD ruggedness in both HBM and CDM time domains.

Acknowledgements

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