Post-Process CMOS Channel Profile Tailoring With Focused Ion Beams

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This paper presents a novel approach of lateral profile engineering addressing sub-lithographic dopant spikes in the MOS channel region. In contrast to conventional approaches, our focused ion beam based method needs only one single dopant activation and damage anneal step avoiding unwanted effects like TED of the implanted species and broadening respective washout of the dopant profiles. We show the viability of this approach to engineer CMOS devices by *in situ* monitoring the impact of the ion beam on device performance, and we prove peak channel implants to gain devices with superior I_{on}/I_{off} ratios and enhanced short channel effect control.

Introduction

In order to overcome the leakage/I_{Dsat} tradeoffs and detrimental short channel effects (SCE) of MOS devices in the deep submicron regime, recent investigations focus on optimized MOSFETs incorporating sharp, sub-lithographic doping peaks, preferably at the source side of the channel [1]. As simulation studies explained [2], the I_{on}/I_{off} ratio of MOS devices can be greatly improved by the introduction of peaking channel dopings. These tripartite channel MOS devices (further on denoted TMOS) should be much less prone to hot carrier degradation due to reduced electric fields, and furthermore less affected by DIBL, thus being easier to scale into the ultra-deep submicron regime. The purpose of this work is to explore the FIB as a high resolution restructuring tool for front end prototyping.

Device Fabrication

In contrast to all work done up to now, in which the doping peaks were implanted during a baseline CMOS process [1] prior to the gate-oxide formation, we implement the doping peak at the very end of the front-end process.

By a masked through-gate implantation, thermal cycling can be reduced to the minimum necessary to eliminate damage and to guarantee dopant activation. The implantation peaks are located at the center of the channel (symmetric device indexed by s) and one quarter off the center (asymmetric device indexed by a) (Fig. 1).

The devices are fabricated relying on preprocessed, fully featured MOS devices with planar silicon gate technology, LDD structure incorporating n^+ polysilicon gates and 9 nm gate oxides. The effective channel length is 0.6 µm for p-MOS and 0.75 µm for n-MOS devices. These n/p-MOS devices are subjected to gallium and phosphorus implants via hard masks, yielding narrow p^+, respectively n^+ regions, dividing the channel into three sections (Fig. 1).

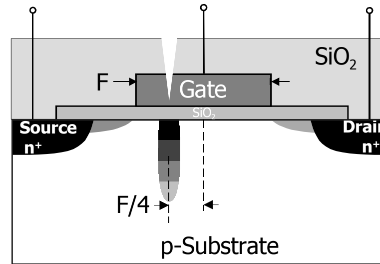


Fig. 1: Schematic of a tripartite n-channel MOSFET (n-TMOS) device with implantation hard mask in an asymmetric configuration.

The implantation windows are formed on top of the gate stack by means of a focused ion beam scheme. The TEM image in Fig. 2 shows a cross section of the implantation trench. All implantation windows for the devices have footprints below 30 nm, thus addressing a sufficiently small aspect ratio respective to the gate related feature sizes.

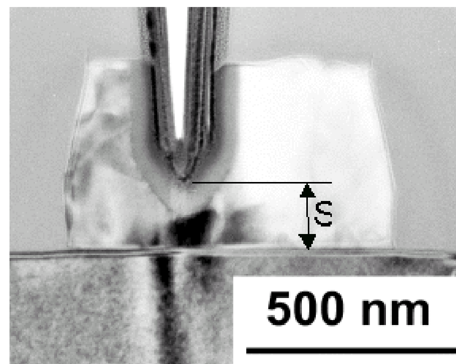
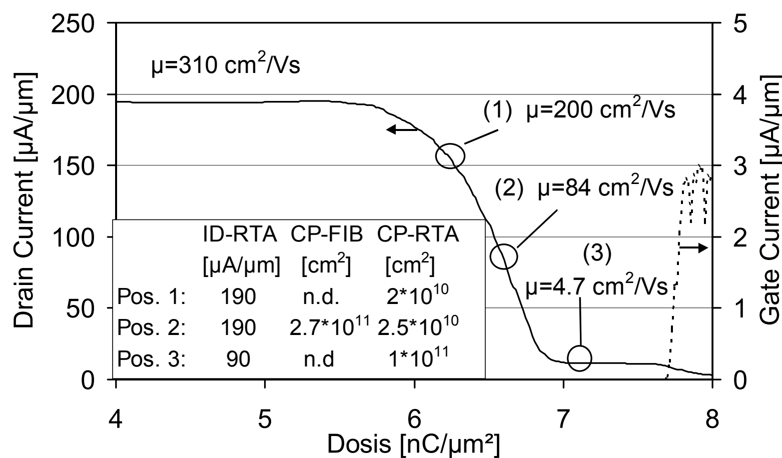


Fig. 2: TEM image of the TMOS with remaining gate seat S

The milling of the implantation trench with Focused Ion Beam is controlled by *in situ* electrical testing. Figure 3 exhibits the drain and gate current during FIB milling of the implantation trench.



	ID-RTA [μA/μm]	CP-FIB [cm²]	CP-RTA [cm²]
Pos. 1:	190	n.d.	2*10^10
Pos. 2:	190	2.7*10^11	2.5*10^10
Pos. 3:	90	n.d	1*10^11

Fig. 3: MOSFET degradation due to FIB milling ($V_G = V_{DS} = 3$ V).

Despite of the fact that the extension of the amorphous region is kept fairly distant to the interface, the transistor begins to degrade due to the decreases of the electron mobility in the disturbed channel region. Charge pumping measurements indicate the formation of interface traps as far as the gate seat approaches 300 nm. Position (2) in Fig. 3 marks the final milling depth with a minimum gate seat of 220 nm. Up to that point, the entire FIB induced damage could be annealed out by an RTA process, and all substantial transistor characteristics could be completely recovered.

Device (dopant)	D[ions/cm^2] E [keV]	V_{th} [mV]	I_{leak} [A/µm]	I_{Dsat} [µA/µm]	SS [mV/dec]
conv. n-MOS	none	509	$1x10^{-13}$	402	82
n-$TMOS_a$ (Ga)	$2x10^{13}$/300	1018	$3x10^{-15}$	319	98
n-$TMOS_s$ (Ga)	$2x10^{13}$/300	1025	$7x10^{-16}$	59	99
n-$TMOS_s$*)(Ga)	5e12/300	842	$5x10^{-14}$	318	103
conv. p-MOS	None	-729	$2x10^{-16}$	196	85,7
p-$TMOS_a$ (P)	$2x10^{13}$/180	-876	$4x10^{-18}$	163	84.6

*) n-TMOS with low dose peak implantation

Tab. 1: Device parameters: implantation dose and energy, threshold voltage, leakage and saturation currents, and the sub-threshold swing.

Electrical Results

Charge pumping was used to determine the interface state density and the residual damage after through-gate implantation and proper post-treatment. Figure 4 exhibits the efficiency of the RTA process for damage anneal.

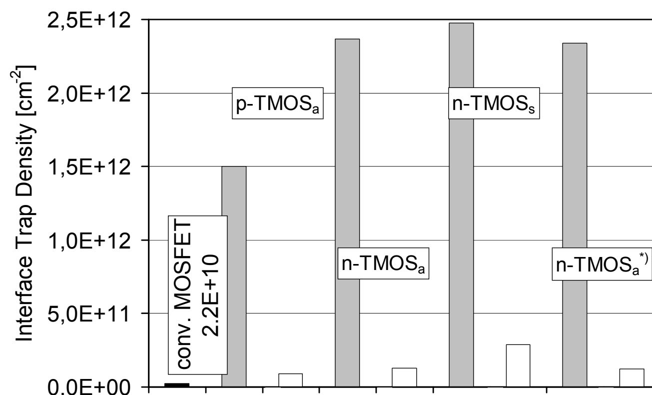


Fig. 4: Interface trap density of MOSFET and TMOS devices after through gate implantation (grey bars) and after RTA processing (white bars).

As expected, the interface trap densities correlate with implantation doses and with ion species, but depend evidently much stronger on the doping peak positioning within the channel. In the asymmetric case the damage cascades overlap with the highly doped S/D region, therefore part of the defects are electrically not detectable. The subthreshold characteristics shown in Fig. 5 exhibit regular behavior and show off-state leakage currents one to two orders of magnitude lower compared to the conventional MOS devices.

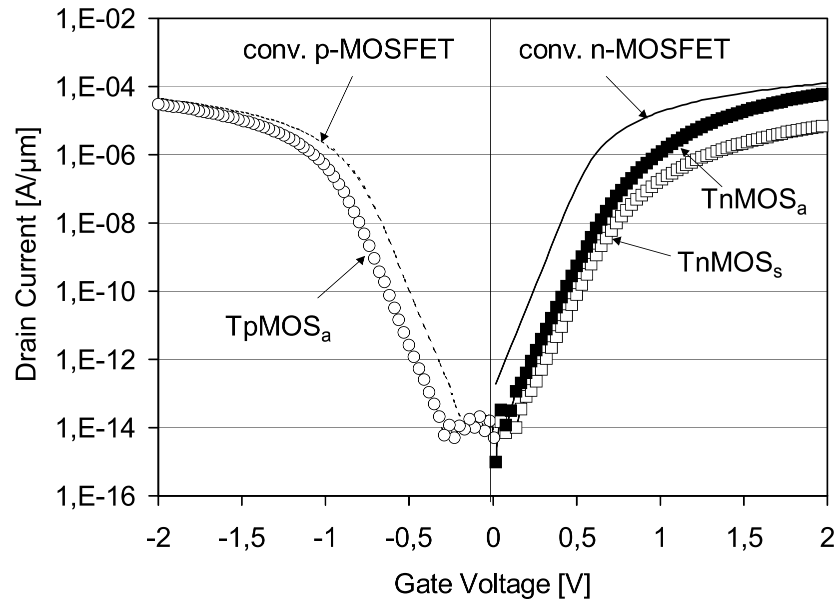


Fig. 5: Comparison of the sub-threshold characteristics for conventional MOSFET and TMOS devices (U_{DS} = 2 V).

The increase of threshold voltage is shown in Tab. 1. The gate drive characteristic in Fig. 6 exhibits the expected improve of the output resistance [1] of the TMOS device with even higher output currents for low gate voltages.

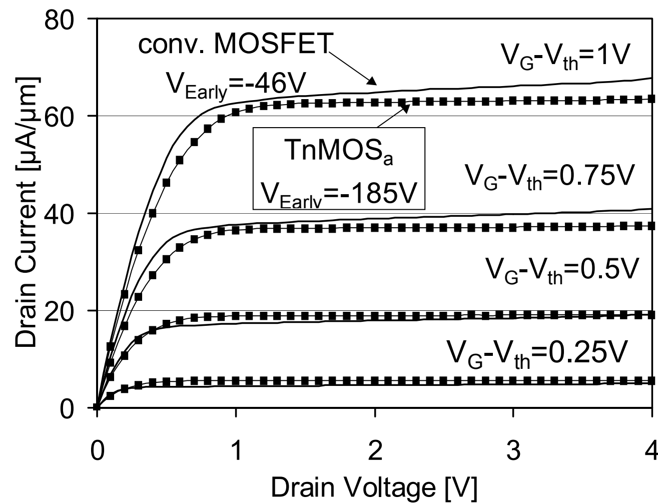


Fig. 6: Gate drive characteristic for the asymmetric n-channel TMOS$_a$ and conventional n-MOSFET device.

Beside the improved device performance, TMOS devices also exhibit enhanced SCE resistance, whereby the placement of the doping peak relative to the LDD extension junction is critical. Figure 7 exhibits the improved DIBL tendency of TMOS. Under reverse biasing conditions, the improved DIBL resistance is kept for the symmetric TMOS devices whereas for the asymmetric device the DIBL gets even worse.

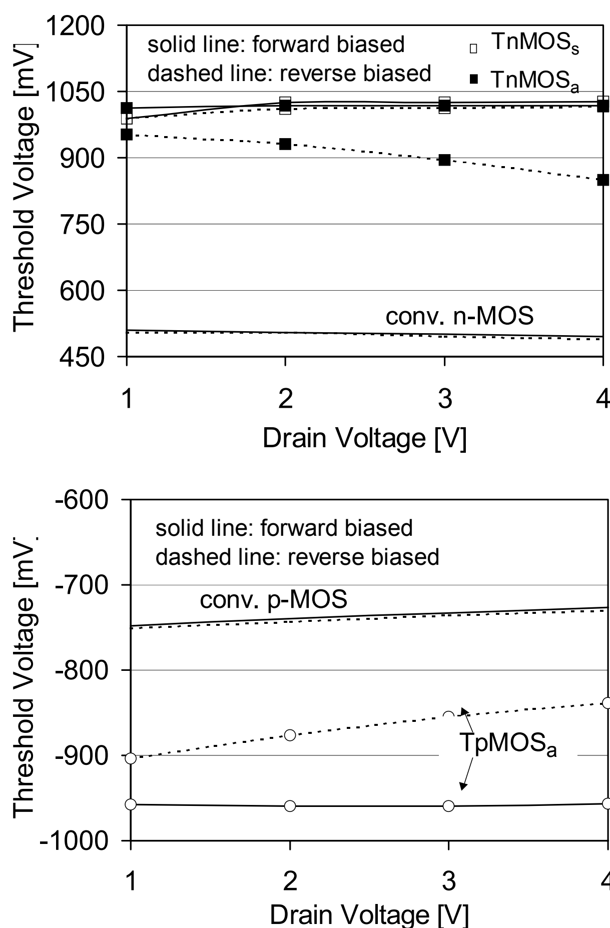


Fig. 7: V_{th}-V_D characteristics of n- and p-MOS devices.

According to the exponential dependence of hot electron degradation on the magnitude of the lateral drain electric field as predicted by simulation results [2] the I_{SUB}/I_{DS} ratio of n- as well as p-channel TMOS devices is 30% lower than that of the conventional MOSFET. The improved resistance to punchthrough of n- and p-TMOS devices is shown in Fig. 8.

Summary

This paper presents a novel technology of lateral profile engineering addressing tripartite channel MOS devices. For the first time MOS devices with highly nonuniform 2-D doping profiles are achieved by post-process implantation of channel doping peaks. In contrast to the conventional approach our focused ion beam based method needs only one moderate dopant activation and damage anneal avoiding unwanted effects like TED of the implanted species and broadening respective washout of the dopant profiles. We have shown, that post implantation can be successfully implemented to form TMOS devices with excellent I_{on}/I_{off} ratios and short channel effect control.

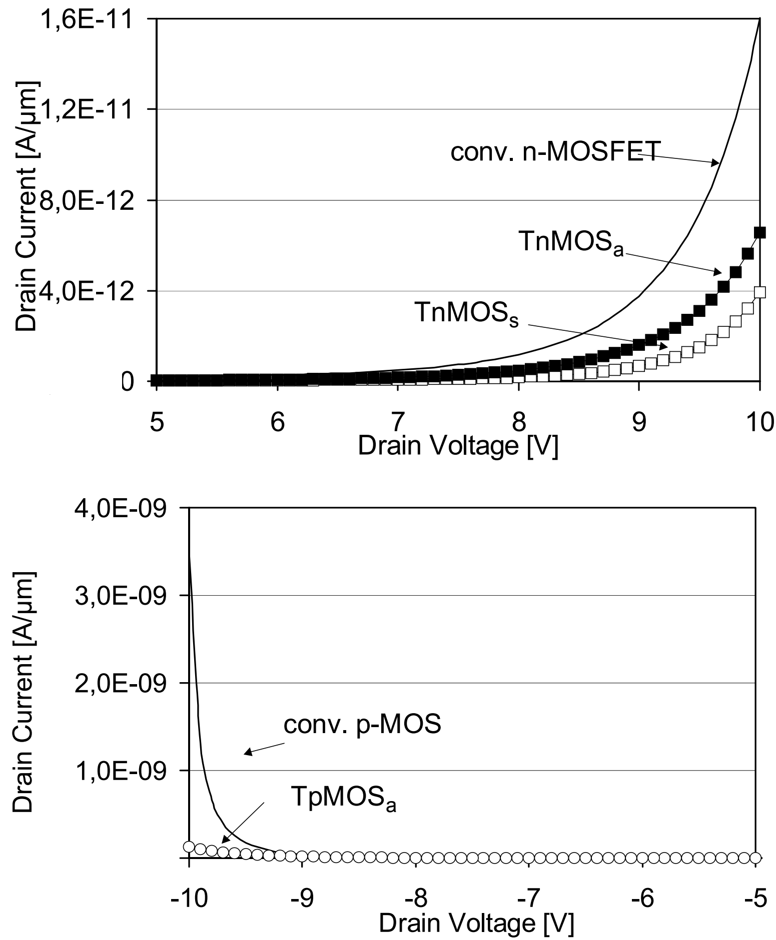


Fig. 8: Punchthrough characteristics of n-MOS devices.

References

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