Local Thermal and Current Imaging in Power Devices

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This paper summarizes recent results obtained at TU Vienna in the field of thermal and free-carrier mapping of semiconductor devices using backside transient interferometric mapping (TIM) technique. The technique is based on measuring optical phase changes due to temperature and free carrier induced variations in semiconductor refractive index. Scanning transient heterodyne and 2D holographic interferometers are used for phase measurements. Thermal distribution, hot spot dynamics, current filament movement, and failure mechanisms are investigated in electrostatic discharge (ESD) protection devices and power vertical DMOS transistors.

Introduction

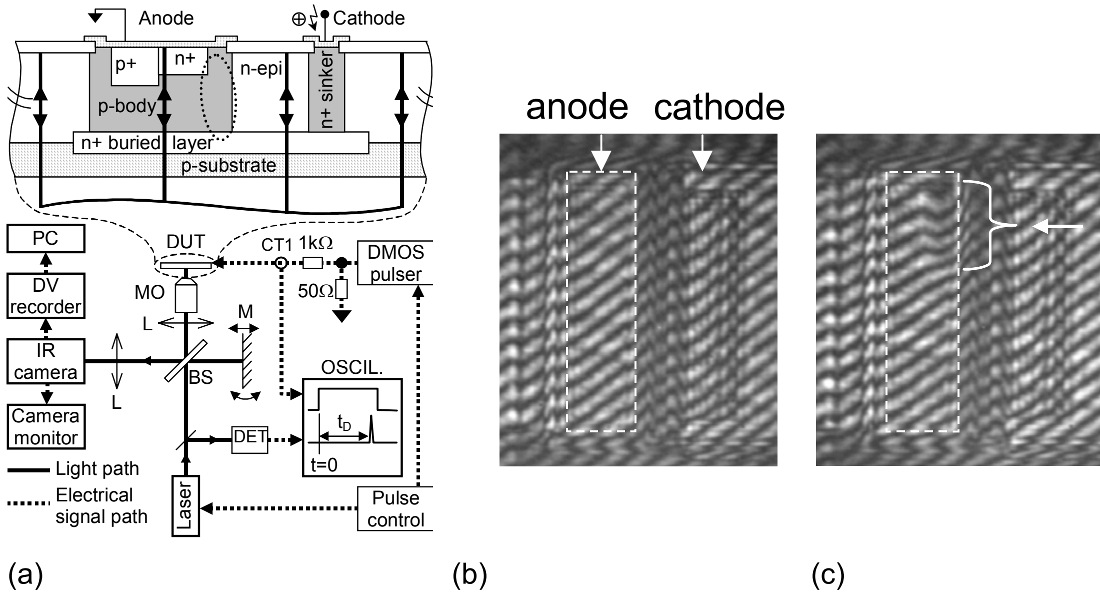
Experimental access to internal parameters of semiconductor devices as carrier concentration, current densities, power dissipation, temperature, etc. is of great interest for the understanding of device physics and for device optimization. Monitoring of temperature is especially important for power [1] and electrostatic discharge (ESD [2]) protection devices (PDs), where the self-heating effect is a main cause of device failure [3]. These devices operate at high current and power densities where the internal device behavior predicted by device simulation has a limited degree of confidence [4]. This is due to a lack of calibrated physical models at high temperatures. Thermal runaway phenomena in power devices occur in microsecond to millisecond time scale [1]. During an ESD event, large currents (1 – 10 A) and power densities (approx. 100 W) are dissipated in the device during 1 – 100 ns [2].

The backside transient interferometric mapping (TIM) technique has shown its potential in quantitative nanosecond thermal, free carrier and current flow mapping in silicon [5] – [8] and III-V [9] electronic devices and far-infrared quantum cascade lasers [10]. In this paper, recent development in the optical testing and analysis methodology is briefly reviewed. The application of TIM method to study hot spots and current filament dynamics in ESD and power DMOS devices is presented.

Experiments and Methodology

In the TIM method, an infrared non-absorbed laser beam (wavelength λ = 1.3 µm) probes temperature- or free carrier-induced changes in the semiconductor refractive index inside a device [5], [7]. The beam passes through the substrate, is reflected on the device topside and returns. The resulting phase shift is detected interferometrically. In a scanning heterodyne interferometer, a focused laser beam scans the device active area and the device is repetitively electrically stressed for each scan position [5]. Transient phase shift is obtained with 3 ns time resolution. A Michelson-like interferometer is used for phase measurements with 0.4 ns time resolution [11]. In a 2D holographic interferometric version of the TIM method, a broad beam illuminates the whole device area [6]. Figure 1 (a) shows a simplified arrangement of the setup. The phase profile is obtained by analyzing a 2D interference fringe pattern, see Fig. 1 (b), (c). The thermal image in the whole sample can be obtained using a single laser pulse, so non-

repeatable phenomena can be studied. The pulse width of 5 ns determines the time resolution. By varying the delay between the laser and stress pulse, the time evolution of thermal distribution can be obtained.



(a) (b) (c)

Fig. 1: Schematics of the 2D TIM method (a). Typical fringe interference pattern in an unstressed (b) and stressed (c) device. The deformation of fringes in (c) marked by an arrow results from local heating causing the phase rise; after [6].

It has been shown that if thermal effects dominate over the free carrier contribution, the measured phase shift $\Delta\varphi(x,y,t)$ can be directly related to a 2D thermal energy density E_{2D} in semiconductor according to the relation [7]:

$$\Delta\varphi(x,y,t) = \frac{4\pi}{\lambda\, c_V}\frac{dn}{dT}E_{2D}(x,y,t) \tag{1}$$

where c_V is the volume specific heat and dn/dT the thermo-optical coefficient. E_{2D} is a “memory” quantity representing the time integration of all the preceding power dissipation. The instantaneous 2D power dissipation density $P_{2D}(x,y,t)$, representing the well the current density if a constant voltage on the device is assumed, can be calculated according to [8]:

$$P_{2D}(x,y,t) = \frac{\lambda}{\frac{dn}{dT}}\frac{c_V}{4\pi}\frac{\partial\Delta\varphi(x,y,t)}{\partial t} - \frac{\lambda}{\frac{dn}{dT}}\frac{\kappa}{4\pi}\left(\frac{\partial^2\Delta\varphi(x,y,t)}{\partial x^2} + \frac{\partial^2\Delta\varphi(x,y,t)}{\partial y^2}\right) \tag{2}$$

where κ is the thermal conductivity.

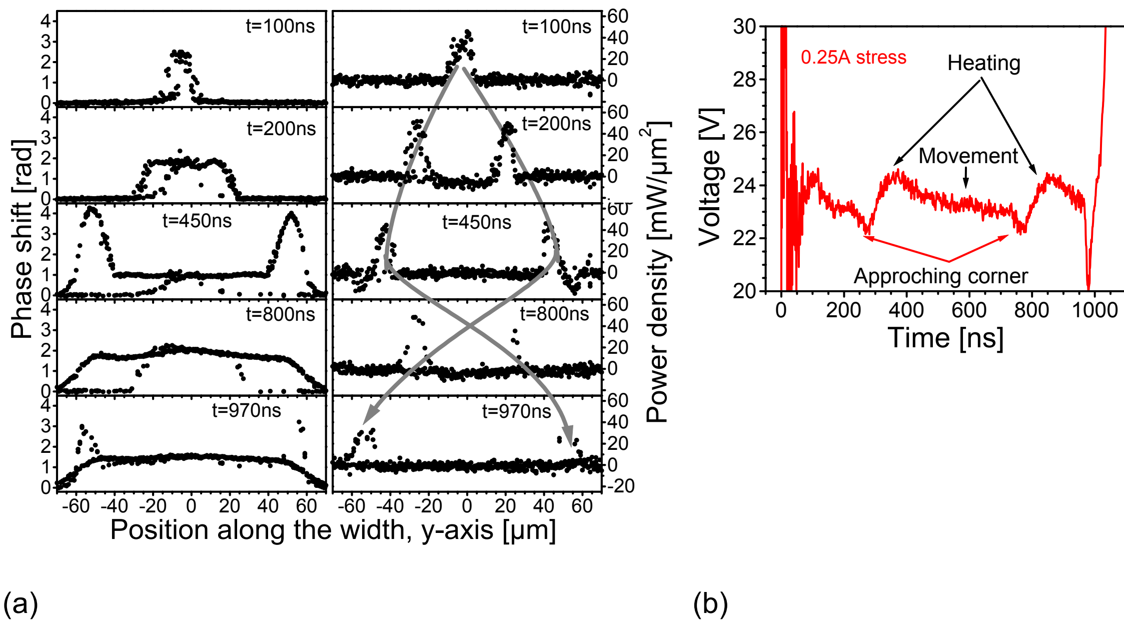
Smart power ESD and vertical power DMOS devices have been investigated. The devices have a common n^+ buried layer serving as collector of a parasitic npn transistor. The devices were stressed by rectangular current pulses of 100 ns – 1 µs duration. If not specified elsewhere, this drives the devices in a bipolar snapback mode.

Results

The dynamics of current flow in ESD PDs has been studied by analyzing the absolute phase shift itself (representing the temperature), the 2D power dissipating density P_{2D},

(representing the current density) and the device voltage waveform [12]. Strongly localized moving current filaments (see Fig. 2(a)) have been observed in devices exhibiting near zero or NDR part in IV characteristics. The filament characteristics, as starting place, size, speed, travelling mode and its occurrence probability depend strongly on stress magnitude I_S. The filaments exhibit pulse-to-pulse instability in their movement direction and position of origin, i.e. the device internal state differs from pulse to pulse. This is due to fluctuations in carrier densities.

At long pulses of low current magnitude the filament can several time travel over the device width without destroying the device, see Fig. 2(a). The filament passage over the device produces a specific fingerprint across the voltage on the device, see Fig. 2(b). When the filament approaches a region with higher impact ionization, e.g. at terminations, or when it passes from a hot region into a cooler region the voltage decreases due to negative temperature dependence of the impact ionization rate [13]. When the filament does not move, as it is initially in the middle and then at corners, the voltage increases due to the self-heating effect to keep the same impact generation rate under the constant current. When the filament moves, a constant voltage is typically observed, which is due to a stabilizing effect of the movement on the temperature in the filament. The filament localization and persistence is caused by fast cooling to lateral sides.



(a) (b)

Fig. 2: (a) Scatter plot of measured phase shift (left) and extracted P_{2D} at several time instants in a silicon controlled rectifier device exhibiting moving filaments at current of 0.15 A. The filament path is marked by the gray lines with arrow. The scattered nature of data is due to pulse-to-pulse instability in the filament movement. (b) Voltage waveform related to the filament movement; after [12].

At higher stress currents, the number of filamentary modes typically increases. Figure 3 shows the 2D thermal distribution at high stress levels, demonstrating the spreading of current flow with time. The high-energy input in the filament exceeds the energy output by cooling to lateral sides. This causes that the current density decreases with time, which leads to a current homogenization or spreading with time [6]. Similar effects have previously been observed indirectly by repetitive photon emission measurements [14].

The speed of the current filaments and of the filament spreading increases with time and with the stress current I_S, see inset of Fig. 3(d). This effect, beneficial for ESD ro-

bustness, is due to a negative temperature dependence of impact ionization rate [13]. The pulse-to-pulse instabilities in the device internal behavior leads to formation of a pattern in IV curves when plotting the IV curve point by point without time or ensemble averaging [12].

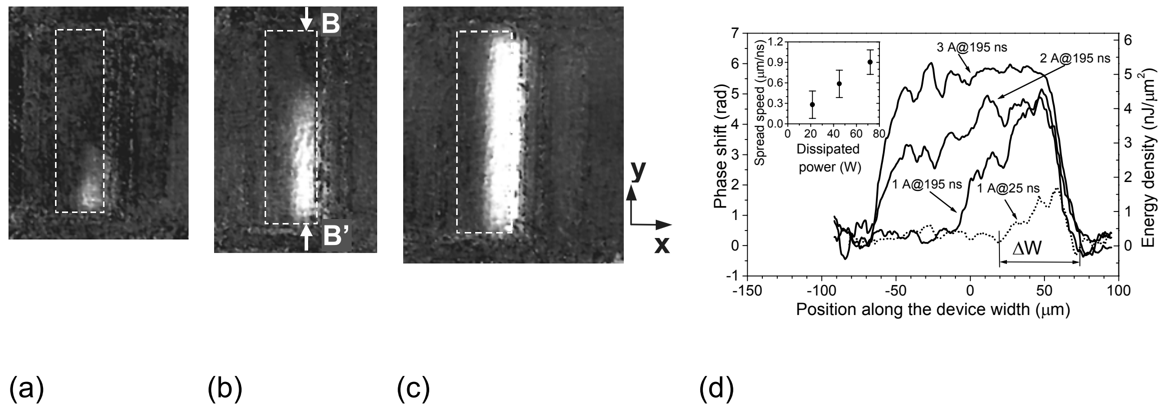


Fig. 3: Single shot 2D phase profiles in a ESD protection device demonstrating the spreading of current flow with time and I_S: (a) 1 A @ 40 ns, (b) 1 A @ 195 ns, (c) 3 A @ 195 ns. (d) Phase profiles along the B-B' line in (b). Inset: Filament spreading speed as a function of I_S; after [6].

Vertical DMOS transistors with different number of cells were investigated before [15] and in bipolar snapback operation [16], [17] using TIM method. Before snapback, the current sharing between the cells is homogeneous, due to a negative thermal feedback during the avalanche breakdown [15]. Under snapback conditions, the current flow is strongly inhomogeneous, forming localized current filaments, see Fig. 4. The cells at the drain terminations are triggered first due to higher electric field there. With time the neighboring cells trigger as well, causing that the current flow moves toward the device area or along the termination (Fig. 4). The observed feature of DMOS behavior in snapback is qualitatively reproduced by 2D and 3D device simulation [16]. The base-push-out or Kirk effect and the negative temperature dependence of the impact ionization rate were found to play a decisive role in the cell-to-cell hoping of the current flow. This is plausible for ESD robustness.

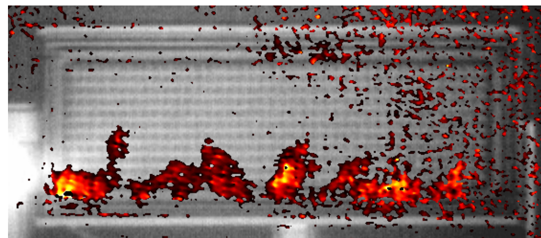
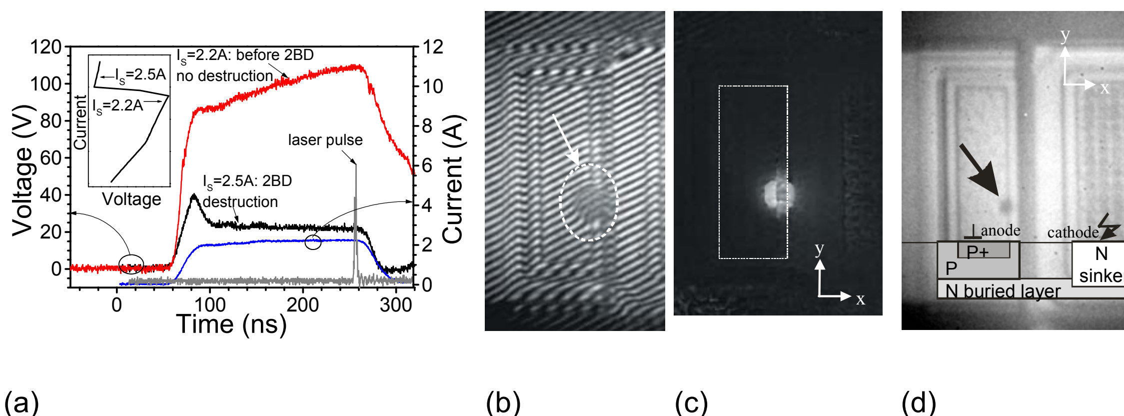


Fig. 4: Phase image in a 440 cell DMOS device recorded at time 150 ns after the beginning of a 7A current stress pulse. The phase image is aligned with the back-side infrared device image; after [16], [17].

Finally, failure mechanisms have been studied during single destructive pulses [18]. Fig. 5 shows the device interferogram and extracted phase shift in a diode structure, recorded during a single destructive 2nd BD event. At the destruction, the voltage across the device drops from the pulse beginning, indicating a current density driven instability, see Fig. 5(a). This leads to a formation of a current filament (see Fig. 5(c)),

whose size, taking into account the thermal diffusion length of 4.2 µm for a 200 ns long pulse, was estimated to be 3 – 4 µm. The diameter of the filament correlates with the size of permanent damage at this position (see Fig. 5(d)). A decreased intensity of the interference fringes was observed during this event (see Fig. 5(b)), which indicates the onset of band-to-band absorption (E_G reduction with temperature increase). Taking into account the data of temperature dependence of absorption coefficient for λ = 1.3 µm [19], the temperature in the filament was estimated to exceed 900 K.



(a) (b) (c) (d)

Fig. 5: Voltage waveform during the destructive event in a diode (a). Fringe pattern (a), extracted phase shift (b) and IR image with defect position (d), after [18].

Conclusion

Current filaments and hot spot dynamics has been investigated in ESD protection and DMOS devices. Using the single shot capability of TIM method, current flow instabilities and destructive mechanisms have been revealed. The movement and spreading of current filaments have been identified as a thermally driven process. The TIM method is a powerful tool providing the design engineer a unique insight into internal device behavior of semiconductor devices and to verify device simulation models.

Acknowledgements

Prof. E. Gornik, S. Bychikhin, M. Blaho, V. Dubec, J. Kuzmik and M. Litzenberger from FKE TU Vienna and M. Denison, N. Jensen and M. Stecher from Infineon Technologies are greatly acknowledged. This work was supported by EU IST Project DEMAND and FWF Wittgenstein award.

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