Using Extreme Sono-Effects to Improve on the Selectivity of Particle Removal to Microelectronic Structure Damage Below 65 nm

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Development work for the next generation of microelectronic devices, 65 and especially 45 nm, is under full steam, and major challenges for 32 nm and beyond are being tackled one-by-one by scientists and engineers working in pre-development, corporate and academic research centers. It seems that the red brick wall painted a couple years ago has become a little porous again as novel, sensitive substrates and materials finally find themselves being implemented or are close to introduction in the manufacturing process, e.g. strained silicon, high-k dielectrics, new silicides or maybe even metal gates. The excitement related to this seemingly everlasting move towards the ultimate nano-structured device however should not let us forget to explore in detail and understand the added process complexity and especially the increased requirements for contamination control and surface preparation.

In this presentation one major challenge microelectronic device manufacturers are facing will be especially highlighted: selective removal of nm sized particles without damage to equally or just slightly larger device structures. A novel approach to understand and improve on “physically assisted” chemical cleaning will be discussed.