Sensor Interface Electronics

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The importance of tailored electronic readout circuits in biosensing applications has in the past often been neglected. In this contribution we demonstrate the relevance of the issue considering a practical example of closely coupled co-design of micro- and nanosystems: a high-quality recording platform for single ion channel measurements on functionalized artificial lipid membranes.

Introduction

Ion-channels on cell membranes play crucial roles in physiology and pathophysiology and are important drug targets [1]. Microelectrode-based electrophysiological techniques which access the interior of a cell and can directly measure the minute currents through these channels have been employed in the past for the study of ion-channels.

The most successful of these techniques and the current golden standard is the patch-clamp technique [2]. Although traditionally performed manually and thus yielding very low throughputs in the order of 10 data points/technician/day, during the last decade several automated high-throughput screening (HTS) lab-on-a-chip systems have been proposed which have throughput rates going up to 20.000 data points/day [3]. The quality of the data produced by these systems is however not yet high enough to resolve single ion-channel currents in a repeatable manner.

Recording the sub-picoampere currents flowing through single ion channels in cell membranes with sub-millisecond resolution has up to date been difficult and often impossible due to both the limitations of the readout electronics and the difficulty of establishing a repeatable clean interface between the cell and the biosensor so as to form a so-called gigaseal. Yet, such recordings would yield valuable information in the study of the highly dynamic processes occurring upon e.g. channel gating or the membrane relaxation after potential steps and phase transitions and thus open way to significant advances in ion channel research.

In this paper we describe a low-noise amplifier design which is part of a planar patch-clamp chip being developed at our institute in cooperation with the Centre of Nanobiotechnology (CNB, University of Natural Resources and Applied Sciences, Vienna, Austria) for the recording of single ion channel currents on arrays of functionalized supported artificial lipid bilayer membrane (BLM) patches The topic of this contribution is the design of an amplifier for optimal noise performance to be employed in single ion channel current measurements.

Envisioned System

Together with the CNB [4] we are developing a low-noise single ion-channel recording platform in which an array of functionalized artificial lipid membrane patches with implanted ion channels will be patterned on a solid support (see Fig. 1) including provision for a clean interface to the electronic measurement setup.

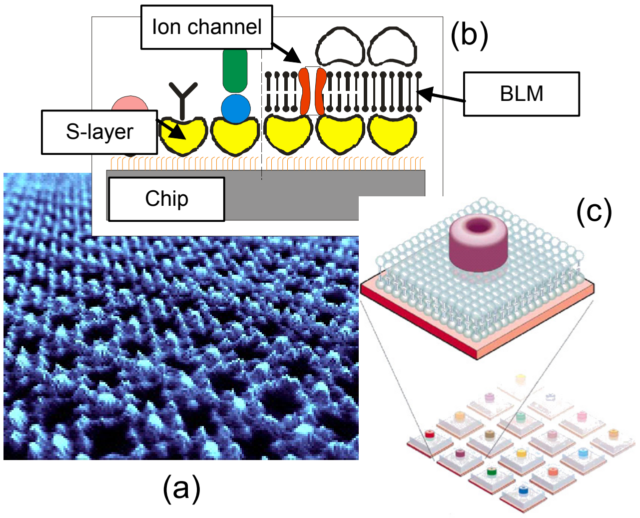


Fig. 1: Functionalized supported lipid bilayer membranes (BLM) [4]. (a) AFM of BLM support layer based on S-layer proteins. (CNB/BoKu), (b) and (c) schematic representations of respectively a supported BLM and an array of BLMs with implanted ion channels.

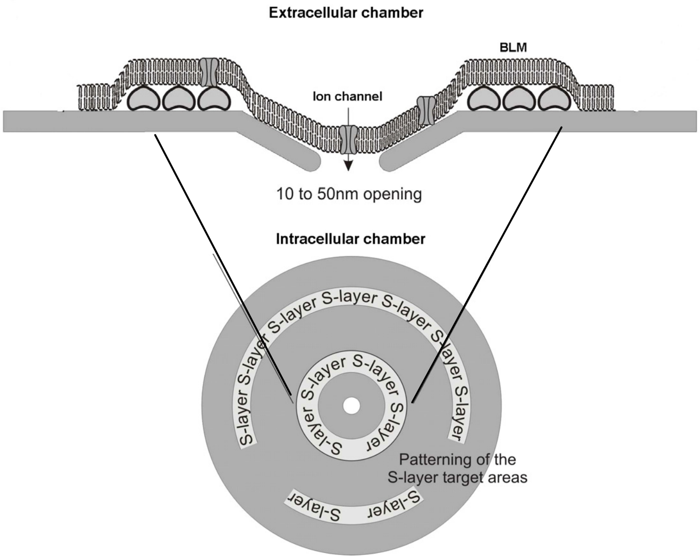


Fig. 2: Biomimetic cell-chip interface for improved adhesion of the cell membrane to the substrate so as to reach seal resistances in the order of 100 GΩ and above. Side view (top figure). Top view (bottom figure).

When looking at the minimization of noise, one of the most important features for high quality single ion channel recordings is a good seal between the intra and extracellular measurement chambers. Any current path having a conductance comparable to a single ion channel's conductance (1 – 150 pS) would generate an excessive amount of noise and lead to it being impossible to discern the minute signal current flowing through the ion channel from the noise generated by the leakage conductance.

On the one hand, we intend to improve the seal impedance by one order of magnitude when compared to traditional on-chip patch-clamp measurement setups so as to reach seal resistances in the order of 100 GΩ and above. For that purpose we will employ a biomimetic interface based on S-layer proteins (see Fig. 2). By providing conditions which closely match the cell's natural environment, we expect the adhesion to the substrate to be vastly improved thus yielding better quality seals.

On the other hand, low-noise electronics need to be delivered, which will amplify the low-power signals to more robust levels that may easily be transported off-chip for further processing. The design of such an amplifier is the subject of the following section.

Optimal Low-Noise Amplifier Design

In the quest towards studying singular ion channels artificially implanted into engineered BLM patches having widths and lengths in the range of a few hundred nanometers, the need arises for optimal interfacing between the biosensor and the readout electronics.

In order to reach input-referred noise levels well below 100 fA in a band from 0 to 20 kHz, one must necessarily match the amplifier's input stage to the source impedance. An electrical lumped-element model corresponding to a membrane patch including the seal impedance and the access resistance is given in Fig. 3. This impedance is seen to be mainly capacitive in the frequency range of interest.

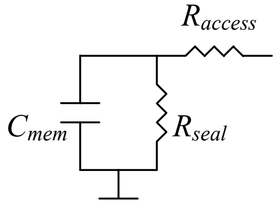
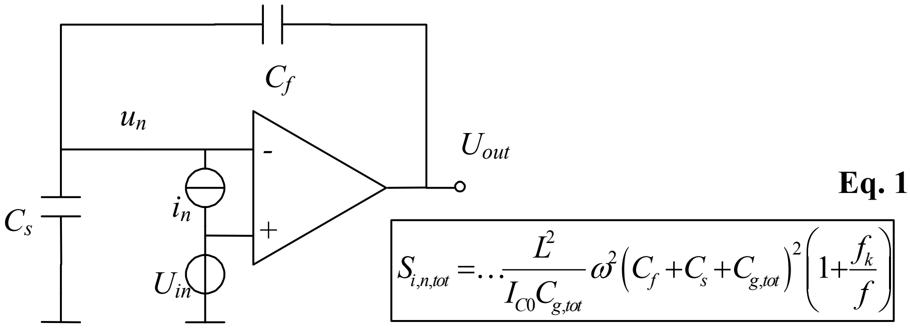


Fig. 3: Lumped element model of a membrane patch. C_{mem} has a typical density of 1 µF / cm^2, for the 1 µm^2 patches we are targeting $C_{mem} \approx 10$ fF. A good seal will have resistances of $R_{seal} > 100$ GΩ and R_{access} will typically be a few MΩ. For the frequencies of interest, the one dominant component is C_{mem}.



Eq. 1

$$\boxed{S_{i,n,tot} = \ldots \frac{L^2}{I_{C0} C_{g,tot}} \omega^2 \left(C_f + C_s + C_{g,tot}\right)^2 \left(1 + \frac{f_k}{f}\right)}$$

Fig. 4: Feedback configuration including noise sources u_n and i_n. Equation 1 shows the dependence of the total input-referred noise current power spectral density with C_s, C_f, the total gate capacitance $C_{g,tot}$, the gate length of the input transistor L and the inversion coefficient I_{C0}. One can see that L should be chosen to be minimal, the transistor should biased deep in strong inversion and $C_{g,tot}$ should be equal to $C_f + C_s$

One possible feedback configuration for the amplifier would be the transimpedance amplifier shown in Fig. 4. Notice that capacitive feedback has been used in order to eliminate noise contributions stemming from the passive elements. The main source of noise thus comes from the amplifier itself and is originated mainly by the drain noise current. It can be modeled by the two equivalent sources i_n and u_n at the amplifier's input port (see Fig. 4), where it can be shown that i_n is proportional to $C_{g,tot} = C_{gs} + C_{gd}$ and u_n is inversely proportional to $C_{g,tot}$. Both noise sources have a component stemming from the drain current's thermal noise and another due to its 1/f noise. The thermal noise component is minimized for a minimal gate length L, $C_{g,tot} = C_f + C_s$ and when the input stage is biased deep in strong inversion ($I_{C0} >> 1$, see Equation 1 in Fig. 4 and Fig. 6).

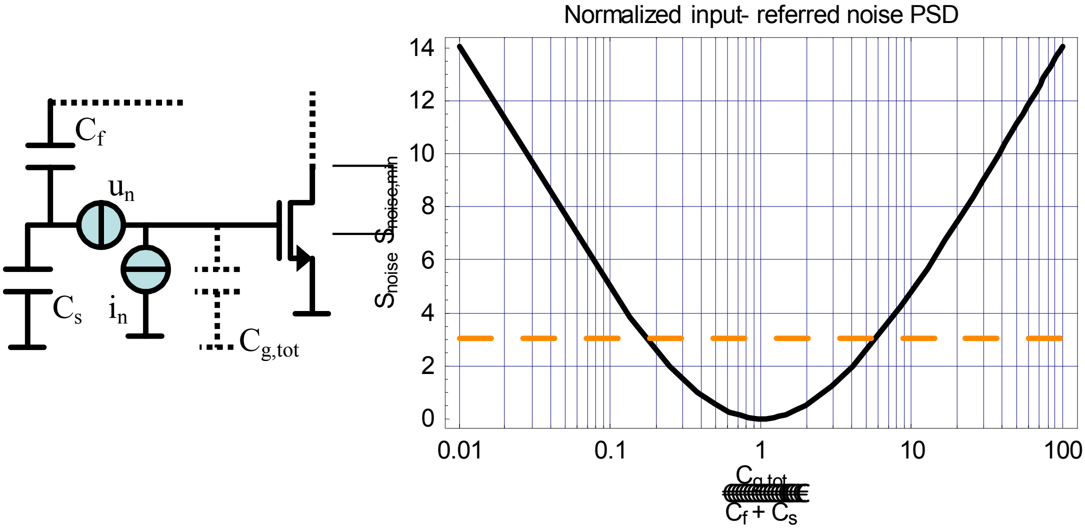


Fig. 5: Normalized input-referred noise power spectral density (PSD) as a function of the ratio of the input stage's capacitance ($C_{g,tot}$) and the sum of the feedback and source capacitances (C_f+C_s).

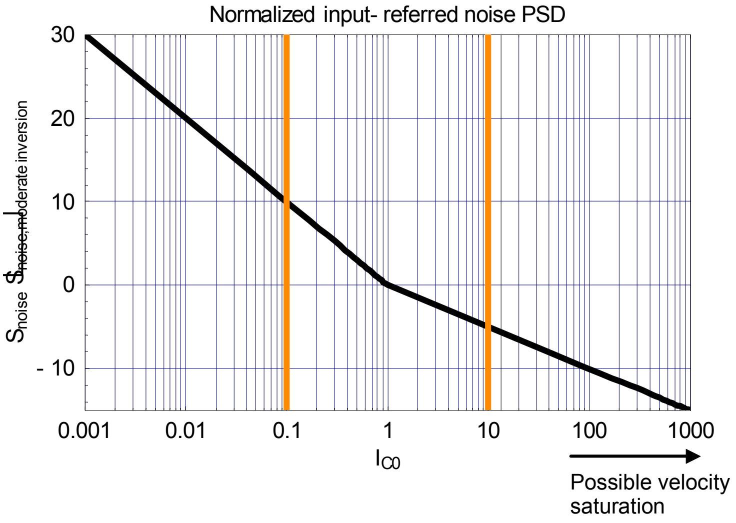


Fig. 6: Normalized input-referred power spectral density (PSD) as a function of the inversion coefficient (where I_{C0} = 1 corresponds to the center of moderate inversion)

For the very small source capacitances corresponding to nanosized BLM patches, the optimal input stage transistor sizes will thus become very small, consequently yielding an increase in 1/f noise. In order to reduce the 1/f noise component, the autozeroed architecture depicted in Fig. 7 has been employed [5]. It uses an auxiliary amplifier for reducing the 1/f noise component of the main amplifier and has the advantage that both input terminals of the main amplifier are permanently usable, as needed for the feedback configuration depicted in Fig. 4. On phase Φ_2, the auxiliary amplifier autozeroes itself in order to become a very low-offset amplifier which is subsequently used for measuring the main amplifier's offset and 1/f noise, canceling it via a low-frequency feedback path.

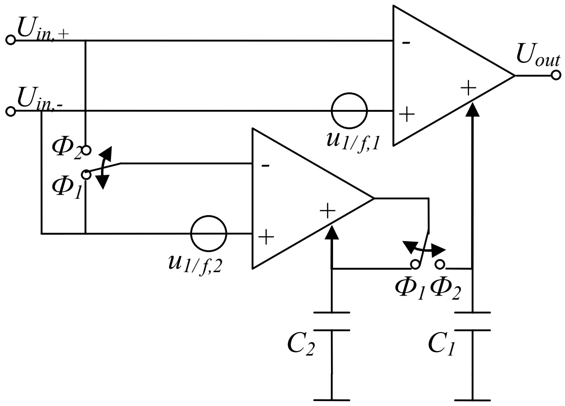


Fig. 7: Autozeroed amplifier. Both the main and the auxiliary amplifiers have an additional control input for offset cancellation. $U_{out}=A\ (U_{in+} - U_{in-}) + A_{Az}\ U_{1/f}$. On phase Φ_1 the auxiliary amp autozeroes itself, thus becoming a very low offset sense amplifier for the main amp's offset voltage which is detected on phase Φ_2. The control voltages are held on capacitors C_1 and C_2 respectively during phases Φ_1 and Φ_2 respectively.

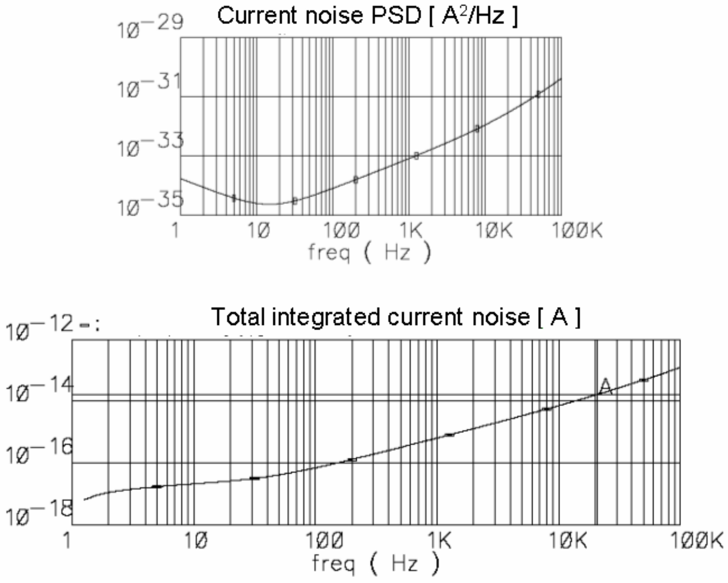


Fig. 8: Simulated noise power spectral density (top) total input-referred noise current. Results obtained with periodic noise analysis using Spectre RF simulator. At 20 kHz a total inband noise of 16.4 fA was obtained.

Simulation results show that it is possible to reach noise levels of about 17 fA for 1 µm x 1 µm patches using a standard 0.8 µm CMOS process from austriaMicrosystems (see Fig. 8).

Conclusion

The design of a low-noise amplifier for optimal noise performance to be employed in a state-of-the-art recording platform for the measurement of sub-picoampere currents flowing through single ion channels implanted on artificial lipid bilayer membrane (BLM) patches has been presented. The resulting amplifier features a simulated total inband noise of 16.4 fA in a band spanning from 0 to 20 kHz, which represents about one order of magnitude improvement in noise performance when compared to current state-of-the-art patch-clamp amplifiers.

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