Degradation Mechanisms in AlGaN/GaN HEMTs under Electrostatic Overstress

J. Kuzmík, M. Blaho, S. Bychikhin, D. Pogany, E. Gornik

Institute of Solid State Electronics Vienna University of Technology, A-1040 Vienna

P. Javorka, P. Kordoš

Institute of Thin Films and Interfaces, Research Centre Jülich, Jülich D-52425, Germany

We study degradation mechanism in AlGaN/GaN HEMTs under 100 ns long rectangular current pulses applied on the drain contact. Devices were dc characterized after consecutive current stresses. We observed a sudden increase of source and drain resistances after the stress of 1.65 A. We used a backside transient interferometric mapping technique to localize the current path in the device during stresses. We revealed a current filamentation during stresses and dark spots formation in the position corresponding to filaments occurrence. We assume electron injection into the device buffer layer and an electromigration on contacts.

Introduction

Devices may face electrical overstress events (EOS) during manufacturing, handling or device operation. Typical current pulses are in the ampere range with duration between nanoseconds and microseconds. The importance of a failure mechanism study in III-nitride transistors is given by their potential usage as power devices in many defense and commercial applications where harsh environment conditions can be expected. It was previously suggested that the electrical conduction mechanism in AlGaN/GaN HEMTs during EOS might be linked to the avalanche-injection processes in the GaN buffer layer [1]. On the other hand, the device's ohmic and Schottky barrier contacts degradation was revealed as the main mechanism responsible for the failure of Al-GaN/GaN HEMTs after EOS [2].

Experimental

The AlGaN/GaN HEMT structures used in this study were grown on both-sides polished sapphire wafer by MO-VPE. The device processing included e-beam lithography [2], the gate geometry was 50 µm width, 450 nm length. We used a transmission line pulser (TLP) to stress the device. In the TLP technique a coaxial cable (TL) with a 50 Ω characteristic impedance is charged by a voltage source and afterwards is discharged by closing a relay, providing rectangular current pulses for our devices. Devices were characterized after consecutive current stresses of increasing level. Ohmic contact and open channel resistances were extrapolated from the functional dependence of the source-drain resistance on gate voltage [3]. We used backside interferometric mapping (TIM) technique [4] to localize the current path (dissipated power) in HEMTs during TLP stresses. The mapping was performed using an infrared laser beam scanning the device from the backside. The measured phase shift, caused by the temperatureinduced change in the refractive index, is directly proportional to a local 2D energy density in the device [4].

Results and Discussion

The HEMT drain-source high-current pulsed *I-V* characteristics exhibit S-shape with three regions (see Fig. 1): A low-current / high-impedance region A, a NDC region B, and a high-current / low-voltage region C. A parasitic bipolar effect [1] may be linked to the S-shape.



Fig. 1: Typical drain-source high-current pulsed *I-V* curve of the HEMT. The inset illustrates the band diagram and assumed process of the hole accumulation and electron injection into the GaN buffer (after [1]).



Fig. 2: Evolution of the AIGaN/GaN HEMT threshold voltage, open channel resistance and source + drain resistances values in dependence of previous current stress level (after [2]).

Transistor threshold voltage V_{τ} , open channel resistance R_0 , and the sum of the source R_s and drain R_D ohmic contact resistances as a function of the current stress level are shown in Fig. 2. The ohmic contacts' catastrophic degradation (ten-fold increase from the nominal value) was recorded at $I_{stress} = 1.65$ A. The abrupt $R_s + R_D$ increase is accompanied with a partial increase of the open channel resistance R_0 . However, R_0 becomes marginal in comparison to $R_s + R_D$ at this point.



Fig. 3: Phase shift distributions of the AlGaN/GaN HEMT along the drain and source at *I_{stress}* = 0.25 A at the end of the pulse. Source was grounded for a scan along the drain and vice versa. Inset: Schematic device layout with indicated scan lines (after [2]).



Fig. 4: Backside infrared camera view of the AIGaN/GaN HEMT after *I_{stress}* = 0.25 A on the (a) drain, (b) source. Arrows mark dark spot (DS1 – 3) appearance, laser beam indicates the position of the maximal phase shift signal (after [2]).

Results of the TIM technique are presented in Fig. 3. The device was scanned along the stressed contact with a step of 7 μ m. First, the source was grounded and the drain was stressed with a positive pulse. The phase shift characteristics show a fair local maximum at the right edge of the HEMT. Following the change of the stress polarity (drain grounded, source stressed), two new maxima appeared in new positions close to the previous one. These observation correlates with the backside infrared images of the device (Figs. 4 (a), (b)) where dark spot positions correspond to the phase shift maxima on the grounded (opposite) contact.

Conclusion

The AlGaN/GaN HEMT behavior and degradation mechanisms under pulsed overstress conditions have been investigated. The current filament formation and the electromigration effect were shown to be responsible for the *ohmic* contact dark spot formation. Dark spots may be considered as a precursor of the *ohmic* contact degradation. Semiconductor material parameters are not changed substantially during the EOS event.

References

- [1] Kuzmík J., Pogany D., Gornik E., Javorka P., Kordoš P., "Electrostatic discharge effects in AlGaN/GaN HEMTs", Applied Physics Letters, Vol. 83, 2003, pp. 4655 – 4657.
- [2] Kuzmík J., Pogany D., Gornik E., Javorka P., Kordoš P., "Electrical overstress in AlGaN/GaN HEMTs: study of degradation processes", Solid-State Electronics, Vol. 48, 2004, pp. 271-276.
- [3] Shur M., GaAs Devices and Circuits, New York and London: Plenum Press, 1987. p.369-372.
- [4] Pogany D., Bychikhin S., Fürböck C., Litzenberger M., Gornik E., Groos G., Esmark K., Stecher M., "Quantitative internal thermal energy mapping of semiconductor devices under short current stress using backside laser interferometry", IEEE Trans. Electron Dev Vol.49, 2002 pp. 2070-2079.