New Materials and Devices for Future Generation CMOS Technologies

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Introduction

New materials and devices will be needed to continue the performance scaling for future generation CMOS technologies. The introduction of high mobility channel materials (e.g. Ge, strained Si, and III/V) on a Si-based platform, or the implementation of high-*k* and metal gate materials into the MOS-stack will be necessary to achieve the scaling goals as given in the International Technology Roadmap for Semiconductors (ITRS) [1]. In general, the transistor performance can be enhanced by (i) reducing the channel length (scaling), (ii) increasing the carrier mobility μ, or by (iii) reducing the oxide thickness (increasing C_{ox}). New materials and device concepts are necessary to address the concepts mentioned above. Point (i) is still realized by the classical scaling approach, but in future technology generations new device geometries such as FinFETs or nanowires may be of advantage (see also Fig. 1); (ii) μ can be increased by using strain and high-mobility channel materials, and (iii) is already in production at Intel© by introducing the high-*k*/metal gate approach [2]. In this work, we present an overview of such materials and devices, including high-*k*/metal gate technology on high-mobility substrates such as Ge or strained Si, as well as new device geometry concepts.

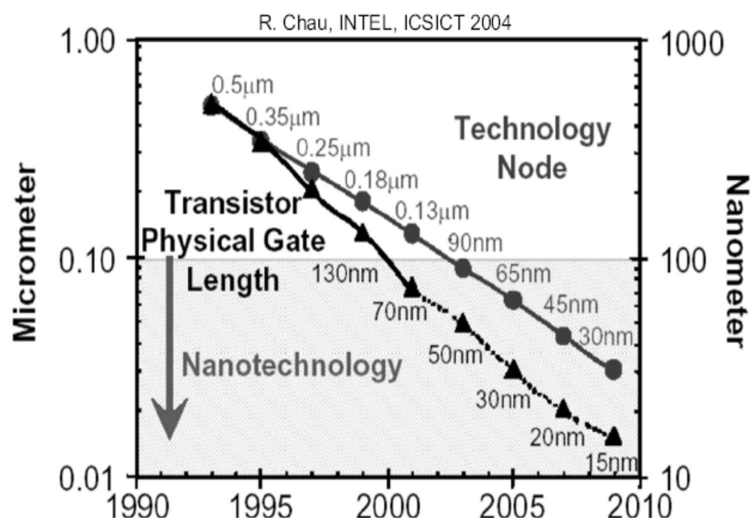

Fig. 1: Transistor physical gate length and technology node as a function of year of introduction (From R. Chau, INTEL, ICSICT 2004).

Experimental

We apply Atomic Layer Deposition (ALD) or Metal-Organic Chemical Vapor Deposition (MOCVD) to grow ultra-thin films of oxides such as Al_2O_3, ZrO_2, La_2O_3, HfO_2, and ternary oxides or oxide stacks of these. In some cases, the fabricated dielectric stacks are subjected to a post deposition anneal (PDA) in nitrogen- or argon-atmosphere. Metal electrodes, such as Aluminum (Al) or platinum (Pt) are deposited by ALD or sputter deposition, and patterned by optical lithography including lift-off technique or by wet-chemical etching. Some devices are then subjected to a post metallization anneal (PMA) in forming gas atmosphere. The finalized stacks or devices are characterized by physico-chemical or electrical measurement techniques. More details on the experimental and on the measurement procedures, as well as on the results that are exemplary given beneath can be found in [3] – [6].

Results

Silicon Substrates

In Fig. 2 measured leakage current density values at –1 V (accumulation regime) of MOS capacitors incorporating Al-gates and various oxide/semiconductor stack types are compared. All samples have been subjected to a PDA at various temperatures ranging from 400 °C to 800 °C, and a PMA at 425 °C. Regarding the single ternary oxides $La_xAl_yO_z$ and $La_xZr_yO_z$ (not shown), $La_xAl_yO_z$ exhibits clearly superior insulation properties compared to $La_xZr_yO_z$. If we introduce a thin layer of Al_2O_3 either at the bottom or the top, leakage currents are clearly reduced. The best leakage currents are achieved if the ternary oxide is sandwiched in between to thin layers of Al_2O_3. Additionally, from Fig. 4 we can learn that the following measures have a positive impact on the leakage current: (i) increasing the PDA-temperature, (ii) reducing the amount of La_2O_3 in the ternary oxides, and (iii) increasing the thickness of the single films. Point (i) is most likely due to an increased and more SiO_2-containing interfacial layer at the oxide/ Si-substrate interface. Point (ii) indicates that the La_2O_3 ALD-process seems to be problematic, and point (iii) is due to reduced conductance mechanisms like tunnel- or Frenkel-Poole emission.

Germanium Substrates

The I-V measurements, shown in Fig. 3, indicate that lowering of the ALD deposition temperature from 300 °C to 150 °C yields lower gate leakage currents of about one order of magnitude. There are two possible explanations for this behavior: first, (i) much longer purge times during the ALD growth at lower deposition temperatures (see also Table 1) strongly increase the process time, and therefore enlarge possible diffusion times for oxygen, which may lead to a stronger GeO_x regrowth at the germanium/ oxide interface. Second, despite of the thinness of the films an increased polycrystalline amount in the ZrO_2 layer at higher deposition temperatures may exist, and therefore generate a larger quantity of leakage paths across the oxide. All dielectric stacks exhibit a breakdown in the range of 3 V to 4 V gate bias with corresponding leakage current of >1 A/cm^2, except of the samples with HBr pre-treatment, whereat the breakdown occurs not until bias voltage has been driven to about 6 V. We believe that this remarkable result is correlated to the entire removal of the sub-oxide. For silicon, it has been reported that a thin interfacial SiO_2 layer is the origin of breakdown of high-k dielectric stacks. Assigned to our results, a thin interfacial GeO_x layer yields to a breakdown of the dielectric stacks at lower gate bias voltage compared to stacks deposited on a GeO_x-free germanium substrate.

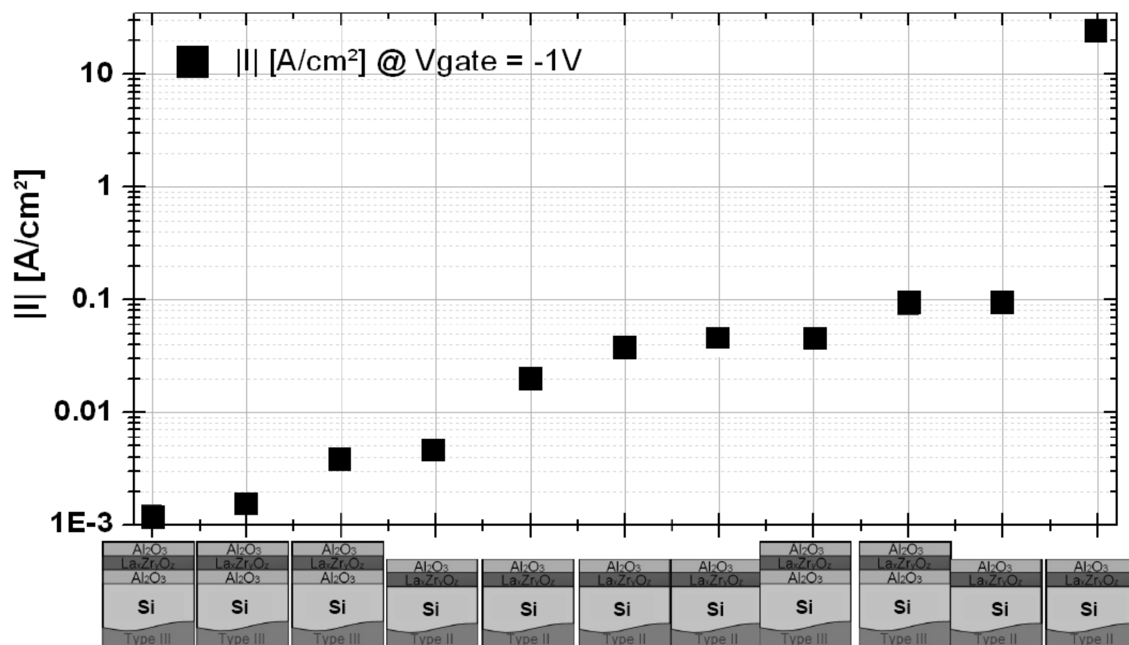

Fig. 2: Gate leakage current density values at –1V (accumulation regime) gate bias of MOS capacitors incorporating Al gate electrodes, p-Si substrates and various gate dielectrics. Every value corresponds to one gate stack type that is schematically shown at the bottom.

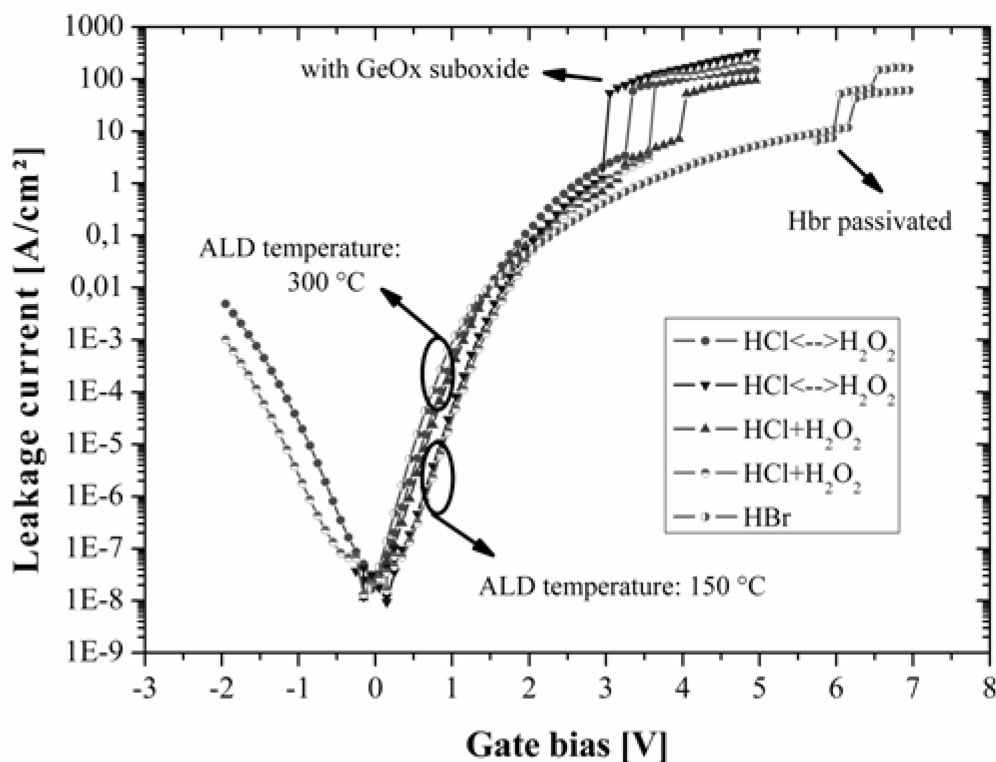

Fig. 3: FTIR spectra of the sample in Fig. 2 in the frequency range of the carbon-related local vibration modes. With increasing annealing time more and more carbon moves from substitutional into SiC sites.

Top-Down Vertical Nanowire Transistor with High-*k*/Metal Gate

Figure 4 summarizes a new device concept based on a top-down etching approach of Si nanowires. The Ni-dots serve as a hard mask to etch the wires out of the Si wafer as well as the top contact. The etched wires are capped by ALD deposited Al_2O_3 and Pt forming the gate stack. The advantage of this method is that well structured patterns of a distinct number of devices can be fabricated, which determine the obtained current of one pattern as shown in the upper left image of Fig. 4.

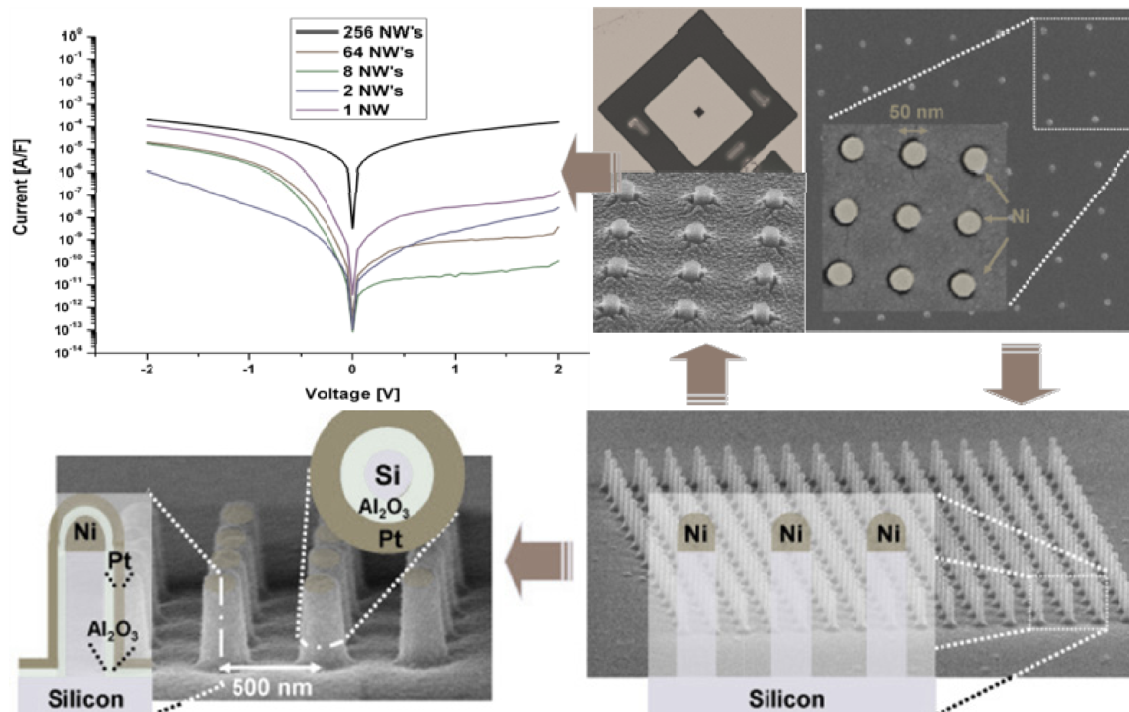

Fig. 4: Top-down vertical nanowire transistor device concept with high-k/metal gate technology deposited by ALD.

Conclusion

An overview of materials and devices, including high-*k*/metal gate technology on high-mobility substrates such as Ge or strained Si, as well as new device geometry concepts has been given.

References

[1] International Technology Roadmap for Semiconductors, http://www.itrs.net/

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