Atomic Layer Deposition of High-*k* Gate Dielectrics on Germanium and Silicon Substrates

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$Al_2O_3/ZrO_2/Al_2O_3$ high-k dielectric stacks are grown on Germanium and Silicon substrates by Atomic Layer Deposition at temperatures of 110 °C, 150 °C, 200 °C and 300 °C from trimethylaluminum (TMA) and tetrakis-(dimethylamino)zirconium (Zr(NEt2)4) precursors with water. The stacks are investigated and compared in terms of deposition temperature and Ge-substrate preparation. As a result, we show that in general the deposition of the stacks at lower temperatures (150 °C) leads to lower leakage currents in the range of several orders of magnitude. The deposition on GeOx-free Ge-substrates, obtained by HBr-etching, yields much higher breakdown voltage of the high-k oxide.

Introduction

Aside from silicon, germanium is an attractive material in downscaled Complementary-Metal-Oxide-Semiconductor (CMOS) devices due to its high electron mobility and its low dopant activation temperatures. The fact that Ge does not offer a stable natural oxide is no more a disadvantage over Si. For the extrinsic ultra thin dielectric layers envisaged for future CMOS-devices, Atomic Layer Deposition (ALD) is the favored deposition process for high-k dielectric materials like hafnium dioxide (HfO_2) or zirconium dioxide (ZrO_2). For the deposition process, alternative semiconductors as well as novel device architectures issues a lowering of the deposition temperature well below 300 °C.

Electrical and structural characterization of ALD triple stacks of $Al_2O_3/ZrO_2/Al_2O_3$ (AZA) on Si grown by a chlorine-based ($ZrCl_4$) chemistry for ZrO_2 deposition at temperatures of 300 °C have already been performed [1]. However, residual chlorine content in the ALD films leads to increased oxide charge concentrations and interface states, if deposited at lower temperatures [2]. Only a chlorine-free metal amide precursor seems to be favorable for a low temperature deposition with satisfactory electrical characteristics.

In this work AZA triple layers grown by ALD on Si and Ge from a chlorine-free precursor system at deposition temperatures ranging from 110 °C to 150 °C are compared with dielectrics deposited at the usual higher temperatures ranging from 200 °C to 300 °C in terms of their applicability in nanoscaled MOS devices. In order to explore the thermodynamical stability of the as-grown oxides, different Ge surface pretreatments and post deposition annealing steps are applied. The morphology is verified by High-Resolution Transmission Electron Microscopy (HR-TEM) analysis. MOS capacitors are used to characterize the electrical performance referred with film stack structure and morphology.

Experimental

Sample Preparation

Silicon

As substrates, boron (p)-doped, (100)-oriented Si wafers with 1 – 5 Ohm·cm sheet resistance have been used. After ultrasonically enhanced Piranha- and RCA-type cleaning, all substrates were exposed for 10 min to a 2% HF solution to remove the native SiO_2 layer from the substrates. Immediately prior to deposition, a short H_2O-rinse or a variable exposure of 10 min has been applied.

Germanium

Here, antimony-doped (100)-oriented n-Ge wafers with 6 – 10 Ω·cm sheet resistance have been used. All substrates were exposed for 3 min to one of the following wet chemical treatments to remove the instable native GeO_x:(i) 20-% HCl-solution with cyclic 35%-H_2O_2-rinse (HCl <—> H_2O_2), (ii) 20-% HCl solution with incorporated 1% H_2O_2 solution (HCl+H_2O_2) and (iii) 48-% HBr solution (HBr). A short H_2O rinse and a subsequent N_2 blow has been applied to remove chemical residuals.

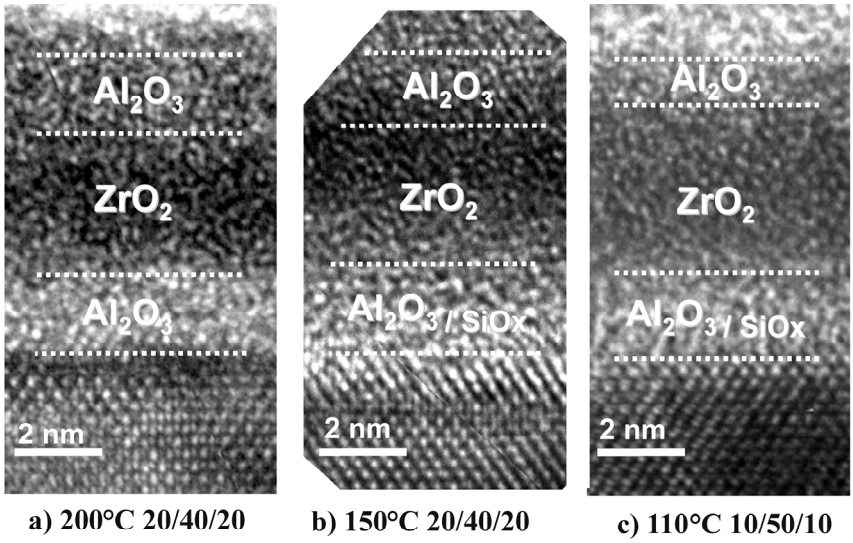

Fig. 1: HR-TEM of $Al_2O_3/ZrO_2/Al_2O_3$ stacks deposited at (a) 200 °C, (b) 150 °C and (c) 110 °C on Si substrates.

The high-*k* oxide stacks have been grown in a Savannah 100 ALD reactor from Cambridge NanoTech Inc. The substrate temperatures during ALD growth have been set to 110 °C, 150 °C, 200 °C, and 300 °C, respectively. In order to achieve a reliable layer by layer growth, we applied purging times from 3 seconds to 90 seconds. Three different dielectric stacks have been deposited: (i) 70 ALD-growth-cycles of pure ZrO_2 (0/70/0), (ii) stacks composed of a 10 ALD-growth-cycles Al_2O_3 at the bottom and at the top of a 50 ALD-growth-cycles ZrO_2, respectively (10/50/10), and (iii) stacks corresponding to 20 ALD-growth-cycles Al_2O_3 at the bottom and at the top of 40 ALD-growth-cycles ZrO_2, respectively (20/40/20). After oxide deposition, a Post Deposition Annealing (PDA) in inert, reductive, and oxidative atmospheres, respectively, has been applied for a duration of 5 min at 400 °C. In order to complete the MOS capacitors, circular aluminum (Al) electrodes with diameters of 100 µm have been fabricated by sputter deposition and patterned by photolithography involving a lift-off technique.

Measurements

Morphology

In Fig. 1 a morphological analysis from HR-TEM of 10/50/10 stacks deposited on Si at 110 °C and 20/40/20 stacks deposited at 150 °C and 200 °C with similar total thickness of about 6.9 nm to 7.0 nm is shown. The images indicate contiguous amorphous ZrO_2 and Al_2O_3 films even at deposition temperature of 200°C. Samples deposited at 200 °C exhibit no interfacial SiO_2 whereas samples deposited at 150 °C and at 110 °C most likely exhibit SiO_2 or mixtures of Al_2O_3 and SiO_2 at the oxide/semiconductor interface. These oxides may have two origins, (i) a partly fragmentary, not fully contiguous Al_2O_3 bottom layer, and/or (ii) much longer purge times during the ALD growth at lower deposition temperatures strongly increase the process time, and therefore enlarge possible diffusion times for oxygen, which may lead to a stronger SiO_2 growth at the Si/oxide interface. In both cases, oxygen may be able to diffuse through the ZrO_2 matrix during the oxide growth process and to oxidize the Si surface. In the case of the 10 ALD-growth-cycle process, the Al_2O_3 layer is most likely not contiguous due to the previously mentioned inhibited growth, and therefore the oxygen is able to diffuse easier to the dielectric/ Si interface to form an interfacial SiO_2 layer.

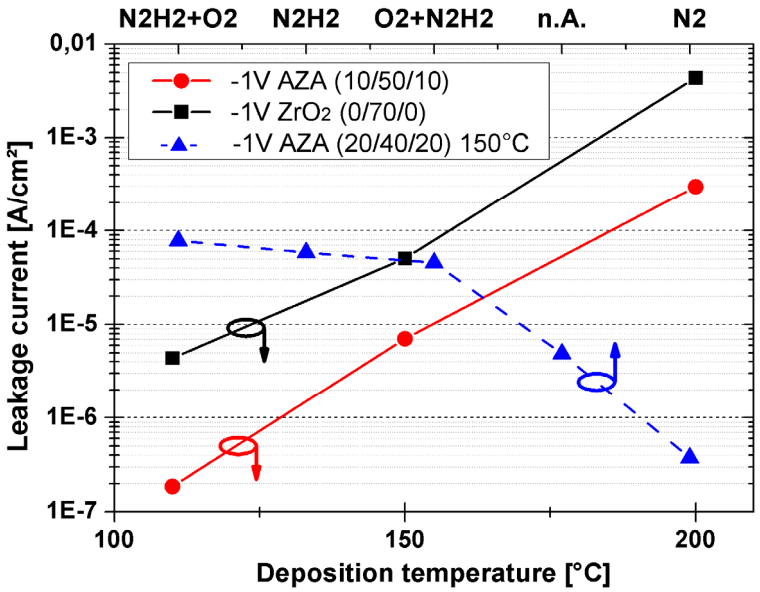

Fig. 2: Impact of the deposition temperature and PDA on the leakage current of the various high-*k* MOS-capacitors at -1 V gate bias.

Electrical characterization

As an important result on Si substrates, it can be seen that lowering of the deposition temperature from 200 °C to 110 °C yields lower gate leakage currents of about 3 orders of magnitude, as shown in Fig. 2. As mentioned above, this is most likely to longer purge times at lower deposition temperatures, which may lead to a stronger SiO_2 growth at the Si/oxide interface.

The *I-V* measurements of AZA stacks on Ge substrates, shown in Fig. 3, indicate that lowering of the deposition temperature from 300 °C to 150 °C yields lower gate leakage currents of about one order of magnitude. Here, similar explanations are presumably: Much longer purge times during the ALD growth at lower deposition temperatures enlarge possible diffusion times for oxygen, which may lead to a stronger GeO_x regrowth at the Ge interface. All dielectric stacks exhibit a breakdown in the range of 3 to

4 gate bias, except of the samples with HBr pre-treatment, where the breakdown occurs not until bias has been driven to ~6 V. We believe that this remarkable result is correlated with a complete removal of the sub-oxide through HBr, as reported. In the same way, it has been reported for Si that a thin interfacial SiO_2 layer is the origin of breakdown of high-k dielectric stacks [3].

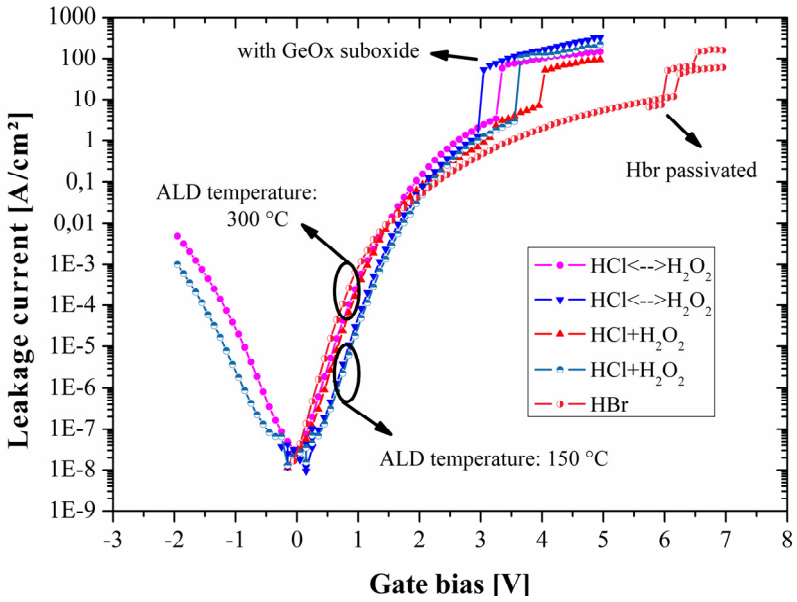

Fig. 3: Leakage current measurements of the Al/oxide/n-Ge MOS capacitors with AZA 20/40/20 dielectric stack as oxide, deposited at 150 °C and 300 °C.

Conclusion

In conclusion, dielectric stacks grown at low temperatures are suitable to design high performance MOS devices, exhibiting well-behaved electrical characteristics and low gate leakage currents. Therefore, the “low temperature” process appears applicable for lift-off processes involving resist polymers, or for the deposition on alloy heterostructures, making it potentially attractive for scaled CMOS device applications.

Acknowledgements

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