

Engineering of Dielectric Materials for Silicon Technology

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Scaling of electronic devices, especially of CMOS devices, follows Moore's law for more than two decades. But today, severe difficulties related to fundamental physical effects in ultra thin layers and small lateral structures have emerged. Among them are increased leakage currents and fast degradation of device parameters. One approach to overcome these problems is the introduction of new materials with specific tailored properties. Therefore, silicon technology, which was built on a rather restricted set of materials, has opened itself to a variety of new materials.

The most prominent case is probably the replacement of the gate dielectrics, silicon dioxide, by so called high k materials. In this talk, the problems related to the introduction of these new high-k materials will be discussed. The permittivity of high-k layers like Hf, Zr, or Ti based oxides is the driving force to use them in CMOS transistors to increase device performance like current drive. But in order to utilize those layers, many other problems occur and have to be solved. Examples are threshold voltage shift, mobility degradation, or parameter instability. Also new process steps like Atomic Layer Deposition had to be introduced and developed, mainly to control interfaces on sub-monolayer scale. Today, new high-k dielectrics are engineered materials with tailored properties for specific applications. High-k based gate stacks require well controlled interface and layer formation to ensure high carrier mobility, low and symmetrical threshold voltages, and tolerable degradation. After discussing this approach for MOS transistors, the application of tailored high-k dielectrics in DRAM capacitors and Flash memory cells will be shown. In DRAM capacitors, leakage current and dielectric integrity are the main issues to be engineered. On the other side, floating gate flash memory cells require controlled band alignment and low parasitic trapping in order to improve device performance.

Finally, a short outlook will show that new materials, engineered for specific electronic parameters, will open a variety of new option for scaling of classical devices as well as for heterogeneous integration of electronic components.