Process Integration of Pt-Metal-Gate High-k ALD Dielectrics on sSOI

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In this presentation we focus on the electrical properties of high-k-dielectric gate stacks, namely aluminum-oxide (Al_2O_3) on strained silicon-on-insulator (sSOI). In order to get both, stoichiometry as well as atomic scale smoothness, these oxides are deposited by Atomic Layer Deposition. These properties are compared to those obtained for MOSFET devices on bulk silicon.

Introduction

The superior properties of the silicon-silicon dioxide combination are the key to the success and the opportunity to continuously shrink the device geometry of modern transistors. However, to keep the inversion channel in a quasi-2-dimensional arrangement, the silicon dioxide has to be shrunk accordingly to the lateral dimensions, thus modern devices approach the tunnel limit for the gate dielectric, giving rise to the onset of high gate leakage currents. Silicon dioxide has therefore to be replaced by proper high-κ-dielectrics, enabling larger tunnel barriers at approximately the same drive current. In industrial CMOS, such high-κ-dielectrics were introduced at and beyond the 45 nm technology node, often in combination with metal gates.

Further improvement of the device performance is addressed by the replacement of bulk silicon as substrate material. By this step, mobility constrains of the bulk silicon substrates should be overcome. Promising candidates for this purpose are high-carrier-mobility substrates like SiGe or Ge. Another approach is the use of engineered substrates like strained silicon, offering the opportunity of an enhancement of both, the electron and the hole mobility [1].

In this presentation we focus on the electrical properties of high-κ-dielectric gate stacks, namely aluminum-oxide (Al_2O_3) on strained silicon-on-insulator (sSOI). In order to get both, stoichiometry as well as atomic scale smoothness, this oxide is deposited by Atomic Layer Deposition (ALD) [2]. The electrical properties are compared to those obtained for MOSFET devices on bulk silicon. Suitable process temperature ranges for annealing post-treatments are determined.

Experimental

Process Flow and Sample Preparation

The process flow is schematically depicted in Fig. 1 (left). The high-κ dielectric Al_2O_3 is deposited at temperatures of 200 °C to sSOI substrates. A scheme of the final device is shown in Fig. 1 (right). The influence of different process parameters to the properties

of Bulk-Si MOSFETs is investigated. Different Post-Deposition and Post Metallization Annealing Treatments are applied.

In a final step the optimized process flow is applied to strained Silicon-on-Insulator substrates. Schottky-Barrier-MOSFET devices with PtSi source/drain regions were processed with the same deposition and pretreatment parameters (Fig. 4).

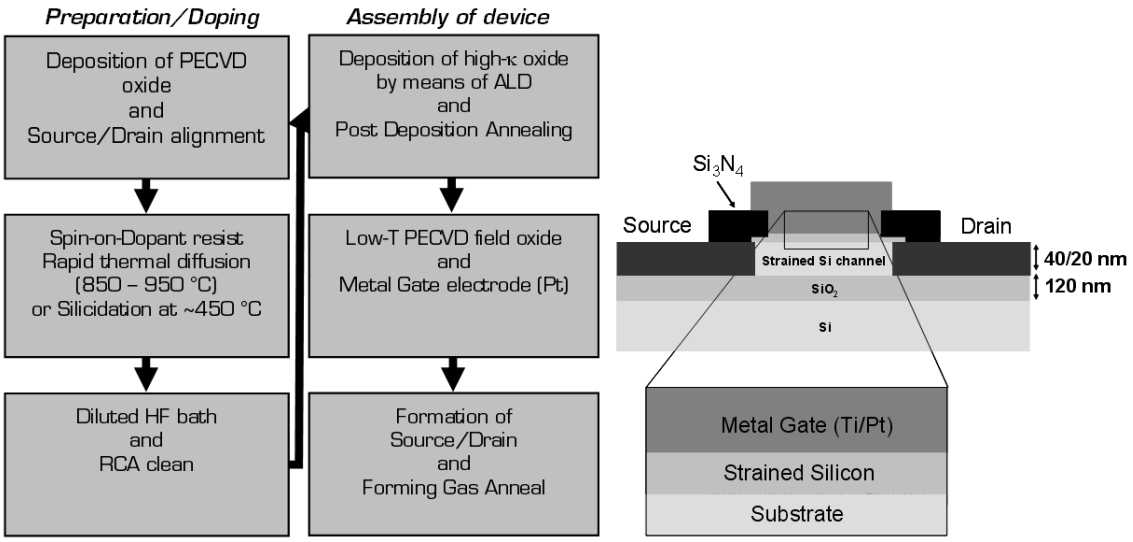

Fig. 1: Process Flow for MOSFET devices (left) and a schematic of the final MOSFET (right).

Results

Current-Voltage Characteristics

Optimized process conditions were found for the deposition of Al_2O_3. A Post Metallization Anneal was applied in Forming Gas atmosphere at 500 °C for 30 minutes. Figure 2 shows the resulting Transfer and Output characteristics of the Bulk-Si MOSFET.

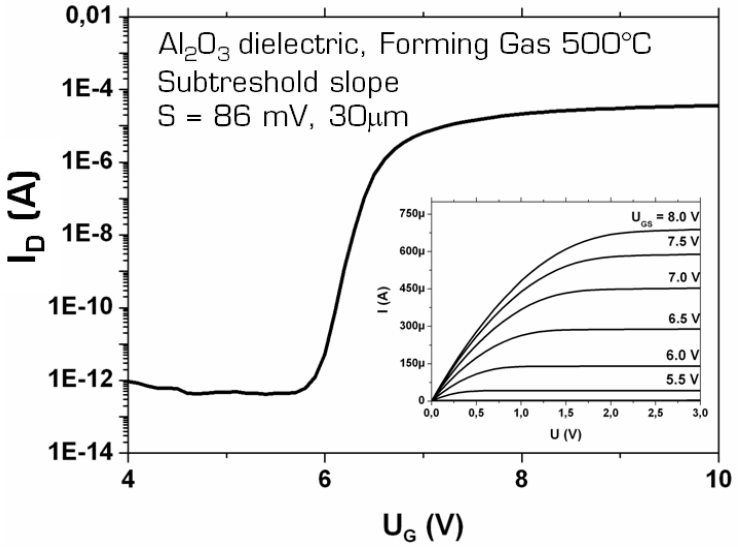

Fig. 2: Transfer-/Output characteristic for bulk-Si.

Applying the same process parameters to SB-MOSFETs on sSOI results in well behaved current characteristics. These can be seen in Fig. 3.

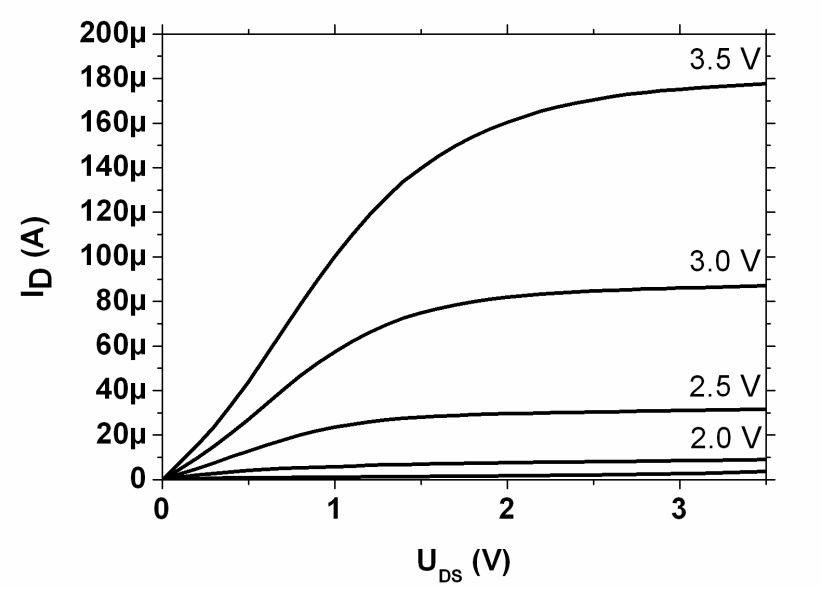

Fig. 3: Output characteristic for sSOI substrates. The strained silicon film thickness is 40 nm.

Split-CV Measurements for Mobility Determination

By means of split-capacitance-voltage measurements [3] the mobility of processed devices can be investigated. Thus, interface quality of the Si-channel to gate oxide is determined. An optimized deposition process was studied for bulk-Si and Al_2O_3 with the optimized process conditions. Here peak mobilities of 175 cm^2/Vs can be obtained (Fig. 4). These results can be compared to the results obtained for sSOI substrates with mobilities of 53 cm^2/Vs.

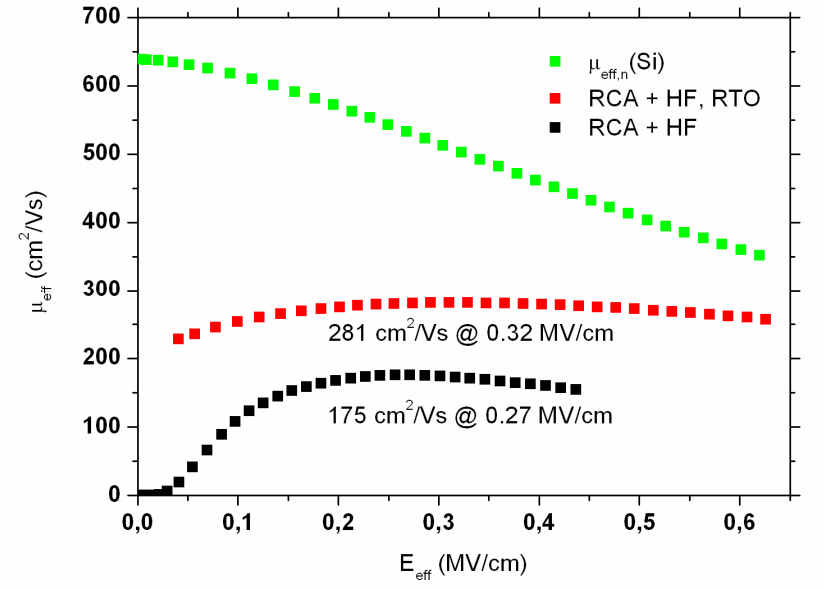

Fig. 4: Effective mobilities of n-MOSFET and the universal field mobility for n-Si/SiO_2.

Conclusion

Properties of metal gate high-κ dielectrics on strained Silicon-on-Insulator substrates (sSOI) have been investigated. A successful integration scheme of high-κ dielectrics on sSOI substrate is presented using metallic source-drain contacts processed by silicidation. The results are compared to those of bulk silicon substrates where MOSFET characteristics have been evaluated. Further studies will address the optimization of the deposition process in combination with the formation of the source/drain contacts on sSOI substrates.

Acknowledgements

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