# Recent Improvements on InAlN/GaN MOS-HEMTs

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We present the technology and the performance of InAlN/GaN MOS-HEMTs with gate insulation and surface passivation by using $ZrO_2$ and $HfO_2$. 10-nm thick high-k dielectrics were deposited by MOCVD and by ALD before the ohmic contacts which were annealed at only 600 ºC. The passivation and the insulation of 2 µm gate-length MOS-HEMTs led to a gate leakage current reduction by four orders of magnitude and a 2,5x increase of the pulsed source drain current if compared to Schottky barrier (SB)-HEMTs when the high-k is deposited by MOCVD. Moreover, clear current collapse suppression is observed also when the $ZrO_2$ is deposited by ALD.

## Introduction

Gallium Nitride (GaN) has become the superior material for high power devices in microwave applications due to its large bandgap, the high saturation velocity, the high thermal conductivity, and its high mobility in 2-dimensional electron gas (2DEG). This 2DEG is based on the strong ionic bonding of the GaN crystal structure causing large spontaneous and piezoelectric polarization fields at interfaces [1] as used in conventional AlGaN/GaN high mobility electron transistors (HEMTs). However, the stress at the interfaces limits the device performance. Heterostructure devices based on InAlN/GaN [2] have already shown superior results [3], [4] in comparison to conventional AlGaN/GaN HEMTs, due to their higher spontaneous polarization and the possibility of lattice-matched growth of InAlN on GaN at an indium composition of around 18%. Therefore, higher power operation and thermal stability are expected from such devices. However, RF dispersion defined as decreasing output power at large signal gate modulation is still an important issue to be solved. Preview results on AlGaN/GaN devices have shown that surface-related traps are causing transients that prevent the gate from opening after channel depletion [5], [6].

In this report we present our current improvements on InAlN/AlN/GaN MOS-HEMT devices with $ZrO_2$ or $HfO_2$ for gate insulation and surface passivation. Metal-Organic Vapor Deposition (MOCVD) and Atomic Layer Deposition (ALD) techniques have been used for the $ZrO_2$ deposition.

## Experimental

The lattice-matched heterostructure was grown by MOCVD on a sapphire substrate. The 1.1 nm thick AlN interlayer was inserted in the conventional structure to increase the mobility in the 2DEG. The dielectric deposition was directly done after Ar-based mesa isolation, requiring that post processed steps are done at lower temperatures without dielectric degradation.

It was found that plasma pre-treatment with $SiCl_4$ before metal evaporation could decrease the ohmic resistance to 0.7 Ω/mm after annealing at only 600 °C. Investigating the surface by Auger Electron Spectroscopy (AES) showed that the total concentration of carbon impurities was reduced only after pre-treatment and for lower temperatures. For the rapid thermal annealing RTA at 600 °C without the RIE pretreatment the ohmic contact resistance $R_C$ was shown to have an unacceptable value of 12 Ωmm. On the other hand $SiCl_4$-based plasma pretreatment led to a contact resistance $R_C$ value as low as 1 Ωmm.

Consequently plasma pretreatment and RTA at 600 °C for 2 minutes was used for the MOS HEMT processing. The final gate processing was done by 2 μm wide Ni/Au contacts (Fig. 1).

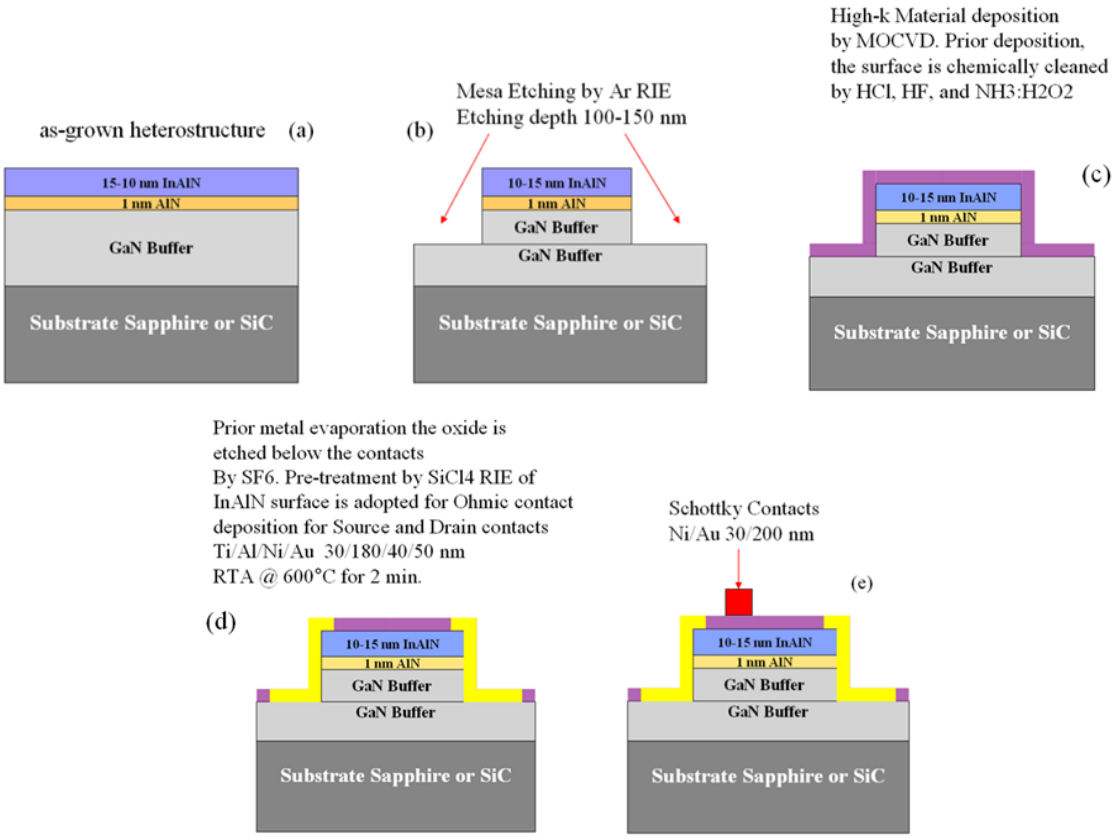


Fig. 1: Schematic illustration: technological steps for the fabrication of the MOS-HEMT structure. The oxide is deposited after the mesa fabrication and before the ohmic contacts metallization.

Figure 2 shows the gate *I–V* characteristics in the reverse and forward direction of InAlN/GaN HEMTs, and MOS-HEMTs. A strong reduction of about four orders of magnitude of the leakage current in MOS-HEMTs is observed in comparison to the HEMTs, whereas the $ZrO_2$-based HEMTs exhibit the same reduction of the leakage current as the $HfO_2$-based HEMTs. From the MOS *I–V* breakdown at about 4 V forward bias in the case of $HfO_2$ and $ZrO_2$ (current density $J = 5\times10^3$ mA cm$^{-2}$) we roughly estimate the oxide field strength to be about 4 MV cm$^{-1}$.

The output characteristic of the MOS-HEMT was not only improved by higher drain current at increased forward bias, possibly due to the gate insulation, but also showed slightly higher transconductance than the compared SB HEMT. This behavior was ex-

plained by improvement of the intrinsic mobility below the gate, which is more effective in long channel devices [7].

For the current collapse investigation we pulse the HEMT gate contact from the "off-state" level of –10 V to a chosen gate-source voltage $V_{GS}$ value while the constant drain-source voltage $V_{DS}$ is applied on the drain.

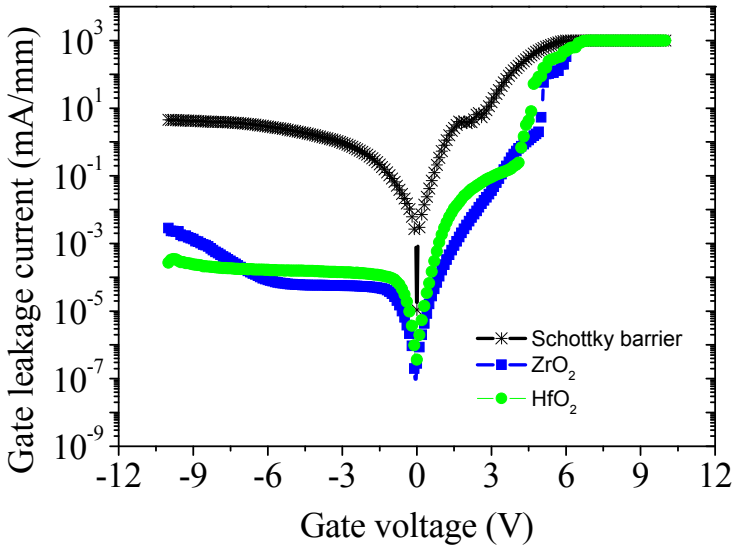


Fig. 2: *I-V* characteristics of the gate leakage current as function of the gate voltage of $HfO_2$ ($ZrO_2$)-based MOS-HEMTs (green and blue, respectively) and of a Schottky barrier HEMT (black curve).

Figure 3 (a) (SB-HEMT) confirms a clear lag of the drain transient current $I_{DS}$ behind the *dc* values (for $V_{GS}$ = 0 V) in the linear part of the characteristics.

For $V_{GS}$ = 0 V the transients are shown at two different pulse durations (100 and 200 ns). Higher values obtained for 200 ns indicate gradual surface de-trapping in the SB-HEMTs.

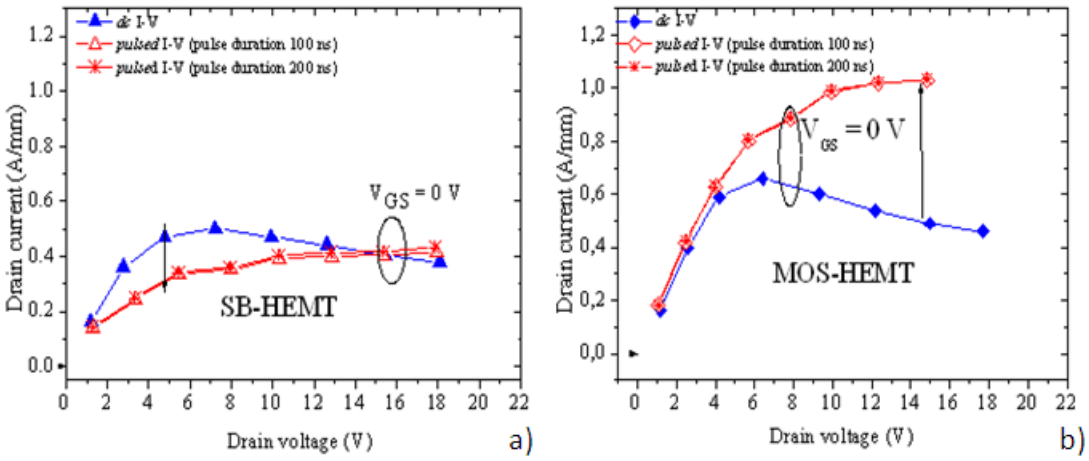


Fig. 3: *dc* and *pulsed* output characteristics of InAlN/GaN SB-HEMTs (a) and of $ZrO_2$-InAlN/GaN MOS-HEMTs (b). Gate contact is pulsed from –10 V to the set $V_{GS}$, $V_{DS}$ is sequentially increased, the duration of the pulse is 100 ns and 200 ns

On the other hand, the linear part of the output characteristics of InAlN/GaN MOS HEMTs (see Fig. 3 (b)) show coincidence of the pulsed and the *dc* current characteristics suggesting a stable InAlN surface potential.

For low value of the drain-source voltage $V_{DS}$ in the linear part of the output characteristics we can assume a minimal self-heating effect even in the *dc* mode of operation and thus the coincidence with the pulsed characteristics suggests an effective surface passivation.

In the *dc* mode of operation we observe a drain current enhancement only by about 20% in MOS-HEMTs if compared to SB-HEMTs (Fig. 3 (a) and (b)).

However the pulsed drain current $I_{DS}$ at gate-source voltage $V_{GS}$ = 0 V is up-to 2.5 times higher for MOS HEMTs if compared to SB HEMTs and that clearly demonstrates the superiority of the MOS-HEMT with the surface passivation by dielectrics. We note that the almost similar performance enhancement was observed for both $ZrO_2$- and $HfO_2$-based MOS HEMTs.

The low density of trapped electrons and low surface potential at the InAlN/dielectric interface was further validated by measuring the sheet resistance $R_{ht}$ of the SB-HEMTs and MOS HEMTs (in the steady state). For the SB-HEMT we observed an increased value of $R_{sh} \sim 500$ Ω/square (compared with 237 Ω/square measured by Hall method just after the InAlN/GaN growth) probably because of a gradual oxidation and/or contamination of InAlN surface before and during the HEMT processing.

On the other hand an extremely low $R_{sh} \sim 110$ (135) Ω/square has been observed when the InAlN surface is thoroughly etched and subsequently passivated by $ZrO_2$ ($HfO_2$), indicating a low surface potential and/or high carrier mobility in the channel.

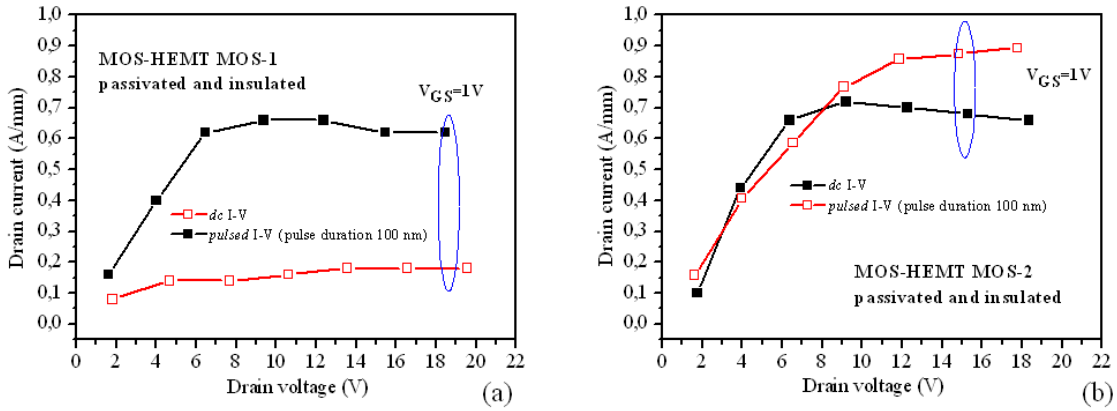


Fig. 4: *dc* and *pulsed* output characteristics of InAlN/GaN MOS-HEMTs. In MOS-1 the $ZrO_2$ is prepared starting with a single water pulse is passivated while in MOS-2 the $ZrO_2$ is prepared starting with 10 water pulses prior to the actual ALD process. Gate contact is pulsed from –10 V to the set $V_{GS}$, $V_{DS}$ is sequentially increased, the duration of the pulse is 100 ns

By using ALD for the $ZrO_2$ deposition, an aggressive ex-situ chemical surface cleaning in combination with an increased hydroxylation of the InAlN surface by repetitive in-situ $H_2O$ treatment is needful in order to guarantee a good and a stable oxide/semiconductor interface. Since we may believe that the InAlN-surface is not perfectly hydroxide-terminated after the initial chemical ex-situ cleaning procedure we vary the initial phase of the ALD process. By this method we try to improve the hydroxide-termination of the InAlN surface. This may in turn support the initial growth behavior of the ALD process

and improve the oxide/semiconductor interface. The actual ALD process consists of 150 cycles, which results in 10.5 – 11.0 nm thick $ZrO_2$. Figure 4 (b) shows a clear reduction of the current collapse thanks to an aggressive ex-situ chemical surface cleaning in combination with an increased hydroxylation of the InAlN surface by repetitive in-situ $H_2O$ treatment.

## Conclusion

We have shown that the optimized InAlN/GaN MOS-HEMTs exhibit reduced gate leakage currents of about 4 orders of magnitude as compared to SB-HEMTs and a significantly reduced current collapse effect by using high-k dielectrics deposited both by MOCVD and ALD. Moreover an aggressive ex-situ chemical surface cleaning in combination with an increased hydroxylation of the InAlN surface by repetitive in-situ $H_2O$ treatment has to precede gate insulation and surface passivation. This in turn enhances the ALD growth of the $ZrO_2$ during the first ALD cycles leading to an improved $ZrO_2$/InAlN interface.

## Acknowledgements

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