ALD Based La_2O_3 Ge Interface Passivation for High Performance MOS-Device Applications

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Ge is the most attractive channel material for next generation p-channel metal-oxide semiconductor (pMOS) devices due to its highest hole mobility and its low dopant activation temperatures. The disadvantage of Ge not to offer a stable, natural homogenous oxide requires the application of an “extrinsic” heterogeneous oxide in terms of electrical and chemical compatibility. For ultrathin dielectric layers envisaged for future CMOS-devices, Atomic Layer Deposition (ALD) is one of the favored deposition processes for high-*k* dielectric materials due to its high uniformity, high conformity, and excellent thickness controllability of the layers. Several very capable approaches for Ge surface passivation techniques have been reported, and superior electrical behavior of the dielectrics by using Atomic Layer Deposition (ALD) mainly on interfacial GeO_2 has been observed. The rare earth oxide La_2O_3 is one of the most promising high-k dielectrics in order to passivate the hardly controllable Ge interface. It seems that La_2O_3 passivations can uniquely meet required scaling abilities and low interface trap densities. In this discussion, both aspects will be addressed: On the one hand, it will be shown that ALD grown La_2O_3 is capable to reach 0.5 nm equivalent oxide thickness (EOT) and on the other hand, a strong reduction of interface trap densities down to mid-10^{11} $eV^{-1}cm^{-2}$ will be presented by a Pt-assisted annealing approach of La_2O_3/ZrO_2 oxide stacks. Conductance measurements also indicate the absence of compromising mid-gap traps by using La_2O_3 passivation layers.

This work is funded by the Austrian Science Fund (FWF), project No. P19787-N14. The Gesellschaft für Mikro- und Nanoelektronik (GMe), as well as the ZMNS, are gratefully acknowledged.

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