GaAs-MMIC Design Aspects for High Volume Production

Hartmut Kapusta

GaAs MMIC CAD and Foundry
Balanstr.73, D-81541 München

1. Introduction

1.1 History – Volume Production-Processes

Starting 1980 with GaAs-MESFETS and 1982 with the world's first GaAs-MMIC, production of GaAs devices at Siemens HL ramped up to more than 80 million pieces in 1998.

Three kinds of active device families are in production today, a MESFET, a HEMT and a HBT process. They all are produced in one single GaAs fab using the same equipment. Unified passive components make the MMICs complete.

Also the backend activities (thinning, via etching, sawing and packaging) are common for the three families.

For the MESFET family a patented self-aligned ion implantation process DIOM (**D**ouble **I**mplantation **O**ne **M**etalization) is used, which results in robust, reliable, and uniform devices compared to conventional recessed gate processes.

The process parameters are optimized to the application requirements:

Gate lengths of 0.8 and 0.5 µm are used depending on the frequency of operation. The active channel is optimized to either low noise or high power applications, and especially for mobile communication high power devices with low supply voltage allow to reduce the number of battery cells and therefore the weight and size of handheld mobile phones.

HEMT processes are based on epitaxial grown materials. For frequencies up to ~40 GHz a gate length of 0.18 µm is used (f_t > 60 GHz), and process parameters are optimized for either low noise or high power applications. For even higher frequencies 0.13 µm gates are used which results in f_t of 110 GHz.

The most advanced process uses **h**etero **b**ipolar **t**ransistors (HBT). Several MMIC designs are in the evaluation phase with very promising results regarding output power and efficiency at minimized chip area.

The passive components for all of the processes above follow unified design rules and are processed using the same standards and equipment. They cover lumped elements like resistors, inductors, and capacitors as well as distributed elements like microstrip and coplanar lines and their discontinuities. Interconnections between different compo-

nents are preferably realized by air bridges of plated Au which offer low parasitic capacitance and avoid edge problems due to non-planar surface.

Low inductive substrate via holes are essential for the behavior of microstrip based unbalanced circuits.

2. Essentials for Volume Production

2.1 Competitive Products in Cost and Performance, Customer Acceptance

Most impulses for volume production in the last few years have been due to the boom in the mobile communication market. Two contrary GaAs MMIC trends can be observed for the RF power stage in mobile stations:

- Devices as cheap and small as possible; DC circuits and matching on chip waste expensive chip area and should be added externally.
  Microwave skill by the mobile phone designer is essential.
- PA should be a black box, in- and output internally matched, bias circuit on chip. The customer doesn't want to care about microwave behavior.

As a manufacturer who provides components for all the different mobile communication systems all over the world Siemens offers both types to its customers. Figure 1 shows in identical scale MMIC examples for the minimized and the "all functions included" type.

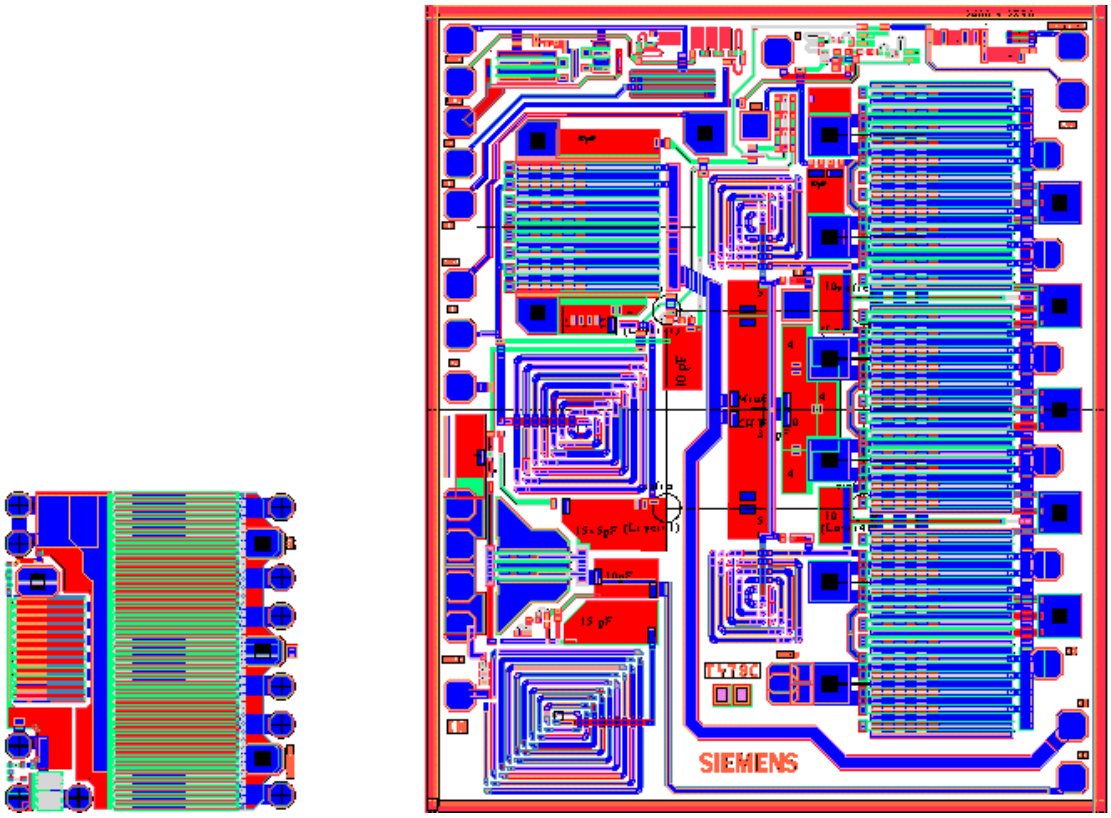

Fig. 1: 3 stage GSM PA MMIC minimized and "all included" type (identical scale)

2.2 Avoid Production Bottlenecks

Sometimes it is important to find workarounds for possible bottlenecks in production.

One example is the substrate via etching process. A wet etching process takes a few minutes per wafer while a dry etching process takes roughly ten times longer. Despite some advantages of the dry etching process (smaller structures and distances possible) the wet etching process is preferred because of its higher throughput.

A further example is the sub-0.3 µm gate process for HEMTs. It is not possible to realize these gate lengths with conventional lithography on an I-line stepper (365 nm). Alternatively, E-beam, deep UV, or X-ray lithography could be used, but they do not fulfil our requirements for throughput and/or cost reduction.

We use chromeless phaseshift masks on I-line steppers to define a well controlled homogeneous photoresist structure well below 0.5 µm, but for physical reasons still larger than the target gate length. Two or more subsequent spacer processes stepwise narrow the gate length precisely to its final value.

3. Cost Reduction

3.1 Component Shrink – High Packing Density – Plastic Packages

A key factor for cost reduction is chip shrinking. The design rules for active and passive components consider that the components are producible with sufficient yield. Progresses in process or equipment are opportunities to update the rules, which is performed permanently. Of course the maximum ratings for current density and breakthrough voltage must be taken into account. Usually there is little effect of shrinking on passive component models. Active devices should be remodeled, while special care has to be taken on thermal modeling, when shrinking the gate pitch (gate to gate distance).

Increasing the packing density may have effects on the circuit simulation that are difficult to handle. Exact models for electrical or magnetic coupling between components that are placed close to each other are not available in commercial simulation tools. To overcome this problem it is convenient to perform field simulation for some local coupling problems. Field simulation of complete MMICs still overcharges EM-simulators. It is still not possible to include active devices into EM-simulation.

SMD plastic packages are cheap and easy to handle for the application but not optimal in their RF-behavior and difficult to simulate. The model depends on bond wire length, chip size and even the location of chip via holes. The chip “ground” (backside metal) is connected to the external ground through an inductive lead. Ground current causes a voltage drop along this lead with the effect that the backside metal of the chip carries a certain RF-potential. This causes feedback across stages, which without any prevention may lead to a total degradation of the electrical behavior of the packaged MMIC.

Principally, a non perfect chip ground calls in question the models for microstrip-like components, because they generally are developed under the assumption of a perfect ground.

3.2 Design Consequences

Parasitics due to high packing density in principle are low loss capacitive and inductive effects, and experience shows that they mainly cause frequency shifts and gain slope

which usually can be compensated. The designer and layouter should be aware of these effects. Microwave skill in the layout phase helps to minimize their influence by clever chip architecture. Nevertheless these effects are difficult to be quantified. Knowing this simulation can be used to look for components which principally can compensate frequency shifts and gain slopes. If these components are designed with tuning options a method has been found to tune prototypes of the circuits experimentally.

The final component values have to be transferred to a production mask. The redesign procedure will be accelerated if the tuning options are defined late in the wafer process.

4. Future Trends

Distance radar in car traffic promises for the future similar production volumes like mobile communication today. A point of interest for this mm-wave application is flip-chip mounting and bumps for low inductive interconnections and for thermal reasons.