Focused Ion Beam Technology – A New Approach for the Sub 100 nm Microfabrication Regime

A. Lugstein, H. Wanzenböck, E. Bertagnolli

**Vienna University of Technology,
Institute of Solid State Electronics,
Semiconductor Technology,
A-1040 Vienna, Floragasse 7/1, Austria**

Focused ion beam (FIB) technology is an attractive tool for various maskless processes with the capability of structure fabrication below 100 nm. The current state of the art and the potential application for device modification, failure analysis, and process development is reviewed. The utilization of the FIB as a substantial component for fabrication and testing of metrology and the relevant electrical properties in the sub 100 nm regime is described.

1. Introduction

The focused ion beam represents a versatile tool for metrology and highly resolved 3-dimensional imaging of complex multilayer structures. Furthermore, it allows the fabrication of ultrafine structures by direct deposition of metal or insulator schemes and spatially confined doping. A minimum feature size down to 25 nm and a nesting tolerance of 10 nm could be obtained. Composite materials were selectively etched in reactive gas atmospheres achieving aspect ratios up to 100.

These characteristics are very attractive for future VLSI device processing techniques, because FIB provides the flexibility and reliability necessary for explorative work on scaled or entirely new devices. The ability to view, modify and analyze devices in the submicron range has established this technique in three major semiconductor applications of industrial relevance: device modification, failure analysis, and process monitoring.

The initial results shown prove the flexibility of the FIB for nanostructuring of microcircuits and suggest the relevance of this technique for the development of entirely new devices.

2. Experimental

All the experiments reported were performed on a Micrion 2500 FIB system operating at 50 kV acceleration voltage with a Ga liquid metal ion source (LMIS). The system allows the use of an ion beam with currents ranging from 1 pA to 11 nA, with a beam diameter of 5 nm (FWHM), respectively 500 nm (FWHM) for the high current mode. The energy of the ion beam can be varied between 15 and 50 keV in steps of 5 keV. The system has an additional charge neutralization electron flood gun system which guarantees higher beam stability and ESD prevention.

The stage allows translation of the sample ± 38 mm perpendicular to the beam, 360° continuous rotation, and tilting of the sample up to 60°.

The vacuum in the recipient ($p < 10^{-7}$ Torr) is maintained by a turbo molecular pump backed by a remote mechanical pump to guarantee hydrocarbon free vacuum.

The precursor gas for the tungsten deposition was $W(CO)_6$ respectively trimethyl-cyclotetrasiloxane (TMCTS) and oxygen for SiO_2 formation. All depositions were performed at room temperature. For enhanced etching, XeF_2 and Cl_2 could be introduced through a nozzle. The process conditions for deposition and gas assisted etching are summarized in Table 1.

Table 1: Process parameters

FIB	Gaseous component	Accel. voltage	Beam current	Minimum spot size	Pixel dwelltime	Pixel spacing
		kV	pA	nm	µs	µm
GAE (Fig. 1)	XeF_2	50	1575	100	0.5	0.15
W-depo. (Fig. 1)	$W(CO)_6$	50	700	65	0.5	0.11
GAE (Fig. 2)	Cl2	50	1575	100	0.5	0.15
W-depo. (Fig.3)	$W(CO)_6$	50	5	8	0.5	0.11

3. Measurements and Results

3.1 Device modification

This tool provides as well the potential to fabricate novel circuit layouts directly without the necessity for a sophisticated mask layout and will foster the development and introduction of new IC designs.

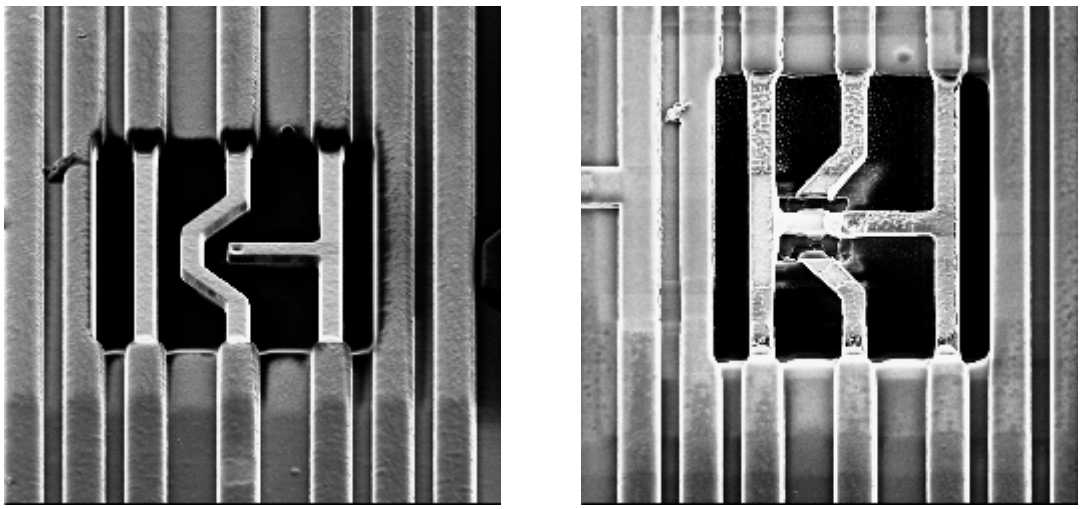


Fig. 1: Sample device modification by isolation cut and rewiring with tungsten deposition.

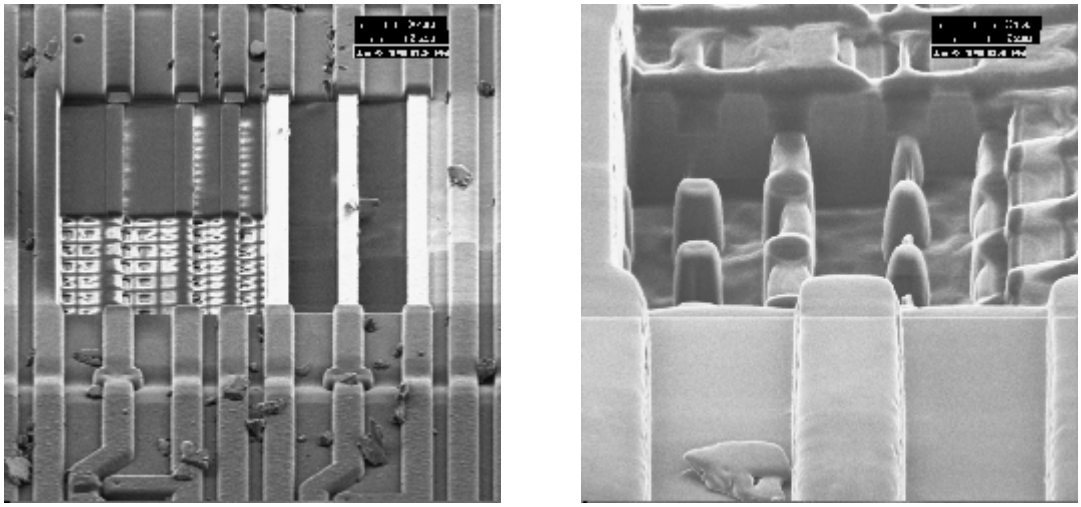
Beyond the analytical capabilities, a combination of deposition and etching steps for metals, semiconductors and insulators allows the direct construction of prototype microelectronic devices. In this operation mode the in-situ modification of circuits directly on the chip was demonstrated (Fig. 1). After the selectively removal of the passivation layer by gas assisted etching the wiring of an exemplary device was locally remodeled by first disconnecting the existing structure with subsequent redeposition of tungsten.

3.2 Failure Analysis

Failure analysis utilizes the capability of FIB technology to access and image structural details hidden beneath the surface. Knowledge of the wiring and type of the composition allows to identify the source of failure.

Using an exemplary microelectronic device the analytical feasibilities of the FIB were exploited revealing an imaging resolution down to 5 nm. By ion milling and gas assisted etching, multilayered structures could be made accessible for investigation within a few minutes and without further laborious preparation. In-situ cross-sectional imaging is highly beneficial in a multilayered fabrication sequence as it allows quick evaluation and interpretation of process steps.

Figure 2 shows a preparation sequence of an integrated circuit which was exposed to chlorine assisted sputtering. Conductive material and dielectrics could be very well distinguished by the differing contrast of the materials.



(a) (b)

Fig. 2: Sequential preparing steps of an integrated circuit: (a) Removal of passivation layer/metal lines/isolation layer, respectively; (b) cross-sectional preparation of a memory cell array.

3.3 Process development

The most attractive feature of the FIB apart from the high imaging resolution is the ability of metal and insulator deposition. Unfortunately, in all cases these deposits contain influential concentrations of carbon, and oxygen. This affects the resistivity of the deposited metal inasmuch the resistivity of FIB deposited conductors is usually higher compared to pure bulk material.

In situ annealing of the deposition by heating the substrate during the focused ion beam deposition enhances the conductivity nearly equal to the pure metal [1], [2], but could introduce thermal drifts during the deposition process leading to lower pattern accuracy. John Melngailis and coworkers [3] promote a method assigned as laser assisted focused ion beam induced deposition. Thereby a laser heats the area where the ion induced chemical vapor deposition takes place confined to the diameter of the laser beam.

Using a siloxane precursor the FIB offers the capability to deposit insulator materials by ion-beam induced chemical vapor deposition from tetramethylcyclotetrasiloxane (TMCTS) in the presence of oxygen. The variation of the partial pressure of TMCTS respectively oxygen and the variation of dwell- and refresh time allow the variation of the stoichiometric composition. Hence, insulating layers with adjustable optical and electronic properties can be evolved. Such insulating materials formed by ion beam induced CVD mainly consist of Si, O, but may contain trace impurities of Ga (from the LMIS) and C by fragmentation of the silicon precursor [4]. The optical transmittance and electrical properties of the layers are mainly controlled by the amount of enclosed Gallium.

The comprehensive understanding of the deposition process will allow to improve the electrical properties of FIB deposited insulators providing the required reliability for performing circuit modifications. Baker [4] suggested metal-insulator-metal capacitor structures with FIB insulators to test the influence of enclosed Ga with regard to resistivity and breakdown voltages.

Figure 3 displays a capacitance test structure (a) formed by SiO_2 deposition between two metal pads. This setup allows monitoring of leakage current, breakdown voltage, dielectric strength and resistivity for dielectric layers feasible.

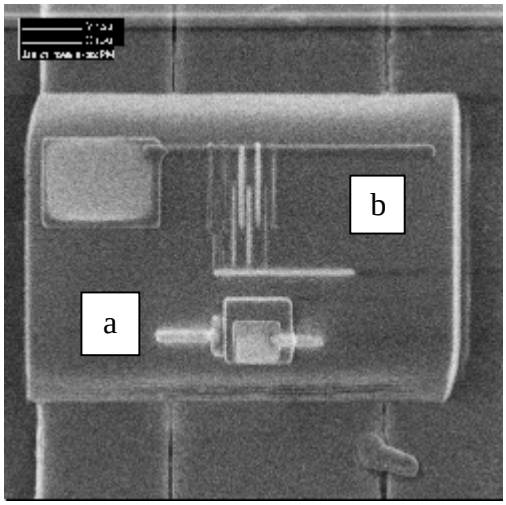


Fig. 3: Capacitor test structure (a) and interdigitated tungsten-fingers (b) with a 220 nm pitch placed on an in situ generated SiO_2 pad.

In general, new materials will be occasionally introduced and the deposition process needs to be adapted in respect to the available precursors, beam energy, refresh- and dwelltime etc. to achieve the desired resistance, dielectric strength, contact resistance and interconnect properties (ohmic or rectifying).

The installation of routine test vehicles is projected for systematic investigation of the morphological and electrical features obtained for specific deposition parameters. The deposition process was found to strongly affect the line width, nesting tolerance, contact hole sizes, etc., and yield of structures. Unified test vehicles provide a suitable mean for gaining a thorough understanding of the complex deposition mechanism.

First test structures (Fig. 3) fabricated by FIB deposition were interdigitated fingers with a 220 nm pitch (b) and metal-insulator-metal capacitor structure (a) to determine conductor to conductor shorts, surface and interfacial leakage currents respectively the dielectric strength of the SiO_2 layer. The highest performance in resolution and pattering achievable was 5 nm respectively 30 nm.

3.4 Shallow implantation

Recent applications of FIB for semiconductor devices focus on an optimized MOSFET (FIBMOS) using the localized beam to fabricate a unique, laterally tailored doping profile along the channel. The arrangement of Ga-LMIS in combination with the high resolution ion column and adjustable beam energy in the range from 50 keV to 15 keV allows generating a strategically placed ultrashallow doping profile with tolerable crystal distortion. Former investigations [5] confirmed that the output resistance improves, detrimental hot electron effects diminish and threshold voltage stabilizes as channel length is reduced, which in general leads to significantly better device performance.

4. Conclusion

Concluding the presented material illustrates the potential of FIB for metrology and highly resolved 3-dimensional imaging of complex multilayer structures. Spatially confined doping and deposition of metal as well as insulating layers was demonstrated in spatially confined areas in the nm range. Concluding, FIB is a prospective tool for the improvement of high-frequency devices as well as fabrication of entirely new circuits.

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