# High Speed Data Converters and New Telecommunication Needs

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Recent technology improvements are leading to significant advances in telecommunications. New sub-micron technologies allow us to design high speed digital processors and high-speed, high-resolution data converters. These basic components push the analog-digital border close to the antenna and favor the implementation of complex digital algorithms. Various system architectures are examined and key data converter specifications are established. Then, the design techniques and the linearization methods that make possible the implementation of the required specifications are discussed.

## 1. Introduction

Many of the applications that are benefiting significantly from progress in microelectronics belong to the communication area. We are enjoying a tremendous growth in mobile communication: new services are being constantly introduced thanks to the availability of high speed data communication. This progress results from two key components: the DSP and the data converter. Using sub-sub-micron technologies it is possible to integrate millions of transistors on a single chip. The speed of digital circuits is increasing up to many hundreds of MHz. Hence, new DSP architectures allow complex algorithms to be implemented at very high computation speeds. However, analog-digital interfaces must be able to match the resolution and the speed of the DSP. Therefore, the second key component completing the basic design set is the high speed and high resolution data converter [1].

The present trend pushing the border of digital conversion towards the transmit and receive terminal leads to ever increasing demands on specifications, namely speed and resolution. We will see that often more than 14 bits and hundred of MHz are necessary. In addition, many applications require continuous reductions in power consumption. As a result, market challenges favor research on high speed data converters. In turn, the results achieved lead to new architectural solutions which create new needs. This paper analyses this process and discusses recent circuit solutions suitable for meeting key system specifications.

## 2. Communication Systems

We can use three main transmission media for analog communication and for data transfer: wireless, twisted-pair cable and coaxial cable. Optic fibers can also be employed, but their high cost make their use suitable only for backbone networks. For data communication, it is possible to utilize either narrow-band connections (up to 56 kb/s)

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or broadband connections (like the T-1 service operating at 1.544 Mb/s). Around the options of media and bandwidth, communication engineers can build many possible architectures. We shall see that in many of them, data converters have a significant role.

For narrow-band wireless we have different standards around the world. In Europe we have the GSM operating in two different frequency bands: 900 and 1800 MHz (GSM 900 and GSM 1800). In the USA we have various mobile radio standards in the 1800 MHz frequency band. The most popular are the PSC 1900, D-AMPS and QUALCOMM CMDA. In Japan the standard used is PDC but another one, the IS-95, is about to be installed. The present scenario is such that, despite the considerable effort spent on standardization, it will be hard to establish a unique worldwide standard for future mobile radio systems. Consequently, managing multiple standards will be ever more necessary creating difficulties to both manufacturers and operators.

Significant help can come from the so-called "software radio" approach [2]. Figure 1 shows the "ideal" software radio solution: a high speed data converter digitizes the RF signal directly at the antenna with all radio functions being performed in the digital domain possibly using a specialized reconfigurable hardware. At present, because of the obvious difficulties in the implementation of the "ideal" solution, the data converter is moved after some analog pre-processing. This is done typically after the low noise amplifier and a first mixing (Fig. 2, showing the Rx section).

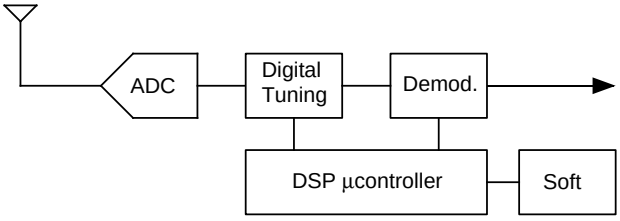


Fig. 1: Ideal software radio.

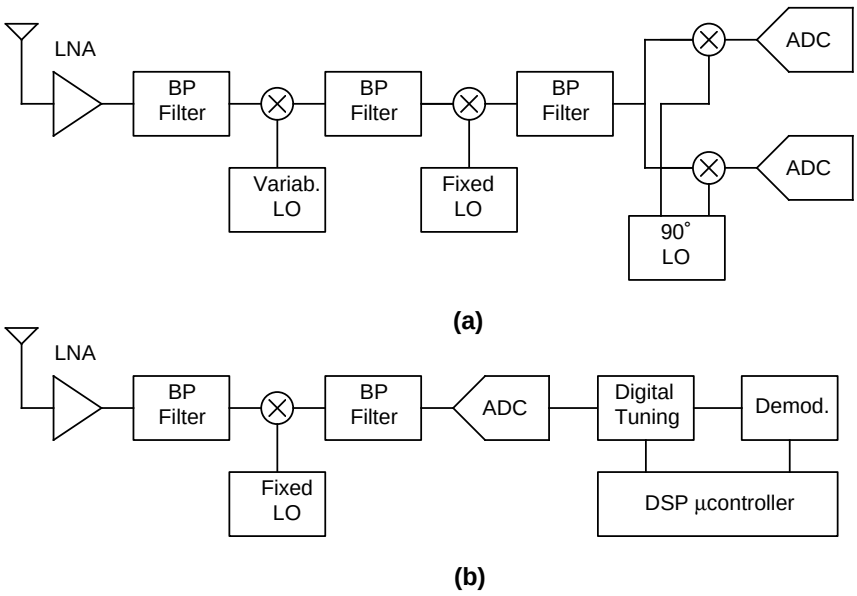


Fig. 2: (a) Conventional architecture of a receive radio; (b) software radio improvement.

More generally, software radio envisages a base station platform with reconfigurable hardware and software. This architecture can be adapted to different standards or services simply by using the appropriate software. Software radio offers many advantages: it is flexible, allows new services to be added quickly thus shortening the time-to-market, offers better management of logistics, maintenance and personnel training. Moreover, software radio permits migration from one standard to the successive generation along an evolutionary path.

About data converters observe that, since channel tuning is performed in the digital domain, the linearity of the converter must be such as to avoid any spurious interference. Fortunately the bandwidth licensed to operators is limited, typically under 10 – 15 MHz. Therefore, appropriate choice of the LO frequency and the sampling frequency of data converters allows some system flexibility that can place images and spurious signals out of band. Thus, data converter specifications depend on the architecture and standard adopted. For modern architectures they span from 12 to 16 bit with spurious performances around 100 dB. The sampling frequency ranges from 60 to 80 MHz.

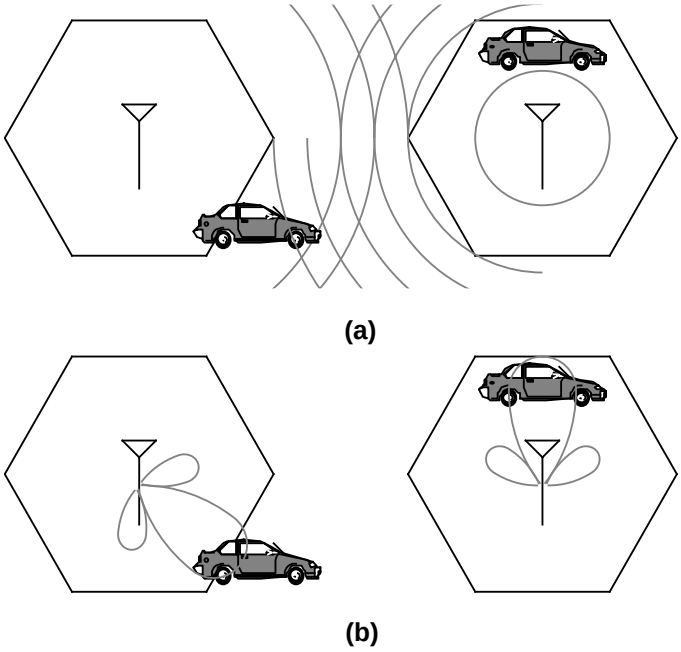


Fig. 3: (a) Omnidirectional antenna; (b) smart antenna.

In cellular communication, important features are coverage, capacity, and service quality. In rural areas ensuring a proper coverage is expensive, in urban areas the capacity is often close to average demand. Moreover, interference from neighbor cells worsens service quality. Smart antennas provide an answer to these problems [3], [4]. A smart antenna is a directional antenna used in the base station to track mobile terminals (Fig. 3). The basic structure uses a switched-beam or an adaptive array architecture. Two or more antenna elements are spatially arranged and the signals are properly processed to produce a directional radiation pattern.

In its simplest form, a smart antenna uses a fixed phase beam network that is switched to the elements of the array so as to produce a beam closer to the desired direction. In the phased array the phases of signals are adjusted to change the array pattern, thus tracking a given mobile or canceling a given interference signal.

Here, different strategies for rural or urban areas are necessary. Therefore, adaptive and reconfigurable architectures are the best solution. Figure 4 shows the block diagram of a possible "digital" implementation. The architecture uses a weight-adjustment algorithm to obtain IF beam-forming. Of course the given architecture is only one possibility, we could design a solution fully in the analog domain. Nevertheless, the digital approach, thanks to the use of the data converter in the IF section, permits complex beam-forming with a digital processor. Therefore, the availability of data converters which answer system requirements leads us to an adaptive system providing superior performance.

The data converter specifications depend on the IF frequency used. Even for these applications the resolution depends on the width of the bandwidth granted to a given provider. In the case of 10 MHz we can satisfy the GSM specifications (receive side) with an 81 dB dynamic range (13.5 bit) and a 97 dB SFDR. Moreover, the clock jitter must be kept below 2 ps. The above figures assume an IF frequency of 70 MHz. More relaxed figures result when considering other standards like the DCS 1800.

Broadband communication offers many examples of architectures that exploit data converters and DSP. Through the already installed copper twisted-pair phone lines it is possible to provide broadband digital services. We have various possibilities, the ADSL (Asymmetric Digital Subscriber Line), HDSL (High speed), the RADSL (Rate Adaptive) and the VDSL (Very high speed). The first class runs at a data rate of up to 8 Mb/s in the downstream direction (from the central office to the subscriber) and up to 1 Mb/s in the upstream direction. The distance from the central office to the subscriber, however, must be a maximum of 5 km. The VDSL service is more advanced, it can provide a data rate as high as 52 Mb/s. The architecture provides a fiber optical connection from the central office to the neighborhood of a group of customers (Optical network Unit, ONU). The connection from the ONU to the subscriber is through a short link (not more than 1200 m) of twisted-pair copper wire [5].

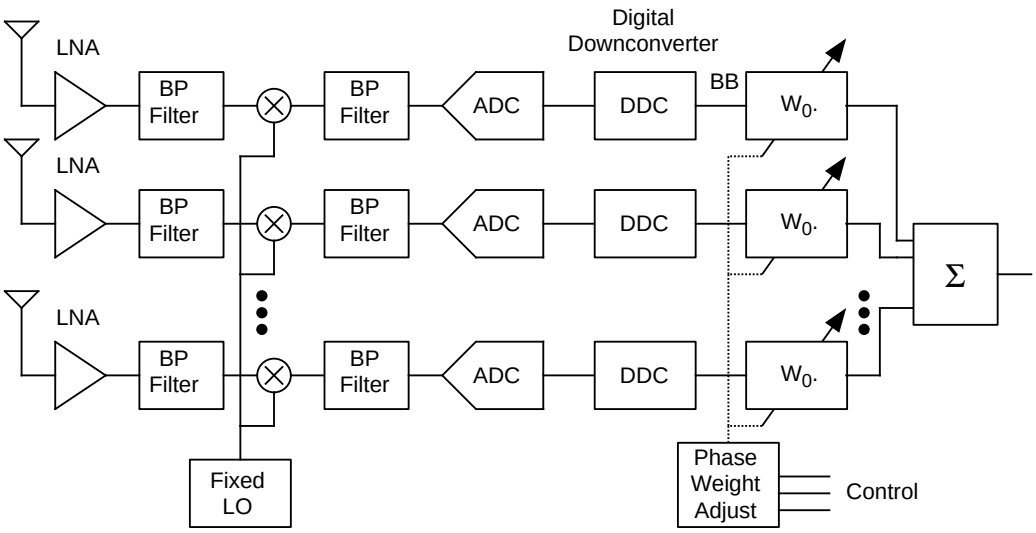


Fig. 4: Architecture of a digital smart antenna.

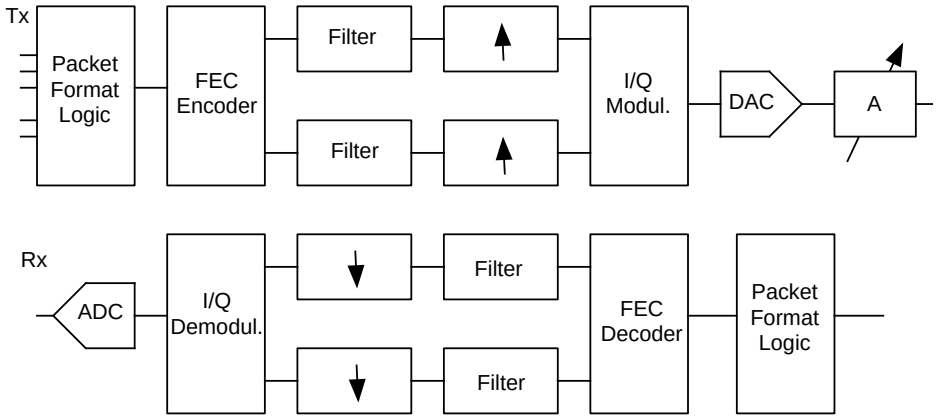


Fig. 5: Architecture of a VDSL transceiver.

The above features are made possible by complex modulation schemes and the relatively high bandwidth of twisted-pair wires (much higher than the 3 kHz filtered voiced channel). An example of VDSL architecture is shown in Fig. 5 [6]. Note that it includes an A/D and a D/A converter very close to the twisted-pair connection. For the ADSL architecture the sampling rate in the two links is 8 – 10 MHz and the required resolution is 12 – 14 bits. For VSDL architectures the resolution required is a bit lower but the sampling rate must be programmable from 1 MHz to 52 MHz.

## 3. High Speed Data Converters

High speed of operation can be achieved with advanced modern technologies. Submicron CMOS and advanced BiCMOS or SiGe permit bandwidths in the order of many GHz. Therefore, speed is an issue that can be satisfactorily addressed by exploiting the available technology. In contrast, accuracy depends on the components' precision and on practical limits related to circuit implementation. Therefore, the processes used, as well as deep-submicron line widths, should also provide precise resistors and capacitors. Moreover, the analog critical nodes must be conveniently protected from spur signals and noise. This demand imposes additional steps on the process: it is necessary to utilize, for example, multiple diffused wells, trench separation, or migrate toward SOI technologies. All these actions are only beneficial, however, when more than 10 – 12 bits are required. For higher resolution the best way to get rid of inaccuracy is to use calibration.

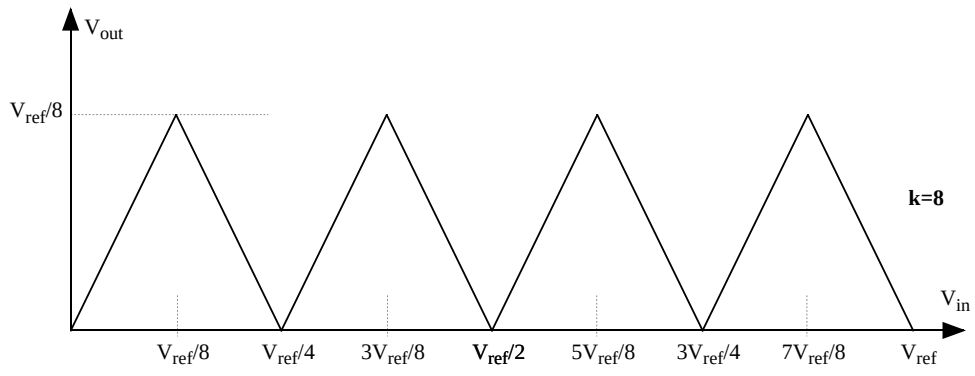


Fig. 6: Folding transfer characteristics.

The simplest manner to achieve high speed is to use one step or two step flash architectures. The flash technique has been used extensively in the past; however, various limitations do not allow us to step outside the 10 bit limit [7]. Another approach is the folding and interpolation technique. Folding consists in nonlinear input processing that produces an output characteristic like the one shown in Fig. 6. The number of foldings performed determines the MSBs (3 bits for the figure). Subsequent data conversion determines additional LSBs. Folding is often associated with interpolation: a suitable network processes two folded outputs and produces transition levels intermediate to the one given by the folding transformation. We can thus extract additional bits at a reduced cost. An example of folding and interpolation architecture is given in [8]. The circuit achieves 10 bits and 40 MS/s using a 7 GHz 0.6 µm CMOS technology.

As mentioned above, it is necessary to use calibration when pursuing more than 10 – 12 bits of accuracy. Various calibration algorithms have been proposed. Some of them correct possible mismatches in the analog domain. For example, if two capacitors must be equal, the difference due to technological mismatch can be adjusted with a binary programmable capacitor array. Other methods measure the analog mismatch and store the information in memory to digitally correct the result achieved afterwards. All these techniques require a calibration/correction cycle, often performed at power-on. Alternatively, it is possible to use a queue-based architecture able to generate time-slots which allocate the calibration cycle without disturbing the conversion operation [9].

Designers widely use pipeline architectures for communication needs: the pipeline solution properly suits speed requirements and digital calibration demands. Fig. 7 shows a typical pipeline scheme. A number of equal cells compose the structure. Each cell provides a given number of bits at the output (say, N) and residual error. The next cell processes the residual error, performs digital conversion and gives another residual error. The output of the DAC is the combination of the bits from each stage of the pipeline. Since the dynamic range of the residual error is smaller than the input by a factor $2^N$, many architectures foresee an amplification of the residual error by the same factor to keep the dynamic range constant along the pipeline. Possible errors are normally corrected digitally. Each stage of the pipeline provides the digital information with some redundancy (for a 1 bit per stage architecture, a 0.5 additional bit). Redundancy avoids loss of information even in the presence of error and permits to fully cancel inaccuracies.

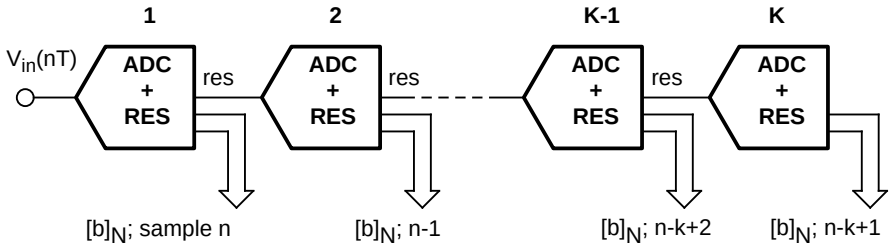


Fig. 7: Pipeline architecture.

Alternative digital calibration methods are proposed in [10] (Fig. 8).Transcoding RAMs useful in correcting converter non-linearities are used. This solution is common to many digital calibration methods. The point is how to generate the transcoding curve. Two methods are proposed. The first one is for off-line correction and the second one acts concurrently with the normal converter operation (on-line).

We can observe that the transcoding operation is not only useful to correct non-linearities, but we can also achieve a precise representation of the transitions between the quantization channels. For this reason the ROM must have more bits than the address does. Hence, thanks to careful correction of the integral non-linearity, we can significantly improve the SFDR. The first scheme in Fig. 8 requires a training-calibration cycle, possibly replacing testing after fabrication. A sine-wave enters the data converter and the output histogram allows the transfer characteristic to be extracted. To this end, the same technique proposed for testing data converters dynamically is used [11].

The second scheme employs an auxiliary conversion channel. It runs at a lower frequency than the main channel. The lower clock rate ensures higher accuracy, thus providing the calibration term necessary for updating the transcoding memory. The algorithm used ensures accuracy and a suitable management of the two multiplexed RAM. Moreover, it is necessary to use a high speed high accuracy track and hold at the input of the system. Observe that the performance of this block limits the performance of the entire system. However, it is possible to achieve excellent linearity (up to 14 – 15 bits) while using clock frequencies up to 100 MHz [12].

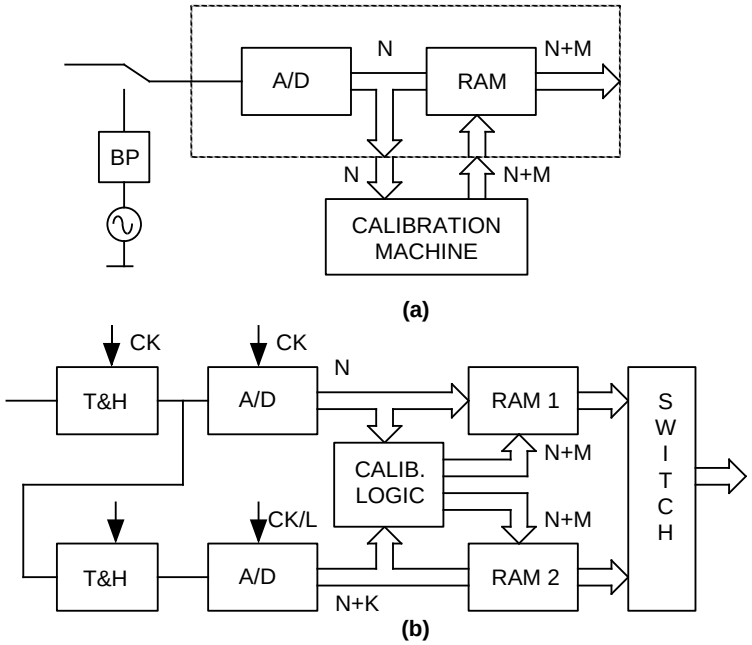


Fig. 8: (a) Off-line and (b) on-line digital calibration.

## 4. Conclusions

We have seen that the tremendous pace in telecommunication developments affects (and is produced by) improvements in data converter performance. We have a combination of technological advances and novel architectures. Typically, benefits come from an extensive use of digital correction and calibration. Therefore, we can talk about a new approach for achieving high performance: using “digitally assisted” data converters.

The market already offers data converters running at 100 Mb/s with 14 bit resolutions and a SFDR of 100 dB. The technology used is, in some cases, complex. Nevertheless,

progress in CMOS processes will soon make available 0.18 µm technologies with migration to the 0.15 µm mark by the year 2000. It is expected that 0.09 µm effective channel length will be achieved by 2001 and 0.07 µm by 2004. If these features are combined with a suitable defense from spur interference 18-bit, 200 Mb/s data converters capable of answering a wide spectrum of telecommunication needs will be on the market by the first decade of the next century.

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