Modulation Doped $Si/Si_{1-x}Ge_x$-Field-Effect Transistors

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Modulation doped $Si/Si_{1-x}Ge_x$ samples show high electron mobilities because of the motion of the carriers along a crystalline heterointerface and the absence of ionized impurities in the conduction channel. We present the methods and technologies that are applied at our institute to fabricate field-effect transistors on MBE-grown modulation doped $Si/Si_{1-x}Ge_x$ substrates. Ion implantation is used to form highly doped regions in the substrate; metal evaporation then realizes ohmic source and drain contacts on the implanted regions, and Schottky gates on unimplanted regions. In a following mesa process, reactive ion etching (RIE) is used to isolate the devices on the substrate laterally. The complete transistor process requires six lithographic steps. We employ optical contact lithography for structures down to 0.5 µm and electron-beam lithography for gate lengths <0.5µm. By incorporation of a variety of test structures in our process, we are able to derive the essential device and process parameters after each technology step. For these characterizations we use an HP 4155 semiconductor parameter analyzer and an HP 4284 LCR-meter in connection with an on-wafer prober.

1. Introduction

In a modulation doped $Si/Si_{1-x}Ge_x$ heterostructure, a 2-dimensional electron gas (2DEG) is formed which shows much higher mobilities than the 2DEG in a conventional SiO_2/Si heterostructure [1]. This is for one due to the fact that the charge carriers move along a crystalline heterointerface instead of an amorphous one. In addition, by modulation doping, the doping layer is spatially separated from the conduction channel, so free electrons are provided without having ionized impurities in the conduction path.

Our aim is to test the device applications of modulation doped $Si/Si_{1-x}Ge_x$ heterostructures grown by MBE at our institute. For this purpose we process several test structures up to a modulation doped field-effect transistor (MODFET). These fabrication processes consist of different technological steps [2] which have to be controlled and optimized with respect to the device and process parameters. In this outline we describe the technological steps that are necessary, as well as the different test structures which we employ to get information about our samples.

2. Technological Background

A field-effect transistor requires two kinds of contacts, nonrectifying ohmic contacts and well rectifying Schottky contacts. For an ohmic metal-semiconductor contact, the semiconductor has to be highly doped, so the charge carriers can tunnel through the Schottky barrier. This doping procedure is done by ion implantation, where the ionized dopants are accelerated toward the sample. The doping profile depth is then a function

of the initial kinetic energy of the ions. In a following rapid thermal annealing step, the spatially destroyed lattice is rebuilt and the dopants become electrically active. Metal evaporation then realizes ohmic source and drain contacts on implanted regions and Schottky gate contacts on unimplanted regions of the sample.

When processing several device structures on one sample, they need to be isolated laterally. For this we apply a mesa structuring that defines the shapes of the devices and prevents electrical contacts via the 2DEG between them. This mesa structuring is done by reactive ion etching (RIE), where the Si and SiGe layers are dry-etched in an SF_6 or CF_4 plasma process.

Every technological step requires a mask structuring of the sample, so that only certain regions of it are prepared while the other regions are shadowed. We employ optical contact lithography for the masking process. A photoresist is applied to the sample and illuminated through a photomask. The illuminated regions of the resist can then be removed in the developing process, the remaining resist saves the underlying sample from the technological processing. With these methods of optical lithography it is possible to process Gate lengths of down to 0.5 µm. For preparing smaller Gate lengths, e.g. for high-frequency applications, electron beam lithography is used.

3. Fabrication of Test Devices

To test the material properties of our MBE-grown modulation doped $Si/Si_{1-x}Ge_x$ heterostructures, we developed a simple fabrication process for a MODFET together with different test structures and devices. The complete process requires six lithographic steps, for which we designed a series of masks [3]. These masks are defining the regions on the sample that are implanted, evaporated or etched. They contain the MODFET Source, Drain and Gate contacts, different Hall bars with optional Gates and various test structures to control and optimize single aspects of the whole process (Fig. 1).

For Hall measurements of our samples, two Hall bars of different sizes and a square Van-der-Pauw geometry are prepared. The Hall bars can have optional gates to control the density of charge carriers in the conduction channel. With a transmission line it is possible to evaluate the ohmic contact resistances and the sheet resistance of the conduction channel. The Schottky diodes allow the measurement of the Schottky barrier height of the gate contacts and the leakage currents around the mesa etched structure. On a transistor flute with varying gate lengths the saturation drift velocity of the charge carriers ban be evaluated.

The transistor fields contain several MODFET structures with different gate lengths. A completely-processed transistor with a gate length of 1 µm is shown in Fig. 2. At these structures we derive the transistor parameters and so the direct device application of our samples as a MODFET. For all of the mentioned characterizations we use an HP 4155 semiconductor parameter analyzer and an HP 4284 LCR-meter in connection with an on-wafer prober. The I-V characteristics for a MODFET with a 1 µm Gate are shown in Fig. 3.

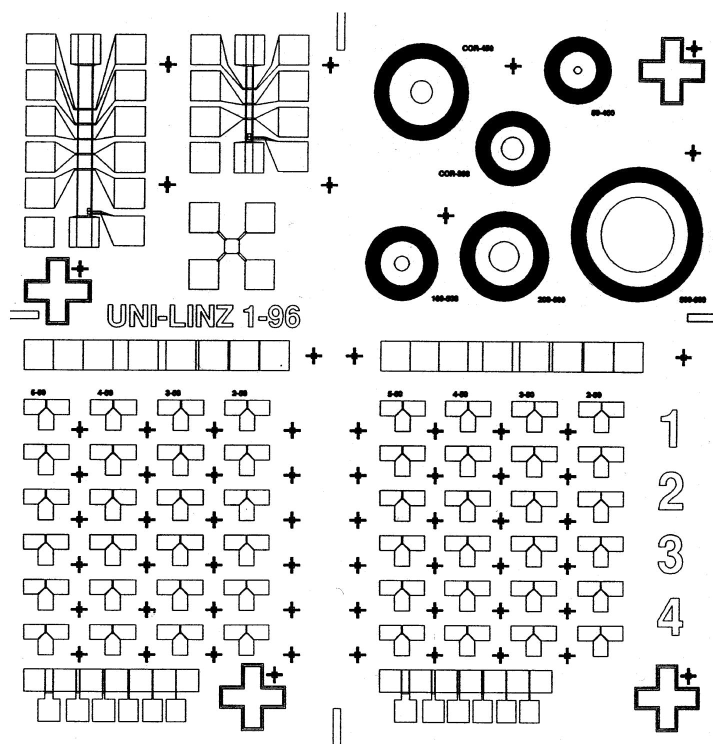

Fig. 1: Overlay of the masks for our MODFET process with six lithographic steps. In the upper left corner the Hall structures are placed, in the upper right corner the Schottky diodes. In the middle there are the transmission lines. The lower half shows the transistor fields and the transistor flutes.

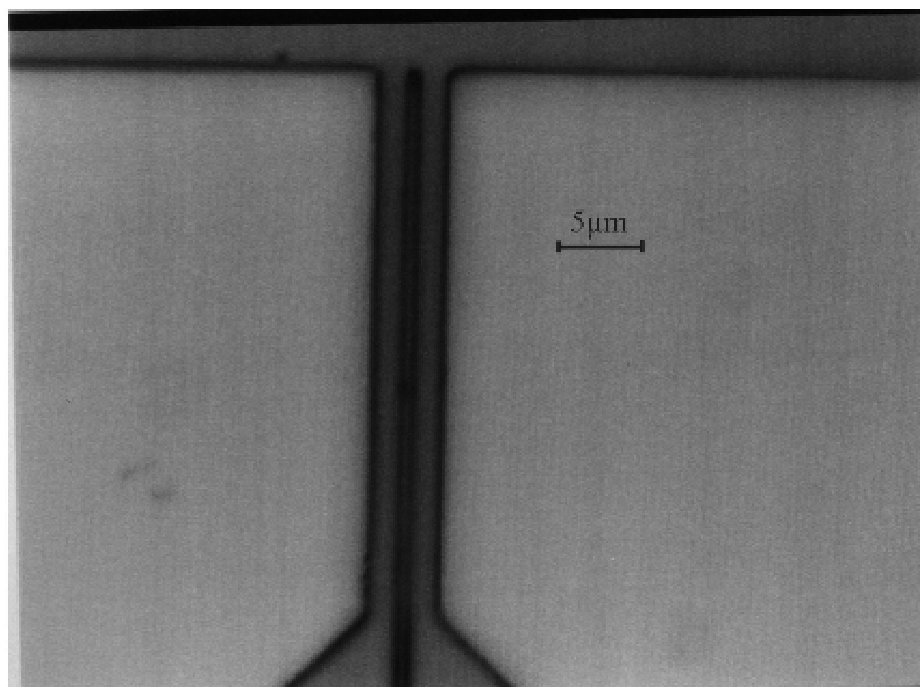

Fig. 2: MODFET with a gate length of 1µm. It is processed on a modulation doped Si/SiGe sample ZSG365 grown by MBE in Linz.

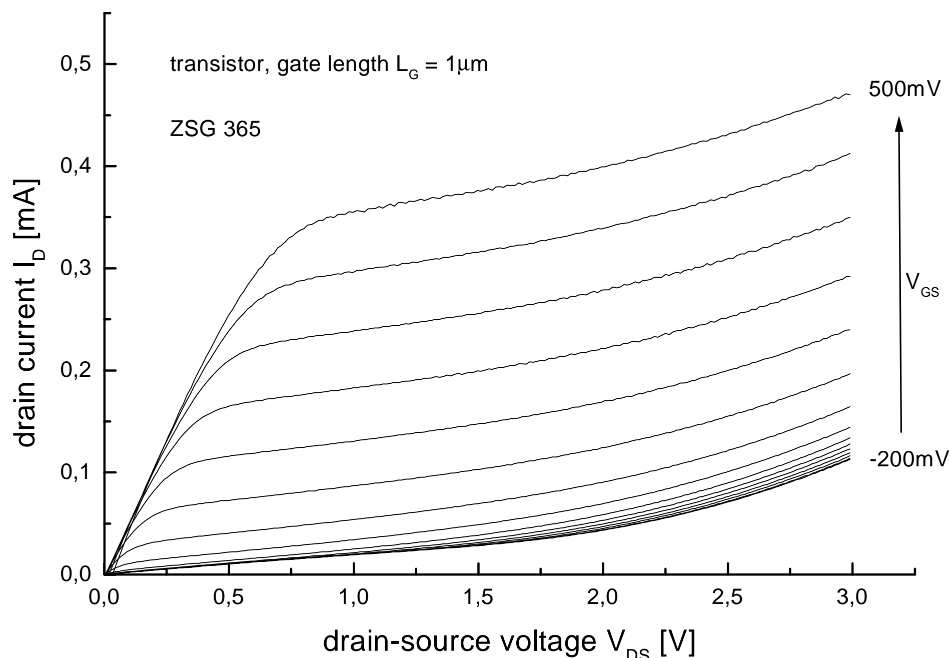

Fig. 3: I-V characteristics of a MODFET with a gate length of 1 µm. This transistor is working in an enhancement mode, so the gate voltage V_{GS} has to be increased.

4. Conclusions

We employ a technological process that allows us to derive the essential material and device parameters of our modulation doped Si/SiGe heterostructures. The test structures and devices can be fabricated in a short time and offer many possibilities for a complete characterization. The device processing can be advanced to Gate lengths <0.5 µm by electron beam lithography, e.g. for high-frequency applications.

Acknowledgements

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