Development of a SiGe BiCMOS Process for ASIC Applications

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1. Introduction

As one of the leading ASIC producers in Europe Austria Microsystems Int. AG has entered the area of high frequency capable processes with introducing a BiCMOS platform in 1993. Today BiCMOS technology comprises 1.2µm, 0.8µm, and 0.6µm processes with a wide range of design features. Based on this platform, Austria Microsystems Int. AG has developed in cooperation with SiGe Microsystems Technology Inc. a SiGe based HBT BiCMOS platform. The HBT process is now in its final stage with qualification, and multi project wafer access is available in mid-1999.

2. Key Design Features of the BiCMOS Process

- N and P buried layer with epi-silicon layer;
- Deep sinker;
- Fast poly-silicon Emitter NPN bipolar transistors (F_T 8 / 12 / 16 GHz);
- Lateral PNP transistors;
- Various resistor types poly resistors: 20 Ohm / 70 Ohm / 1.2 kOhm;
- Poly 1 to sinker capacitors;
- High capacitance poly-poly capacitors (up to 1.75 fF/µm²);
- F_T 16 – 18 GHz (0.6µm process);
- CMOS design compatibility;
- well characterized metal inductors.

In order to go beyond 18 GHz reached in conventional Si-technology AMS started to develop in cooperation with SiGe Microsystems a silicon-germanium process (hetero-junction bipolar transistor) targeting at F_T, $F_{max} > 30$ GHz [1].

[1] F_{max}: frequency at which unilateral power gain drops to unity;
F_T: frequency at which beta drops to unity when no load is connected to collector

$$F_{max} = \left[\frac{f_t}{8 * \pi * R_B * C_{BC}} \right]^{1/2}$$

R_B … Base resistance ; C_{BC} … collector/base junction

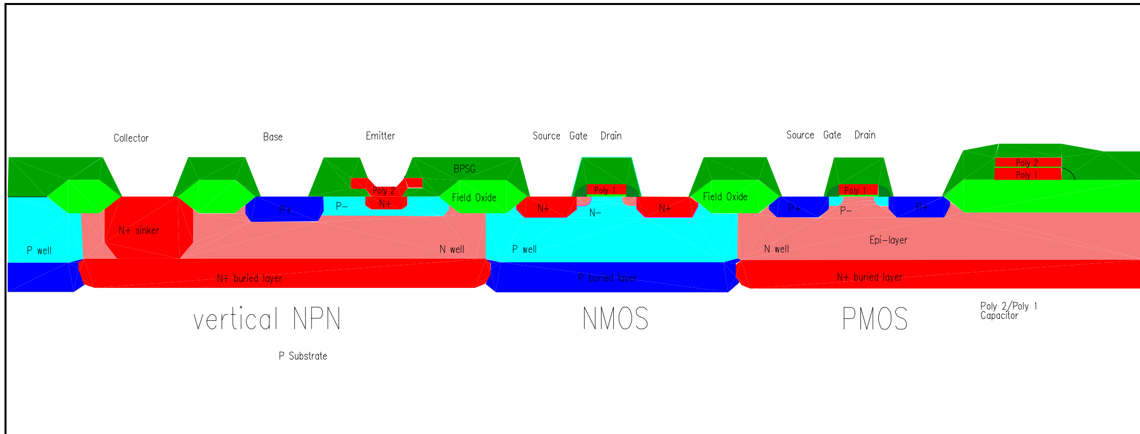

Fig 1: Schematic cross-section of BiCMOS process

Inherent to the operation of bipolar junction transistors (BJT) is the requirement of a low doped base to achieve high current-gain values. A low doped base on the other hand is in conflict with a good HF performance of the device. This contradiction can be resolved by the heterojunction bipolar transistors (HBT). In HBTs the effective doping concentration in a high doped base is kept low by means of the increased intrinsic carrier concentration caused by the bandgap difference between Si and SiGe. This yields an increased collector current (→ increased beta) compared to BJTs.

$$J_C = \frac{\mu q k T}{\int_x^W \frac{N_A(x)}{n_i^2(x)} dx} * \exp\left(\frac{qV_{BE}}{kT}\right) \qquad \text{(Moll–Ross relation)}$$

n_i^2 ... intrinsic carrier concentration

N_A ... base doping

The integration chosen follows a drift transistor approach where the germanium concentration increases linearly (graded Ge profile) from the emitter/base to the base/collector junction (Fig. 2). This concept results in a reduced base transit time which is the major component in the in the transistor delay terms. The graded Ge profile shows an improved Early voltage compared to HBTs with constant Ge profile through out the base (true HBT) whereas the true HBT concept is superior in current gain.

Since the Austria Microsystems Int. AG BiCMOS technology has been well acknowledged by various customers it was imperative to keep the changes in process flow to a minimum when integrating the HBT module in order to guarantee constant process parameters. The integration of SiGe stack could be accomplished with two additional masks compared to the standard BiCMOS platform.

To give an example of the optimization work in the development process I will focus on the collector/base junction. The base collector depletion-zone transit time (τ_{BC}) is for high speed transistors a decisive delay factor. To keep its value small a high collector doping (N_D) is needed. This is contrasted by the necessity of a low N_D to reduce the base/collector capacitance. A high breakdown voltage of the base/collector junction asks for a low doped collector. Optimizing this problem under the given constraints is best done by a pedestal collector implant (SIC) giving F_{max} values around 30 GHz.

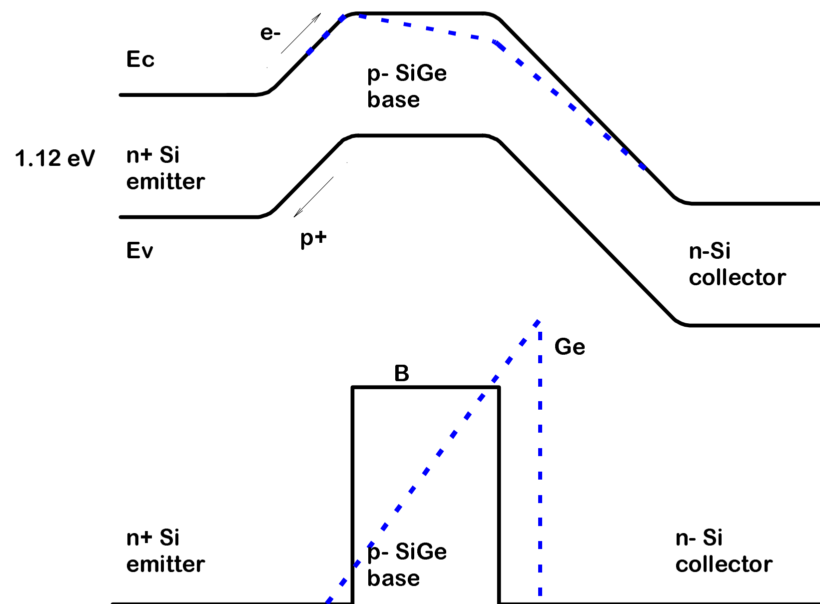

Fig. 2: Band structure diagrams of a conventional Si-NPN bipolar transistor and a modified bandgap of a SiGe NPN-HBTs. The implementation of a graded SiGe-layer reduces the bandgap and leads to a drift acceleration of the electrons.

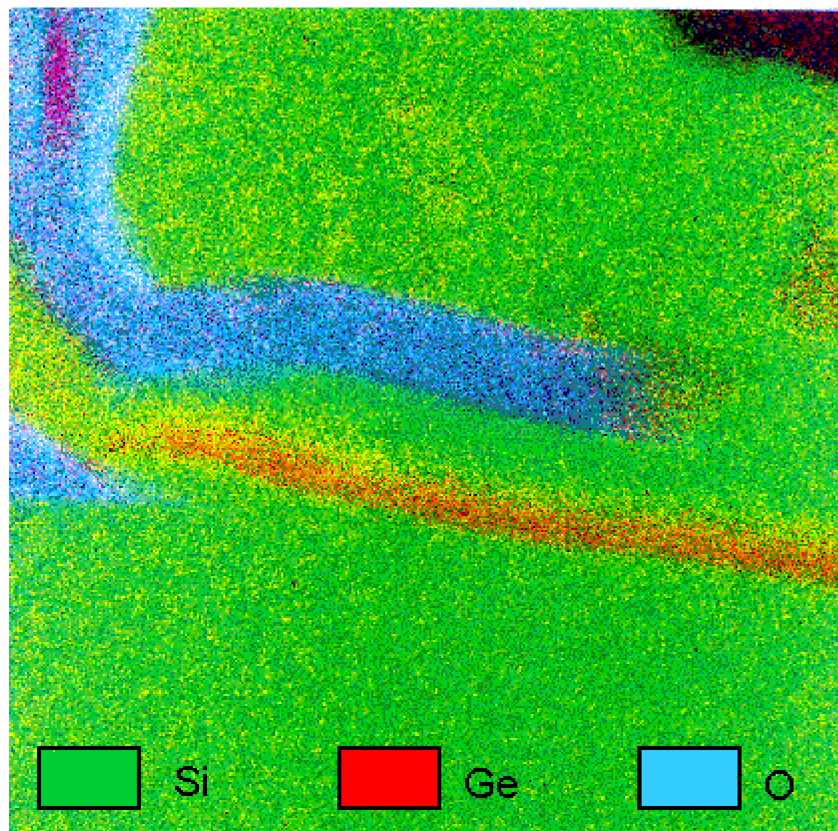

Fig. 3: Transmission electron microscope (TEM) picture with electron energy loss (EELS) analyzer. The picture shows the germanium enriched area in the base.

Trade-offs at collector/base junction:

⇑ ... high	⇓ ... low					
⇓	τ_{BC}	→	N_D	⇑		
⇓	C_{BC}	→	yields high F_{max}	→	N_D	⇓
⇑	BV_{CBO}	→	N_D	⇓	Ionization in Si (”wide gap material”)	
⇒	optimized		**Selective Implanted Collector (SIC)**			

Tab. 1: Trade-offs at collector/base junction.

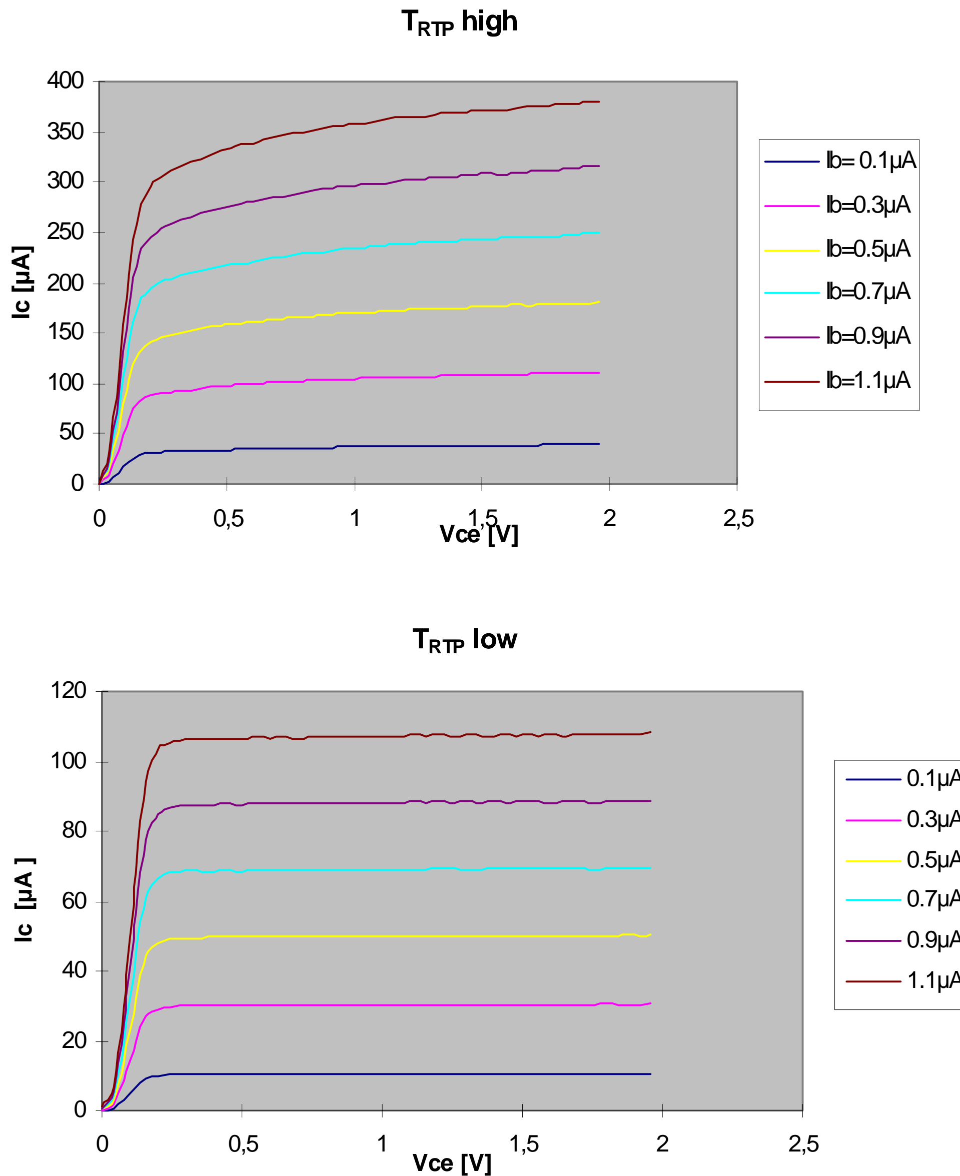

Fig 4 : Shows the dependence of output characteristics Ic vs. Vce on thermal stress (T_{RTP}) due to processing. Note the change in Early voltage.

An other crucial design issue is the alignment of the boron and the germanium profile in the base. Misalignment leads to degradation in device performance seen in a ruined Early voltage and current gain variations. These problems are cured by stringent control over the thermal budget seen by the wafer during processing (Fig. 4).

As a result of this integration a HBT BiCMOS process has been developed and brought to production maturity. This process features all standard BiCMOS process elements like full CMOS design compatibility, various poly resistors, high capacitance poly/poly capacitors, a.s.o. together with SiGe based drift HBTs with F_T's of 30 – 40 GHz, F_{max} of 25 – 35 GHz, low base resistance, and high Early voltage.