GMe

CURRENT DEVELOPMENTS OF MICROELECTRONICS

PROCEEDINGS OF THE SEMINAR
"AKTUELLE ENTWICKLUNGEN DER MIKROELEKTRONIK"
IN BAD HOFGASTEIN/SALZBURG

ORGANIZED BY THE SOCIETY FOR MICROELECTRONICS
(GESELLSCHAFT FÜR MIKROELEKTRONIK – GMe)

3 March 1999 – 6 March 1999

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3 March 1999 – 6 March 1999

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Preface

In spring 1977, the first Austrian microelectronics technology seminar took place in Grossarl, Salzburg, under the title "*Technologie in der Mikroelektronik*" ("*Technology in Microelectronics*"). A long series of biennial seminars in Grossarl followed, the first of which were organized by a group of institutes at the Technical University Vienna. Later, after the Society for Microelectronics (*Gesellschaft für Mikroelektronik*; GMe) had been founded in the mid-1980s, the GMe coordinated the seminars. This sequence of seminars is continued in 1999 with a new venue, Bad Hofgastein, and a new title, "*Current Developments of Microelectronics*".

The main goal of the Society for Microelectronics is to promote microelectronics research and technology at Austrian universities and to establish links to the Austrian industry. The GMe is essentially financed by the government and supports relevant microelectronics activities at Austrian universities. The relatively small budget of the GMe prohibits the full sponsoring of research projects; nevertheless, the GMe supplements other research funding sources by providing contributions for creating and maintaining laboratory infra-structure. In addition to support for other technological activities in the fields of design, sensors, and optoelectronics, the main goal of the GMe in recent years was the support of the two cleanroom centers at the Technical University Vienna and at the University Linz, respectively, where internationally competitive technological equipment has been made available to researchers and students.

With the change of the seminar venue from Grossarl to Bad Hofgastein the scope of the seminar shifted: Great efforts had been made particularly in recent years to invite guest speakers from industry or foreign universities, but due to the rather restrictive limitations of the former seminar facilities in Grossarl, the audience consisted practically exclusively of university researchers, and the presentations were designed as university research reports. The 1999 seminar in Bad Hofgastein, in contrast, appeals to a more application-oriented audience. Most of the oral presentations are review papers presented by top-level speakers from international industry and research facilities. The institutions supported by the GMe also present their results, partly as oral presentations but mostly as posters.

We hope that the proceedings will promote the impact of our seminar and that they may contribute to an even better international cooperation of the Austrian microelectronics researchers.

Univ.Prof. Dr. Erich GORNIK
President of the GMe

Ao.Univ.Prof. Dr. Karl RIEDLING
Secretary General of the GMe

Seminar Program

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High Frequency Systems

HF-Technologie- und Schaltungskonzepte für Mobilfunkanwendungen

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1. Einleitung

Mobile digitale Funkgeräte wie Handies oder Schnurlostelefone sind aus der heutigen Welt nicht mehr wegzudenken. Das auf dem GSM-Standard beruhende zellulare Mobilfunknetz hat seit seiner Einführung im Jahre 1992 Europa erobert und sich in mehr als 120 Ländern in der Welt etabliert [1]. Vom noch recht unhandlichen Statussymbol haben sie sich in wenigen Jahren zum kleinen und leichten Arbeitsgerät mit vielfältigen Zusatzfunktionen entwickelt. Beruhten die früheren analogen Geräte, meist reine Autotelefone, noch auf einer Vielzahl meist regionaler, untereinander inkompatibler Standards, so geht die Entwicklung heute in Richtung von global einsetzbaren universellen Kommunikationsgeräten.

In diesem Beitrag, dessen Schwerpunkt auf der Wechselbeziehung von Geräte- und Technologieentwicklung liegt, soll kein umfassender Überblick über die verschiedenen Systeme gegeben werden. Ebenso bleibt das Zusammenwachsen von Kommunikations- und Datentechnik, das durch die gewaltigen Fortschritte der Digitaltechnik und -technologie ermöglicht wird, außerhalb der Betrachtung.

2. Anforderungen der Mobilgeräte an die Technologie

Tabelle 1 gibt einen Überblick über die in Europa bekanntesten digitalen Mobilfunksysteme. Zellulare Systeme nach dem GSM-Standard bei 900 und 1800 MHz sowie digitale Schnurlostelefone nach dem DECT-Standard bei 1700 MHz beherrschen heute den Markt. Da durch das rasche Wachstum bereits heute die Grenzen der Übertragungskapazitäten erkennbar werden und angesichts der zunehmenden Mobilität wachsender Bedarf besteht, mit dem gleichen Endgerät weltweit telefonieren zu können, wurde der weltweit gültige UMTS-Standard entwickelt, der etwa ab dem Jahr 2002 verfügbar sein wird. Dieser stellt sowohl eine Erweiterung der bestehenden Systeme als auch langfristig deren Ablösung dar. Er vereinigt nicht nur GSM und DECT, sondern integriert auch spezielle Systeme wie Funkruf, Bündelfunk oder Datenfunk.

Von vielfältiger Bedeutung sind die ISM-Frequenzbänder (Tab. 2). Besonderheit dieser Bänder ist, daß die Anwendungen weitgehend frei sind, d.h. ohne Anmeldung und ohne Kontrolle genutzt werden können. Gegenseitige Störungen sind daher freilich nicht ausgeschlossen. Um diese hinreichend klein zu halten, ist die Sendeleistung auf Werte von 1 – 10 mW (max. 100 mW) begrenzt. Damit lassen sich die Sender zusammen mit dem HF-Teil in einem Baustein integrieren, auch Einchip-Lösungen unter Einschluß des

Logikteils sind denkbar. Anwendungen von großem künftigen Marktpotential sind z.B. RKE (Funkautoschlüssel), ESL (elektronische Warenauszeichnung) oder Bluetooth (in Entwicklung befindlicher Standard für drahtlose Verbindung von PC mit Peripheriegeräten).

Name	**Explanation**	**Frequency Range [MHz]**	**Application**
GSM	Global System for Mobile Communication	900	Cellular
DCS	Digital Cellular System	1800 / 1900	Cellular
DECT	Digital Enhanced Cordless System	1700	Cordless
UMTS	Universal Mobile Telecommunication System	1900 - 2200	Universal Mobile Radio
GPS	Global Positioning System	1500	Positioning
ISM	Industrial, Scientific, Medical	see Table 2	

Tab. 1: Digitale Mobilfunk-Systeme.

Frequency [MHz]	**Typical Applications**
433 (Europe)	Headphones Remote control RKE (Remote keyless entry) Toys
866 / 900 (Europe / USA)	Remote control RKE (Remote keyless entry) ESL (electronic shelf label)
2400 (worldwide)	WLAN (Wireless LAN) Bluetooth LPS (Local positioning system) Microwave oven
5700 (worldwide)	t.b.d.

Tab. 2**:** ISM-Frequenzbänder und Anwendungen.

Abbildung 1 zeigt das Blockschaltbild der Elektronik eines Handy. Die Basisbandfunktionen sind in CMOS-Technik realisiert, die IC's des HF-Teils dagegen in Bipolar-Technik, zusätzlich einige Funktionen wie z.B. der Sendeverstärker in GaAs, außerdem eine Vielzahl diskreter Elemente wie Filter, Spulen, Widerstände und Kondensatoren (von den ca. 300 Bauelementen, aus denen der HF-Teil besteht, sind über 80% diskrete Elemente). Von Anfang an richteten sich alle Anstrengungen darauf, die Geräte kleiner, leichter, billiger zu machen und die Betriebsdauer mit einer Akkuladung zu erhöhen.

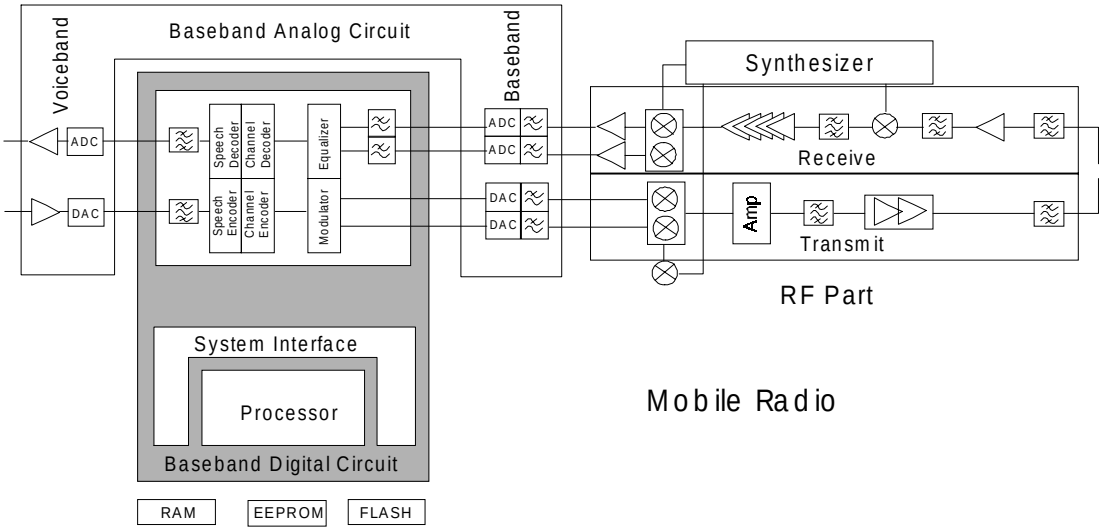

Abb. 1: Blockschaltbild der Elektronik eines GSM-Handys.

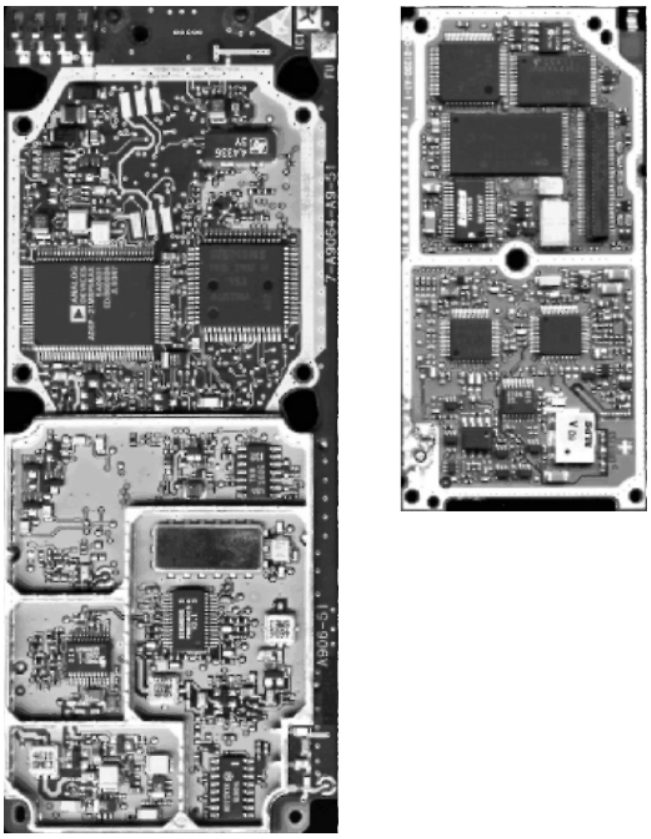

Abb. 2: Schaltungsplatinen von GSM-Handys 1994 und 1998.

Das (vorläufige) Ergebnis ist in Abb. 2 zu sehen, das die Platine eines Gerätes von 1994 und von 1998 in gleichem Maßstab zeigt. Unten ist jeweils der HF-Teil, oben der Basisbandteil zu sehen. Deutlich sind die Maßnahmen zu erkennen, auf denen diese Fortschritte beruhen:

- Höhere Integration, dadurch Verminderung der Zahl der IC's und der diskreten Elemente;
- Verbesserung der Schaltungstechnik, die Verzicht auf Abschirmung ermöglicht;
- Verkleinerung der Gehäuse;
- Miniaturisierung der diskreten Bauelemente, insbesondere der Filter;
- Ferner – auf dem Bild nicht sichtbar – Verringerung der Versorgungsspannungen.

Welche Verbesserungen bei den Halbleitertechnologien notwendig waren, um das zu erreichen, und in wohin die Entwicklung geht, wird im nächsten Abschnitt behandelt.

In der Schaltungstechnik wurden die verschiedene Konzepte erprobt, um den Aufwand zu verringern und zugleich bessere Performance zu erhalten (die Entwicklung der Digitaltechnik soll hier nicht betrachtet werden):

- Zero-IF- (Homodyn-) Technik (Einsparung des SAW-Filters);
- Wahl höherer Zwischenfrequenzen, um Anforderung an die Güte (und damit Größe) der Filter zu verringern;
- Direkte A/D-Wandlung von der Zwischenfrequenz und digitale Weiterverarbeitung (bis heute noch nicht einsetzbar);
- Analog dazu wurden auf der Sendeseite verschiedene Modulationsverfahren entwikkelt (Vor- und Nachteile dieser Verfahren sind in [1] genau dargestellt);
- Höherintegration wie z.B.:
  - Einbau des Low-Noise Amplifiers (LNA) in den Empfängerbaustein;
  - Integrierte Synthesizer-IC's für mehrere Frequenzen;
  - Integration von Teilen der Steuerlogik in die HF-IC's;
  - erste Lösungen für voll integrierte Leistungsverstärker (PA).

Auch in Zukunft geht der Trend in Richtung auf höhere Integration. Dabei geht es vor allem um die Verminderung der Anzahl an Bauteilen, besonders der diskreten. Noch in diesem Jahr wird das erste Gerät mit einem 1-Chip-Transceiver, der Sende- und Empfangspfad und den Synthesizer auf einem Silizium vereint und in einem High-Performance-BICMOS-Prozeß hergestellt wird, auf den Markt kommen.

Weitere Entwicklungsansätze sind:

- Integration von HF- und Basebandfunktionen auf einem Chip;
- Alternativ dazu die Verbindung von Analog- und Digitalfunktionen auf einem einzigen CMOS-Baustein;
- Zusammenfassung von Digitalfunktionen und Speichern;
- Insbesondere für Anwendungen mit geringeren Anforderungen (vor allem in den ISM-Bändern) werden bereits komplette 1-Chip-Lösungen diskutiert.

3. Entwicklungstrends der Siliziumtechnologie

Ohne erhebliche Fortschritte in der Halbleitertechnologie wären die Fortschritte der Gerätetechnik nicht möglich gewesen. Da der Fokus dieses Beitrags besonders auf die

Erhöhung des Integrationsgrades gerichtet ist, beschränke ich mich auf die Entwicklung der Siliziumtechnologie, ohne die Entwicklung der GaAs-Technologie abwerten zu wollen.

Neben der Weiterentwicklung der CMOS-Standardtechnologien für Digitalanwendungen, deren Schwerpunkt Verkleinerung der Strukturen und – dadurch erzwungen und zugleich ermöglicht – der Betriebsspannung war und ist, mußten die Analogtechnologien (Bipolar und CMOS) andersgeartete Forderungen erfüllen:

- Verbesserung der HF- (Grenzfrequenz, Rauschen) und Analogeigenschaften (Toleranzen, Matching, Langzeitstabilität) der Transistoren;
- Bereitstellung passiver Bauelemente hinreichender Güte (Toleranz, Matching, Parameterkonstanz):
  - Widerstände,
  - Kondensatoren,
  - Varaktoren (zur Integration von VCO's),
  - und integrierte Spulen für Anpaßschaltungen, Filter und VCO's.
- Verbindung von digitaler Steuerlogik mit Analogfunktionen (BICMOS-Technologie).

Insbesondere die Integration von Spulen auf Silizium stellt eine große Herausforderung dar, und weltweit werden erhebliche Anstrengungen unternommen, von den derzeit erreichten Gütefaktoren von ca. 5 – 8 auf Werte von mindestens 15 – 20 zu kommen, die notwendig sind, um Filter und Oszillatoren zu realisieren, die diskrete Elemente ersetzen können. Um die im Vergleich zu den optimierten diskreten weiterhin schlechteren Eigenschaften integrierter passiver Bauelemente kompensieren zu können, werden auch für vergleichsweise niedrige Betriebsfrequenzen um 2 GHz SiGe-Transistoren mit Grenzfrequenzen von 50 – 80 GHz entwickelt.

Ein besonders interessanter Aspekt der Entwicklung der nächsten Jahre ist die Frage, wieweit CMOS-Transistoren die bislang dominierenden Bipolartransistoren in HF-Anwendungen ablösen können. Die bisher vorliegenden Ergebnisse scheinen recht vielversprechend, wenn es auch bisher noch keine Produkte gibt, die in höheren Stückzahlen gefertigt werden.

Die Beantwortung der Frage, wieweit die Integration von high-performance Digitalfunktionen (Prozessor, DSP) mit anspruchsvollen Analogfunktionen (DAC/ADC, HF) sinnvoll möglich ist, ist heute noch nicht möglich. Einige grundsätzliche Aspekte lassen jedoch die wahrscheinliche Richtung ahnen:

- Die Anforderungen von Seiten der Digital- und der Analogtechnik sind unterschiedlich (siehe Tab.3): während die Digitaltechnik fast ausschließlich auf höhere Geschwindigkeit und höhere Packungsdichte hin optimiert wird, liegt in der Analogtechnik das Hauptgewicht auf Eigenschaften wie Parameterstabilität, Linearität und Verstärkung, Eigenschaften, die sich kaum mit minimalen Strukturen und kleinsten Versorgungsspannungen realisieren lassen.
- Die Innovationsgeschwindigkeiten sind wesentlich verschieden. Während die Digitaltechnik einem Zyklus von 1 – 2 Jahren folgt (der von einer weitgehend automatisierten, hochsprachenbasierten Designtechnik unterstützt wird), ist eine hoch komplexe Analogschaltung auf absehbare Zeit nicht ohne Redesign realisierbar.

Functional Block		Feature	Aim
Digital Part	Controller	Shrinking dimensions, increasing clock rates, decreasing supply voltage	Low power, increasing complexity, less space
	DSP		
	Memory		
Analog Part	RF	Higher frequencies, high linearity and gain, low noise, high-quality passive devices	Higher integration level, better performance @ lower power, new applications
	ADC/DAC		
	Filter		
	Amplifier		

Tab. 3: Anforderungen digitaler und analoger Funktionen.

Daher ist zu erwarten, daß für Anwendungen mit den höchsten Anforderungen an die Systemperformance wie z.B. GSM die Entwicklung eher in Richtung auf Zusammenfassung aller digitalen und aller analogen Funktionen in jeweils einem eigenen Chip hin gehen wird. Dabei dürfte der Analogteil zunehmend auf einem Silizium integriert werden, wobei die Entwicklung hier von high-performance BICMOS-Technologien mittelfristig hin zu low-cost BICMOS (d.h. Einbau eines Bipolartransistors mittlerer HF-Performance mit möglichst wenig zusätzlichen Fototechnikschritten in einen Analog-CMOS-Prozeß) gehen wird.

Für Anwendungen, die nur geringe Anforderungen an die Performance der Funktionsgruppen stellen und auch nicht die jeweils schnellste Digitaltechnologie erfordern (z.B. Funkverbindungen mit kurzer Reichweite und geringer Datenrate) dürfte eine reine CMOS-Lösung, die auf einem Chip integriert werden kann, ebenso attraktiv wie aussichtsreich sein.

Darüber hinaus gibt es aber weiterhin wachsenden Bedarf an neuen Funkanwendungen, für den weitere, d.h. höhere Frequenzbänder benötigt werden. Beispiel dafür ist das 5,7 GHz ISM-Band, das bereits definiert, aber praktisch noch nicht in Verwendung ist. Die Einführung neuer Frequenzbänder hängt dabei von der Verfügbarkeit sowohl leistungsfähiger als auch kostengünstiger Halbleitertechnologien ab. Daher wird es auch in Zukunft Bedarf an Höchstfrequenztechnologien geben, sei es nun GaAs als die Frontendtechnologie oder high-performance Bipolar/BICMOS als Voraussetzung für kostengünstige Standardanwendung.

4. Zusammenfassung

Für die bekanntesten digitalen Funksysteme werden die Entwicklungstrends und die sich daraus für die Siliziumtechnologien ergebenden Anforderungen vorgestellt. Es wird gezeigt, daß weitere Fortschritte in der Gerätetechnik von der weiteren Verbesserung der aktiven und v.a. der passiven Bauelemente in den Analogtechnologien abhängen. Ferner wird dargestellt, daß die CMOS-Technologie auch im HF-Frontend zunehmende Anwendung finden wird, daß darüber hinaus auch künftig Bedarf an leistungsfähigen Bipolar- und BICMOS-Prozessen bestehen wird.

Literatur

[1] J. Fenk: *Highly integrated RF-IC's for GSM and DECT Systems – A Status Review*; IEEE Trans. on Microwave Theory and Techniques, Vol. 45, No. 12, 1997

High Speed Data Converters and New Telecommunication Needs

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Recent technology improvements are leading to significant advances in telecommunications. New sub-micron technologies allow us to design high speed digital processors and high-speed, high-resolution data converters. These basic components push the analog-digital border close to the antenna and favor the implementation of complex digital algorithms. Various system architectures are examined and key data converter specifications are established. Then, the design techniques and the linearization methods that make possible the implementation of the required specifications are discussed.

1. Introduction

Many of the applications that are benefiting significantly from progress in microelectronics belong to the communication area. We are enjoying a tremendous growth in mobile communication: new services are being constantly introduced thanks to the availability of high speed data communication. This progress results from two key components: the DSP and the data converter. Using sub-sub-micron technologies it is possible to integrate millions of transistors on a single chip. The speed of digital circuits is increasing up to many hundreds of MHz. Hence, new DSP architectures allow complex algorithms to be implemented at very high computation speeds. However, analog-digital interfaces must be able to match the resolution and the speed of the DSP. Therefore, the second key component completing the basic design set is the high speed and high resolution data converter [1].

The present trend pushing the border of digital conversion towards the transmit and receive terminal leads to ever increasing demands on specifications, namely speed and resolution. We will see that often more than 14 bits and hundred of MHz are necessary. In addition, many applications require continuous reductions in power consumption. As a result, market challenges favor research on high speed data converters. In turn, the results achieved lead to new architectural solutions which create new needs. This paper analyses this process and discusses recent circuit solutions suitable for meeting key system specifications.

2. Communication Systems

We can use three main transmission media for analog communication and for data transfer: wireless, twisted-pair cable and coaxial cable. Optic fibers can also be employed, but their high cost make their use suitable only for backbone networks. For data communication, it is possible to utilize either narrow-band connections (up to 56 kb/s)

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or broadband connections (like the T-1 service operating at 1.544 Mb/s). Around the options of media and bandwidth, communication engineers can build many possible architectures. We shall see that in many of them, data converters have a significant role.

For narrow-band wireless we have different standards around the world. In Europe we have the GSM operating in two different frequency bands: 900 and 1800 MHz (GSM 900 and GSM 1800). In the USA we have various mobile radio standards in the 1800 MHz frequency band. The most popular are the PSC 1900, D-AMPS and QUALCOMM CMDA. In Japan the standard used is PDC but another one, the IS-95, is about to be installed. The present scenario is such that, despite the considerable effort spent on standardization, it will be hard to establish a unique worldwide standard for future mobile radio systems. Consequently, managing multiple standards will be ever more necessary creating difficulties to both manufacturers and operators.

Significant help can come from the so-called "software radio" approach [2]. Figure 1 shows the "ideal" software radio solution: a high speed data converter digitizes the RF signal directly at the antenna with all radio functions being performed in the digital domain possibly using a specialized reconfigurable hardware. At present, because of the obvious difficulties in the implementation of the "ideal" solution, the data converter is moved after some analog pre-processing. This is done typically after the low noise amplifier and a first mixing (Fig. 2, showing the Rx section).

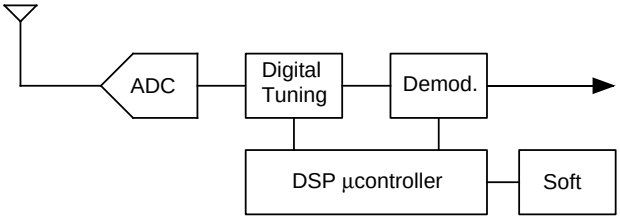

Fig. 1: Ideal software radio.

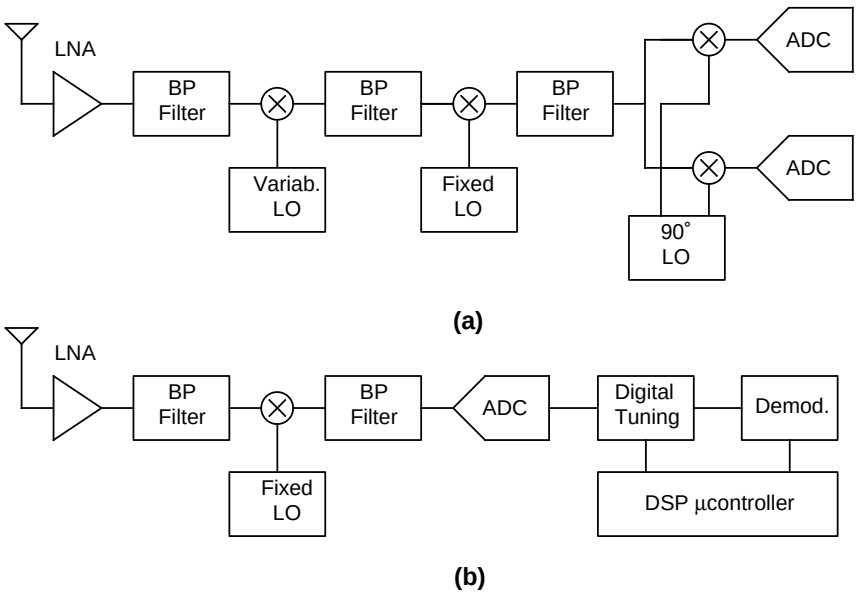

Fig. 2: (a) Conventional architecture of a receive radio; (b) software radio improvement.

More generally, software radio envisages a base station platform with reconfigurable hardware and software. This architecture can be adapted to different standards or services simply by using the appropriate software. Software radio offers many advantages: it is flexible, allows new services to be added quickly thus shortening the time-to-market, offers better management of logistics, maintenance and personnel training. Moreover, software radio permits migration from one standard to the successive generation along an evolutionary path.

About data converters observe that, since channel tuning is performed in the digital domain, the linearity of the converter must be such as to avoid any spurious interference. Fortunately the bandwidth licensed to operators is limited, typically under 10 – 15 MHz. Therefore, appropriate choice of the LO frequency and the sampling frequency of data converters allows some system flexibility that can place images and spurious signals out of band. Thus, data converter specifications depend on the architecture and standard adopted. For modern architectures they span from 12 to 16 bit with spurious performances around 100 dB. The sampling frequency ranges from 60 to 80 MHz.

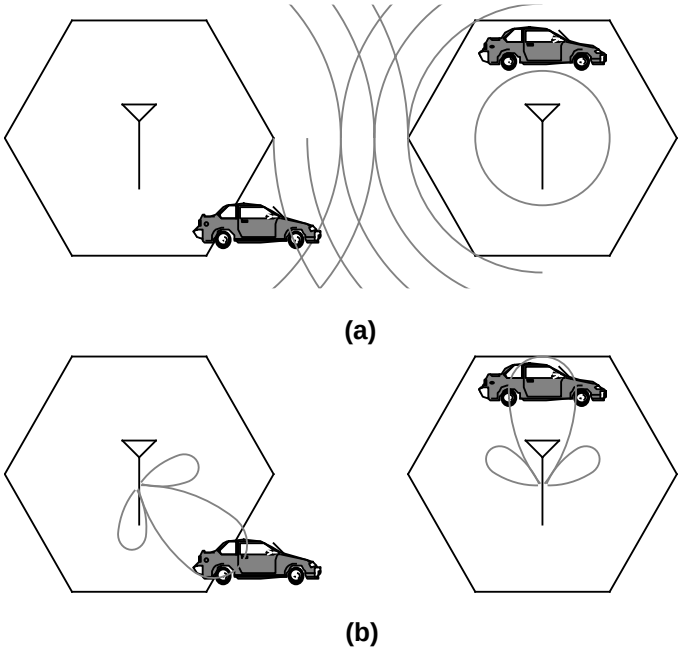

Fig. 3: (a) Omnidirectional antenna; (b) smart antenna.

In cellular communication, important features are coverage, capacity, and service quality. In rural areas ensuring a proper coverage is expensive, in urban areas the capacity is often close to average demand. Moreover, interference from neighbor cells worsens service quality. Smart antennas provide an answer to these problems [3], [4]. A smart antenna is a directional antenna used in the base station to track mobile terminals (Fig. 3). The basic structure uses a switched-beam or an adaptive array architecture. Two or more antenna elements are spatially arranged and the signals are properly processed to produce a directional radiation pattern.

In its simplest form, a smart antenna uses a fixed phase beam network that is switched to the elements of the array so as to produce a beam closer to the desired direction. In the phased array the phases of signals are adjusted to change the array pattern, thus tracking a given mobile or canceling a given interference signal.

Here, different strategies for rural or urban areas are necessary. Therefore, adaptive and reconfigurable architectures are the best solution. Figure 4 shows the block diagram of a possible "digital" implementation. The architecture uses a weight-adjustment algorithm to obtain IF beam-forming. Of course the given architecture is only one possibility, we could design a solution fully in the analog domain. Nevertheless, the digital approach, thanks to the use of the data converter in the IF section, permits complex beam-forming with a digital processor. Therefore, the availability of data converters which answer system requirements leads us to an adaptive system providing superior performance.

The data converter specifications depend on the IF frequency used. Even for these applications the resolution depends on the width of the bandwidth granted to a given provider. In the case of 10 MHz we can satisfy the GSM specifications (receive side) with an 81 dB dynamic range (13.5 bit) and a 97 dB SFDR. Moreover, the clock jitter must be kept below 2 ps. The above figures assume an IF frequency of 70 MHz. More relaxed figures result when considering other standards like the DCS 1800.

Broadband communication offers many examples of architectures that exploit data converters and DSP. Through the already installed copper twisted-pair phone lines it is possible to provide broadband digital services. We have various possibilities, the ADSL (Asymmetric Digital Subscriber Line), HDSL (High speed), the RADSL (Rate Adaptive) and the VDSL (Very high speed). The first class runs at a data rate of up to 8 Mb/s in the downstream direction (from the central office to the subscriber) and up to 1 Mb/s in the upstream direction. The distance from the central office to the subscriber, however, must be a maximum of 5 km. The VDSL service is more advanced, it can provide a data rate as high as 52 Mb/s. The architecture provides a fiber optical connection from the central office to the neighborhood of a group of customers (Optical network Unit, ONU). The connection from the ONU to the subscriber is through a short link (not more than 1200 m) of twisted-pair copper wire [5].

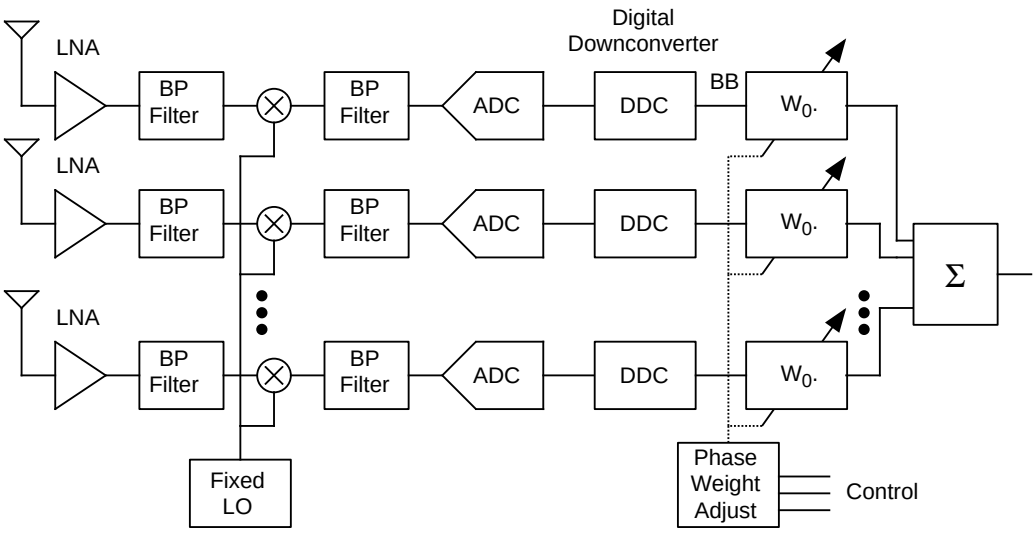

Fig. 4: Architecture of a digital smart antenna.

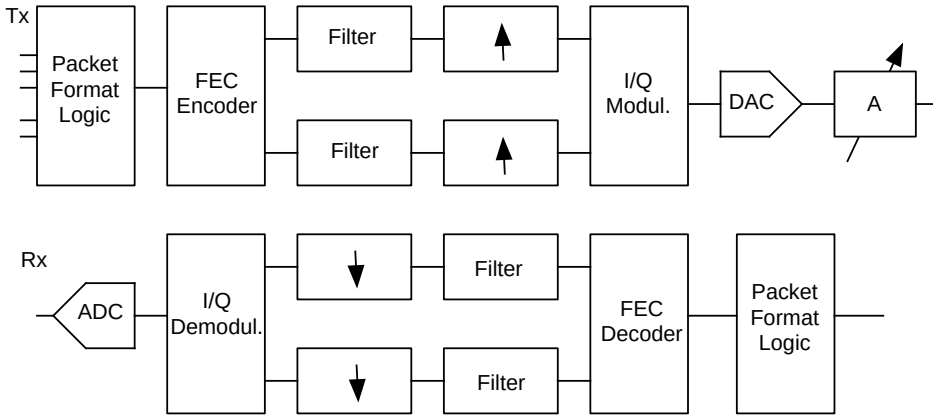

Fig. 5: Architecture of a VDSL transceiver.

The above features are made possible by complex modulation schemes and the relatively high bandwidth of twisted-pair wires (much higher than the 3 kHz filtered voiced channel). An example of VDSL architecture is shown in Fig. 5 [6]. Note that it includes an A/D and a D/A converter very close to the twisted-pair connection. For the ADSL architecture the sampling rate in the two links is 8 – 10 MHz and the required resolution is 12 – 14 bits. For VSDL architectures the resolution required is a bit lower but the sampling rate must be programmable from 1 MHz to 52 MHz.

3. High Speed Data Converters

High speed of operation can be achieved with advanced modern technologies. Submicron CMOS and advanced BiCMOS or SiGe permit bandwidths in the order of many GHz. Therefore, speed is an issue that can be satisfactorily addressed by exploiting the available technology. In contrast, accuracy depends on the components' precision and on practical limits related to circuit implementation. Therefore, the processes used, as well as deep-submicron line widths, should also provide precise resistors and capacitors. Moreover, the analog critical nodes must be conveniently protected from spur signals and noise. This demand imposes additional steps on the process: it is necessary to utilize, for example, multiple diffused wells, trench separation, or migrate toward SOI technologies. All these actions are only beneficial, however, when more than 10 – 12 bits are required. For higher resolution the best way to get rid of inaccuracy is to use calibration.

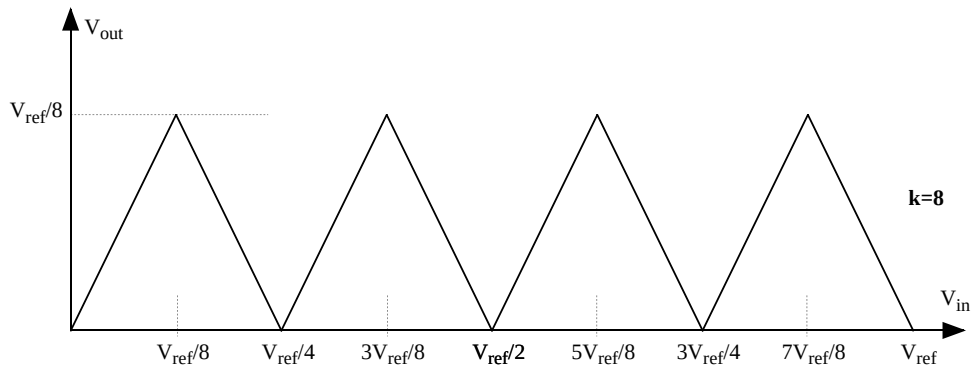

Fig. 6: Folding transfer characteristics.

The simplest manner to achieve high speed is to use one step or two step flash architectures. The flash technique has been used extensively in the past; however, various limitations do not allow us to step outside the 10 bit limit [7]. Another approach is the folding and interpolation technique. Folding consists in nonlinear input processing that produces an output characteristic like the one shown in Fig. 6. The number of foldings performed determines the MSBs (3 bits for the figure). Subsequent data conversion determines additional LSBs. Folding is often associated with interpolation: a suitable network processes two folded outputs and produces transition levels intermediate to the one given by the folding transformation. We can thus extract additional bits at a reduced cost. An example of folding and interpolation architecture is given in [8]. The circuit achieves 10 bits and 40 MS/s using a 7 GHz 0.6 µm CMOS technology.

As mentioned above, it is necessary to use calibration when pursuing more than 10 – 12 bits of accuracy. Various calibration algorithms have been proposed. Some of them correct possible mismatches in the analog domain. For example, if two capacitors must be equal, the difference due to technological mismatch can be adjusted with a binary programmable capacitor array. Other methods measure the analog mismatch and store the information in memory to digitally correct the result achieved afterwards. All these techniques require a calibration/correction cycle, often performed at power-on. Alternatively, it is possible to use a queue-based architecture able to generate time-slots which allocate the calibration cycle without disturbing the conversion operation [9].

Designers widely use pipeline architectures for communication needs: the pipeline solution properly suits speed requirements and digital calibration demands. Fig. 7 shows a typical pipeline scheme. A number of equal cells compose the structure. Each cell provides a given number of bits at the output (say, N) and residual error. The next cell processes the residual error, performs digital conversion and gives another residual error. The output of the DAC is the combination of the bits from each stage of the pipeline. Since the dynamic range of the residual error is smaller than the input by a factor 2^N, many architectures foresee an amplification of the residual error by the same factor to keep the dynamic range constant along the pipeline. Possible errors are normally corrected digitally. Each stage of the pipeline provides the digital information with some redundancy (for a 1 bit per stage architecture, a 0.5 additional bit). Redundancy avoids loss of information even in the presence of error and permits to fully cancel inaccuracies.

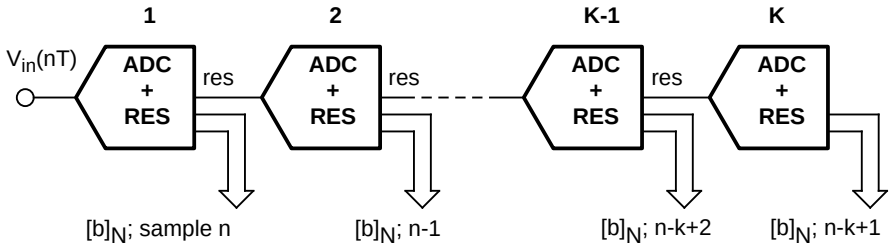

Fig. 7: Pipeline architecture.

Alternative digital calibration methods are proposed in [10] (Fig. 8).Transcoding RAMs useful in correcting converter non-linearities are used. This solution is common to many digital calibration methods. The point is how to generate the transcoding curve. Two methods are proposed. The first one is for off-line correction and the second one acts concurrently with the normal converter operation (on-line).

We can observe that the transcoding operation is not only useful to correct non-linearities, but we can also achieve a precise representation of the transitions between the quantization channels. For this reason the ROM must have more bits than the address does. Hence, thanks to careful correction of the integral non-linearity, we can significantly improve the SFDR. The first scheme in Fig. 8 requires a training-calibration cycle, possibly replacing testing after fabrication. A sine-wave enters the data converter and the output histogram allows the transfer characteristic to be extracted. To this end, the same technique proposed for testing data converters dynamically is used [11].

The second scheme employs an auxiliary conversion channel. It runs at a lower frequency than the main channel. The lower clock rate ensures higher accuracy, thus providing the calibration term necessary for updating the transcoding memory. The algorithm used ensures accuracy and a suitable management of the two multiplexed RAM. Moreover, it is necessary to use a high speed high accuracy track and hold at the input of the system. Observe that the performance of this block limits the performance of the entire system. However, it is possible to achieve excellent linearity (up to 14 – 15 bits) while using clock frequencies up to 100 MHz [12].

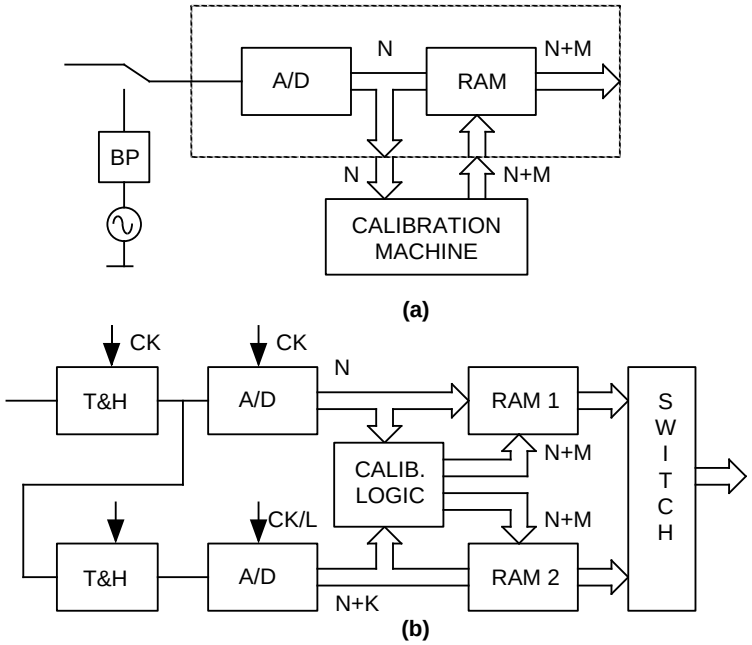

Fig. 8: (a) Off-line and (b) on-line digital calibration.

4. Conclusions

We have seen that the tremendous pace in telecommunication developments affects (and is produced by) improvements in data converter performance. We have a combination of technological advances and novel architectures. Typically, benefits come from an extensive use of digital correction and calibration. Therefore, we can talk about a new approach for achieving high performance: using “digitally assisted” data converters.

The market already offers data converters running at 100 Mb/s with 14 bit resolutions and a SFDR of 100 dB. The technology used is, in some cases, complex. Nevertheless,

progress in CMOS processes will soon make available 0.18 µm technologies with migration to the 0.15 µm mark by the year 2000. It is expected that 0.09 µm effective channel length will be achieved by 2001 and 0.07 µm by 2004. If these features are combined with a suitable defense from spur interference 18-bit, 200 Mb/s data converters capable of answering a wide spectrum of telecommunication needs will be on the market by the first decade of the next century.

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Sicherheitsrelevante Systeme in der Flugsicherung

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Die Firma FREQUENTIS beschäftigt sich insbesondere mit Sprachvermittlungssystemen für die Flugsicherung. Das Wort *Flugsicherung* schließt bereits das Wort *Sicherheit* ein. Es geht hier insbesondere um Ausfallssicherheit. Unter diesem Blickwinkel ist der nachfolgende Beitrag zu sehen.

1. Einleitung

Das Thema Flugsicherung schließt die Kontrolle des zivilen und militärischen Luftraums ein. Es geht dabei um Systeme für die Überwachung und Lenkung des Flugverkehrs. Neben den Radarsystemen und der Radardatenverarbeitung, Flugplandaten, Instrumenten-, etc. Landesystemen steht die Sprachvermittlung an oberster Stelle. Die Sprachvermittlung ist deshalb von so hoher Bedeutung, da es derzeit letztlich das einzige Kommunikationsmittel ist, das international und flächendeckend verfügbar ist, um zwischen dem Boden und dem Flugzeug zu kommunizieren. Ohne Anweisungen über Funk helfen auch die besten anderen Managementsysteme dem Lotsen nichts, wenn er keine Anweisungen an die Piloten geben kann.

2. Welche Sprachvermittlungssysteme sind nun nötig?

Zum einen Teil handelt es sich um Ground/Ground Systeme, die zur Kommunikation der Fluglotsen im Zentrum untereinander beziehungsweise zwischen den einzelnen Kontrollzentralen und den Towereinrichtungen auf den Flugplätzen dienen.

Neben diesen Ground/Ground Verbindungen ist aber insbesondere dem Air/Ground System hohe Bedeutung beigemessen. Es geht hier um spezielle Funkvermittlungssysteme, die die Sprachvermittlung zwischen den Fluglotsen und den Piloten bzw. zwischen Luftfahrzeugen, die unterschiedliche Frequenzen benutzen, herstellen. Eng verbunden mit diesen Air/Ground Kommunikationssystemen, sind auch Remote Control Systeme, die die landesweite Nutzung von Sende/Empfangsanlagen durch eine zentrale Flugverkehrskontrollzentrale ermöglichen.

3. Systemarchitekturen

Die Systemarchitekturen sind von der hohen Anforderung an die Systemverfügbarkeit geprägt. In den meisten Fällen handelt es sich dabei um nachrichtentechnische Systeme, die auf einer sternförmigen Struktur, einer busartigen Verbindung oder auf Ringstrukturen fußen. Hier werden die verschiedenen Systeme auf ihre Vor- und Nachteile untersucht und verglichen.

4. Safety

Der Begriff Safety wird vor allem im angloamerikanischen Raum bereits stark für all jene Untersuchungen und Betrachtungen verwendet, die sich mit Ausfallssicherheit beschäftigen. Umfangreiche Studien im Rahmen des Designs der Systeme und danach tragen dazu bei, daß die zu entwickelnden Systeme von vornherein darauf ausgelegt sind, möglichst wenig Wirkung bei Teilausfällen zu verzeichnen.

Es geht hier um die Betrachtung, was passiert, wenn etwas passiert. Also insbesondere um die Störwirkwerte und das Ausfallsverhalten von Teilkomponenten. Hier sind Analogien zu den verschiedenen Betrachtungen im Bereich der Automobilindustrie durchaus vergleichbar.

5. Zusammenfassung

Systeme in der Flugsicherung haben heute bereits einen hohen Verfügbarkeitsgrad. Hier geht es aber meistens um einzelne Systeme. Einzelne Systeme für die Sprachvermittlung und für die Datenverarbeitung. Diese Systeme sind strikt voneinander getrennt und werden auch von verschiedenen Herstellern erzeugt und von der Flugsicherungsbehörde dann normalerweise integriert.

Es besteht jedoch die klare Tendenz auch hier zu einer Sprachdatenintegration. Das soll vor allem Kosten bei Leitungsmieten aber auch bei der Wartung und Maintenance einsparen helfen. Hand in Hand geht da natürlich die Überlegung, was passiert mit der Ausfallssicherheit dieser Systeme. Das heißt, in Zukunft werden noch höher verfügbare Systeme mit Sprachdatenintegration auf Netzwerkbasis die Flugsicherung dominieren. Im Sinne eines Netzwerks können dann sicher einzelne Komponenten ausfallen, ohne daß das Gesamtsystem wirklich beeinträchtigt wird.

A Survey of ASIC Design Centers at Austrian Universities

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Throughout the last years several groups at Austrian universities succeeded in establishing state-of-the-art ASIC design centers with the aid of regional, national, and European funding. These centers were by no means targeted to facilitate research and education activities alone. The direct support of Austrian enterprises – mainly but not exclusively small and medium sized companies – has been of equal importance to all groups. For the sake of clarification a brief historic summary will start this survey. Subsequently all partners at the Vienna University of Technology, at the Graz University of Technology, and at the Linz University will be introduced. After briefly describing the respective infrastructure, we will cover the areas of interest and special competencies of every center. Finally the results of selected projects will be presented.

1. Introduction

The ASIC design activities at Austrian universities started more than 15 years ago. Traditionally those university institutes engaged in this subject were not focused entirely on research and education alone but intended to address directly the needs of Austrian electronic industry. To accomplish this goal, ASIC design centers had to be established and maintained on a regular basis at every site. Besides the necessary hard- and software for designing integrated circuits specialized measurement equipment for verifying prototype ICs had to be at hand for every design center from the very beginning. Evidently, funding of such activities generally is far beyond the financial capabilities of a single University institute. As a consequence, a series of regional and later national projects were launched in order to facilitate the set-up and operation of ASIC design centers.

Efficiently funded by the GMe, the UNICHIP project was the first initiative of this kind with the Institute of Electronics at the Technical University of Graz and the Institute of General Electrical Engineering and Electronics at the Vienna University of Technology taking part. At that time access to both state-of-the-art design software and prototype fabrication facilities were tremendously expensive even if special discount rates for universities were taken into account. For the same reasons direct cooperation with industrial partners were somehow limited to those firms with previous knowledge on ASIC design. Our main target group – SMEs with little experience in computer aided design methods of integrated circuits and electronic systems – was very difficult to address. An ASIC design was linked to high investments which were considered too risky to undertake. Additionally, all those applications requiring only small and medium production quantities had to be ruled out anyway.

Luckily enough, things changed dramatically as soon as the European Commission launched an initiative to tackle the aforementioned problems on a European scale. Participating in the ESPRIT project EUROCHIP and later in the EUROPRACTICE project enabled universities all over Europe to establish advanced ASIC design facilities for research, education, and direct support of SMEs. Today EUROPRACTICE offers several basic services for Universities: State-of-the-art IC design software may be licensed with affordable annual fees. Secondly, prototype fabrication of integrated circuits based on multi project wafer runs has been setup in cooperation with European IC foundries. For new technologies such as multi chip modules (MCMs) and microsystems a similar approach has been chosen to cut down fabrication costs. Finally, the TBPS (Training and Best Practice Service), a European approach to co-ordinate training and continuous education in the area of microelectronics, concludes the EUROPRACTICE services[1].

Except for the software support service all services of EUROPRACTICE are open for industry as well. Key to the tremendous success of EURORPACTICE was the extension of the prototyping program to small and medium production quantities of fully tested and qualified ASICs, MCMs, and microsystems. Together with an ASIC design center, SMEs are now able to launch to develop their own ASICs for a variety of applications.

As in most of the other EC member states, national programs were launched to fund the participation in EUROPRACTICE for universities dealing with ASIC design. In Austria the AUSTROCHIP project and later the TMOe initiative was proposed.

2. TMOe

The “Technologieverbund Mikroelektronik Österreich” is a loose union of now six university institutes with the goal to intensify the use of microelectronics within Austrian industry. Needless to mention that the participants are putting special emphasis on addressing SMEs. In the following paragraphs all members of the TMOe will be introduced together with their special field of interest in research and education. The TMOe members are in alphabetical order:

- Institute for Applied Electronics and Quantum Electronics,
  situated at the Vienna University of Technology
  http://www.iaee.tuwien.ac.at/agcad
- Carinthian Tech Institute
  http://cti.ac.at
- Institute for Computer Science, situated at the Vienna University of Technology
  http://www.ict.tuwien.ac.at
- Institute for Electronics, situated at the Technical University of Graz
  http://www-ife.tu-graz.ac.at

[1] Although this program is generously funded by the EC, the author has serious doubts about its success. A huge database of courses on nearly any subject in microelectronics offered in Europe has been built up, however, no information on the quality of a specific course has been collected. For engineers in industry seeking education possibilities in microelectronics, the TBPS service is quite useless without inside knowledge of the actual qualification of a course provider. On the other hand, university institutes usually know the relevant experts anyhow and use the TBPS database just as an on-line schedule for ASIC design courses. Hopefully, the role of TBPS will be re-investigated within the 5th framework program (IST)

- Research Institute for Integrated Circuits, situated at the Linz University
  http://www.riic.ac.at
- Institute for Applied Information Processing and Communications,
  situated at the Technical University of Graz
  http://www.iaik.tu-graz.ac.at

2.1 Institute of Applied Electronics and Quantum Electronics

The main areas of interest of the CAD working group are digital and analogue CMOS ASIC design, complex FPGAs and EPLDs, and design of electronic systems. In the recent past the group gained detailed experience in developing ASSPs – application specific digital signal processors. A total of four University lectures are given every year covering the computer aided design of integrated circuits, of field programmable integrated circuits, of printed circuit boards, and finally the test of integrated circuits. Apart from these lectures continuous education by means of specially tailored training courses is offered to SMEs upon special request.

Industrial support and know-how transfer in the area of microelectronics is by far not limited to training courses alone. Typically, an SME seeks assistance on a specific topic such as evaluation of EDA tools or asks for an analysis on whether it is both technically and commercially justifiable to introduce ASICs into a product. As a result of such a feasibility study a design project is defined and in some cases jointly worked on.

During the last few years more than 30 firms took advantage of the service offers of the group, 28 design projects were completed in close cooperation with eight partner enterprises.

2.2 Carinthian Tech Institute (CTI)

Recently the Carinthian Tech Institute became a member of the TMOe. It replaces the Institute für Technische Informatik at the Vienna University of Technology, because Prof. Herbert Grünbacher, former full professor at the institute, shifted his professional interest and is now in charge of coordinating electronic and microelectronic research and education at the CTI. Prof. Grünbacher's work is dedicated to high level system and ASIC design with special emphasis in VHDL based design capture and synthesis. Within the scope of an ESPRIT cooperation (TTA – Time Triggered Architecture), a microcontroller for distributed fault tolerant systems has been developed. The promising results obtained so far will lead to interesting ASIC design activities at the CTI.

2.3 Institute for Computer Science

Methodologies of high level digital circuit design with special emphasis on ICs is one of the main responsibilities of the institute within the computer science curriculum at the faculty of electrical engineering. Several lectures held in combination with hands-on courses are dealing with this subject. Closely linked to the ASIC design work the institute focuses on communication systems paying special attention on field bus systems. Direct support of Austrian SMEs was successfully established in the latter subject by means of special field bus courses. Together with Motorola a hardware accelerator ASIC (LDC, Lower Layer Driver Chip) for the LON field bus has been developed.

2.4 Institute for Applied Information Processing and Communications

Over the past years, this institute has gained advanced knowledge in the area of computer networks and operating systems with special emphasis on data security issues. Custom made complex digital VLSI chips are indispensable for designing reliable and fast data encryption systems. Furthermore, the Institute has successfully supported both private and public organizations in solving data security problems. Naturally, digital VLSI design is a substantial part of undergraduate education the institute is responsible of.

2.5 Institute for Electronics

Originally, research was focused on designing high accuracy sensors for measuring physical quantities like temperature or density of fluids. As a consequence, the opportunities that analogue, digital, and mixed mode ASICs are offering to tackle these problems have been investigated for several years. Thus, the institute has acquired advanced know-how in all areas of CMOS ASIC design, which are now taught in several undergraduate courses in integrated circuits.

The close vicinity to AMS, an Austrian chip foundry, helped to establish a long term relationship between the institute and AMS. Many diploma theses have been completed in the framework of this cooperation. The actual research work on sensors has led to several successful products which have been developed in cooperation with the Austrian firm Anton Paar KG.

2.6 Research Institute for Integrated Circuits (RIIC)

In 1997, the RIIC has been founded with the intention to concentrate all activities in integrated circuit design in one single institute. One of the duties is of course educating computer science and mechatronics students by offering theoretical lectures on communication science and electrical engineering together with hands-on courses in ASIC design. The institute has targeted its research efforts towards the analogue analysis of SiGe devices. In the area of digital design, the main field of interest is located in automated testing of digital ASICs.

Direct support of Austrian SMEs has been accomplished in several ways. The RIIC is participating as a Technology Transfer Node within the ESPRIT EUROPRACTICE FUSE (First User) initiative. Within the frame of the EUREKA project NESSI the RIIC acts as a Support and Competence Center for Austria. Both of these projects are purely focused on direct support of SMEs in introducing microelectronic technologies. As an accompanying measure post graduate training courses are offered on a series of topics such as VHDL-based design techniques or VIEWLogic® software training courses.

3. Selected Projects

This survey shall be concluded by presenting the results of two typical ASIC design projects. Both are examples for an efficient combination of a successful ASIC development with detailed know-how transfer of computer aided design methodologies.

3.1 HST - Headset Transceiver ASIC

Together with Frequentis Nachrichtentechnik an analogue CMOS ASIC has been developed to be used in data communication systems for air traffic control. The HST comprises two independent transceiver circuits, each of which consists itself of two differential power amplifiers together with a microphone input amplifier. Several amplifiers and switching elements provide analogue loop-back functionality for testing purposes. The HST acts as a front-end circuit and thus allows the direct connection of standard headsets to the system.

As our partners did not intend to launch an analogue ASIC design group for their own needs, the know-how transfer was focused on project related issues such as ASIC specification, project flow, sharing and partitioning of responsibilities between all partners.

The HST has been fully qualified by Frequentis and is an integral part of every new design.

3.2 IVASIC-16

The Austrian firm AKG-Acoustics has developed a new method of virtual acoustics which improves in an impressive way the sound perception when using headphones. By means of complex digital filters, a natural sound impression comparable to normal loudspeakers is achieved. After having proved the principle using a standard DSP, AKG decided to introduce ASICs into the system. Two different ASICs, one for professional applications and the other for consumer products, have been developed in close cooperation with AKG. The latter ASIC has been transferred into volume production with the very successful product HEARO777, a wireless headphone with virtual acoustic features.

Although technology transfer was done in a similar way as described in the previous project, AKG was encouraged to participate actively in the design process itself as well. Interface circuits and part of the verification was performed by design engineers of AKG.

Acknowledgements

The work of all design centers of the TMOe would not have been possible without the intensive support of many regional and national organizations. On behalf of all TMOe members the author wishes to express his thanks to the following organizations:

- GMe – Gesellschaft für Mikroelektronik
- BMwA – Bundesministerium für wirtschaftliche Angelegenheiten
- BMWV – Bundesministerium für Wissenschaft und Verkehr
- Jubiläumsfond der Österreichischen Nationalbank
- Amt der Steiermärkischen Landesregierung
- Amt der Niederösterreichischen Landesregierung
- Amt der Oberösterreichischen Landesregierung
- Stadtgemeinde Wr. Neustadt

MMIC Research and Development at Austrian Universities

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Altenberger Str. 69, 4040 Linz, Austria

1. Introduction

Over the past decades, microwave circuit technology has shifted from the conventional waveguide and coaxial line components and systems to the use of planar circuits, so-called MICs or microwave integrated circuits. In the hybrid form active and passive discrete components (in packaged and chip form) are connected to each other by wire or band bonds which suffer from uncontrolled parasitics yielding low reproducibility. These drawbacks have been eliminated by using monolithic microwave integrated circuits or MMICs, wherein all components are fabricated using deposition and etching processes allowing small size, low weight and low-cost mass production which are indispensable for commercial applications.

MIC engineering was characterized by tuning the circuit by the use of metal and dielectric disks, by adjusting bond wire lengths or by the substitution of one FET for another, all while observing the microwave response on a network analyzer. For MMICs, a complete reappraisal of design and technological methods is necessary. Successful realization of MMICs requires process tolerant circuit design and simulation of overall MMIC behavior.

It is obvious that MMIC design and MMIC fabrication must be coordinated as closely as possible. Since MMIC fabrication is very cost-intensive only a few process technologies have been developed successfully in the past, and they are today available at "foundries". They are either silicon-based or gallium-arsenide-based. For both advanced versions have been developed by introducing heterostructure layers (Si/Ge and AlInGaAs) thereby pushing up the frequency limit into the 100 GHz range and beyond.

A very promising alternative approach to MMIC technology is the Flip-Chip technology allowing the combination of MMIC and hybrid technology.

Due to the very broad spectrum of MMIC development small research groups frequently seek cooperation with partners as it is the case for the two examples described below.

2. MMIC R&D at the Technical University of Vienna

2.1 High-Efficiency Harmonic-Control Amplifier[1]

B. Ingruber, W. Pritzl, D. Smely, M. Wachutka and G. Magerl,
Institute of Electrical Measurements

A two-stage half-sinusoidally driven class-A harmonic-control amplifier (hHCA) has been realized in hybrid MIC technology using GaAs MESFETs which delivers 27,9 dBm output power at 1.62 GHz with 22,4 dB gain and 71% overall efficiency. Third and fifth order intermodulation distortion were –29dBc and –21dBc, respectively [1].

An MMIC version of the two-stage hHCA using AlGaAs HEMT technology is presently developed in cooperation with the Fraunhofer-Institute for Applied Physics, Freiburg, where the fabrication of the MMIC will be carried out.

3. MMIC R&D at Johannes Kepler University, Linz

3.1 CAD center

Richard Hagelauer,
Research Institute for Integrated Circuits

Design of front-end chip-sets and bipolar power amplifiers for cellular applications and for microwave sensing, RF CMOS design, single chip radar module, etc., all in silicon technology (Siemens foundry processes like B6HF and others) [2], [3].

3.2 Clean room

Hartwig Thim,
Microelectronics Institute

Fabrication of simple Ga(In)As MMICs in 0,5µm MESFET technology compatible with standard foundry processes, hybrid MIC (interconnection) technologies, etc. [4], [5]. MMICs with smaller dimensions (< 0,5 µm) have been developed in cooperation with foundries, for example, a 40 GHz frequency divider has been supplied by IAF Freiburg.

3.3 Microwave equipment

Robert Weigel,
Institute for Communications and Information Engineering

Network Analyzer + Wafer Prober up to 75GHz, etc., etc.

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A Ka-Band Detector Diode with High Sensitivity

C. G. Diskus, A. Stelzer, K. Lübke, H. W. Thim

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Altenberger Str. 69, 4040 Linz, Austria

In this work the design and matching of a zero bias InGaAs-Schottky detector diode for 35 GHz is described. High voltage sensitivity at zero bias is achieved by incorporating indium and by matching the input impedance to 50 Ω. This diode is used as the receiving part of a Doppler-radar front-end.

1. Introduction

In millimeter-wave systems suited for automotive applications Schottky-barrier diodes are used for detecting and mixing signals because of their high switching speed which results from the unipolar conduction mechanism. III-V semiconductors are the preferred materials because of their higher electron mobility at low fields compared to Silicon. Important parameters of Schottky barrier detector diodes are series resistance, barrier height, and junction capacitance. There are two types of detector diodes: zero-bias devices and detector diodes used with bias, which need a more complicated circuitry.

2. InGaAs Diode

The voltage sensitivity of a detector diode is a function of its reverse saturation current [1]. For optimum sensitivity this current has to be in the range of 10^{-6} A. To achieve this value with GaAs technology at zero bias – which is desirable to keep the circuit as simple as possible – the barrier height must be tailored to 0.22 – 0.25 eV by incorporating indium. With increasing In content the energy gap of the semiconductor is lowered from 1.42 eV (GaAs) to 0.33 eV (InAs). With $In_{0.38}Ga_{0.62}As$ the desired barrier height of the Schottky contact can be achieved.

The diodes were fabricated using epitaxial layers of GaAs and InGaAs grown by metal organic chemical vapor deposition (MOCVD) on GaAs-substrates. Ni/GeAu/Ni/Au films were evaporated thermally and by e-beam, respectively, and annealed to form ohmic contacts on n-type layers, Ti/Au and Cr/Au were evaporated and used for Schottky contacts. The ohmic contacts were recessed by wet chemical etching and the connection to the Schottky contact on the top was led over a SiO_2 bridge. The SiO_2 layers were etched in a reactive ion etching (RIE) reactor. The patterns for the contact pads, the interconnections and the circuit were transferred to the substrate using e-beam lithography. The layer sequence of the Schottky-barrier diodes is shown in Fig. 1. Details of the fabrication can be found in [2].

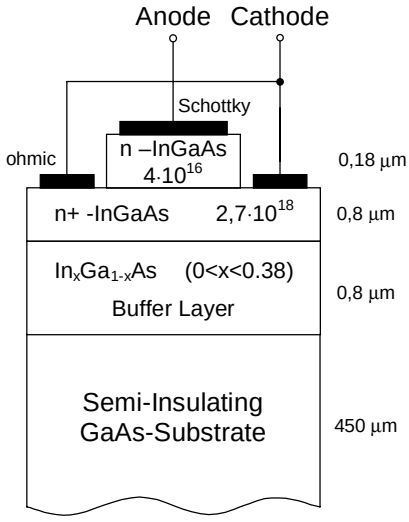

Fig. 1: Layer sequence.

The DC parameters were determined from computer controlled *I-V* measurements. The measured forward current-voltage relationship of a typical device is shown on a semi-logarithmic scale in Fig. 2. The semi-logarithmic plot also allows to calculate ideality factor, series resistance, and barrier height of the devices. A straight line was fitted to the semi-logarithmic data to extract the parameters. Typical values for reverse saturation current I_S, series resistance R_S and ideality factor n of diodes with contact area 3x3 µm^2 are shown in Table 1.

ideality factor	saturation current	series resistance	barrier height	capacitance
1.45	$8.2 \cdot 10^{-6}$ A	9.7 Ω	0.22 V	10.7 fF

Tab. 1: Typical values of $In_{0.38}Ga_{0.62}As$ Schottky barrier diodes (3 µm x 3 µm)

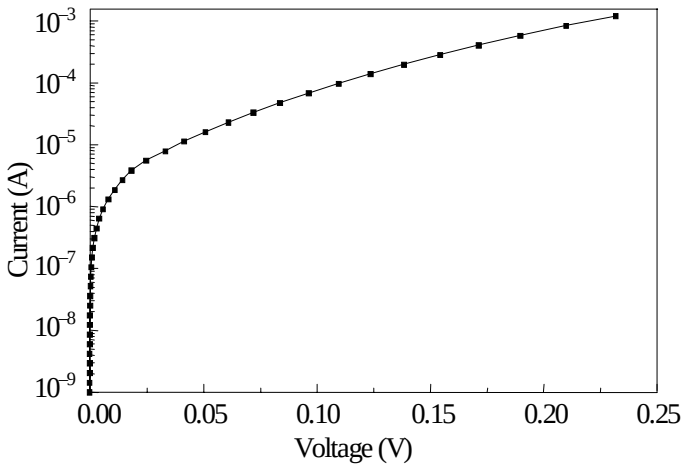

Fig. 2: Semi-logarithmic plot of measured current voltage relation.

From the measured junction capacitance of a diode with 100x100 µm^2 Schottky contact area, the junction capacitance for diodes with 3x3 µm^2 anode area can be calculated. The resulting cut-off frequency $f_{co} = 1/2\pi R_S C$ for these devices is approximately 1500 GHz.

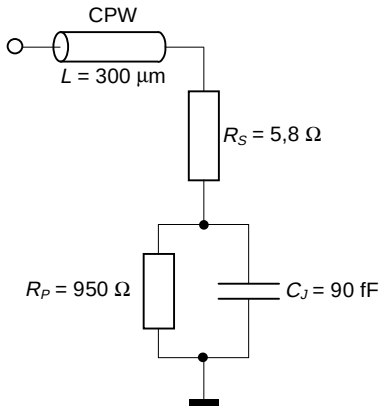

Fig. 3: Small signal model of the diode.

3. Impedance Matching

A connection of the diode to a 50 Ω microstrip line with no further impedance matching yielded a sensitivity of 1 mV/µW. In order to enhance sensibility it is necessary to match the diode impedance to the 50 Ω of the transmission line.

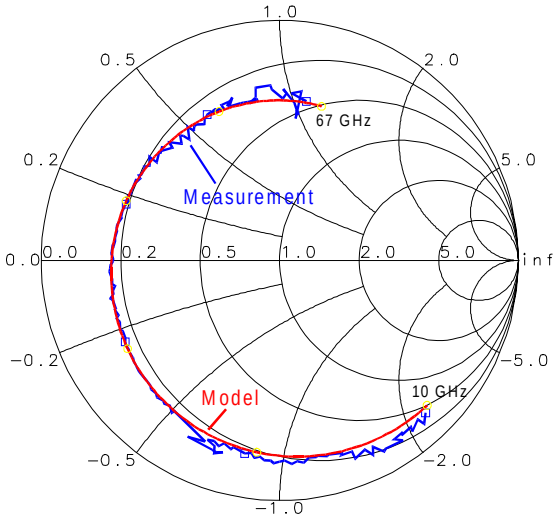

Fig. 4: Reflection coefficient of unmatched diode, frequency range 10 – 67 GHz.

Firstly, a small signal model of the diode was established by fitting the reflection coefficient (S_{11}) of the circuit shown in Fig. 3 to the measured data. The measurement of the diode was accomplished using a vector network analyzer and a wafer prober with co-

planar probe tips. For these measurements the diodes were connected via coplanar transmission lines (CPW) deposited on the semi-insulating GaAs substrate. Figure 4 shows both measured and simulated reflection coefficients. The phase shift of S_{11} is mainly caused by the coplanar transmission line between probe tip and diode.

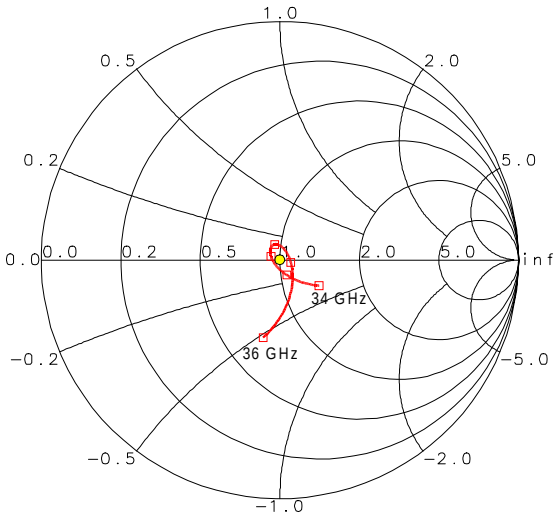

Fig. 5: Reflection coefficient of matched diode, frequency range 34 – 36 GHz.

Next, a three element T-structure matching network was optimized with respect to low S_{11} using HP-EESOF's Series IV Design Suite. The matching network was realized using microstrip technology with radial stubs serving as RF-grounds. Since the operating frequency of the radar front-end is restricted to 34 – 36 GHz a narrow band design is sufficient. Figure 5 shows the reflection coefficient obtained with the matching circuit. With this approach the voltage sensitivity exceeded 5 mV/µW [3]. The dependence of the sensitivity on the input power as well as the frequency dependence are depicted in Fig. 6. A photograph of the realized chip is shown in Fig. 7.

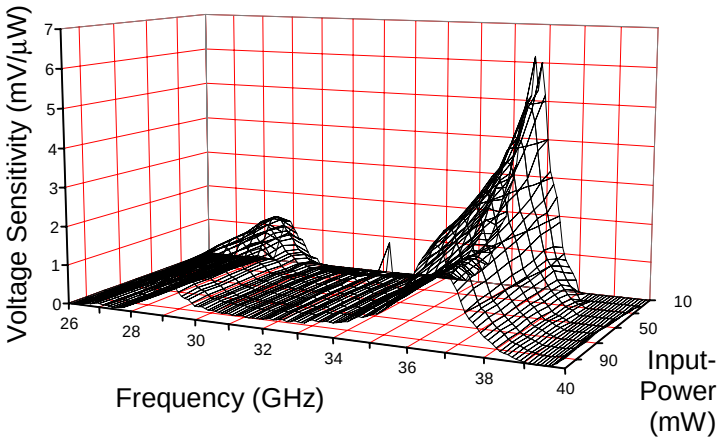

Fig. 6: Voltage sensitivity vs. frequency and input power

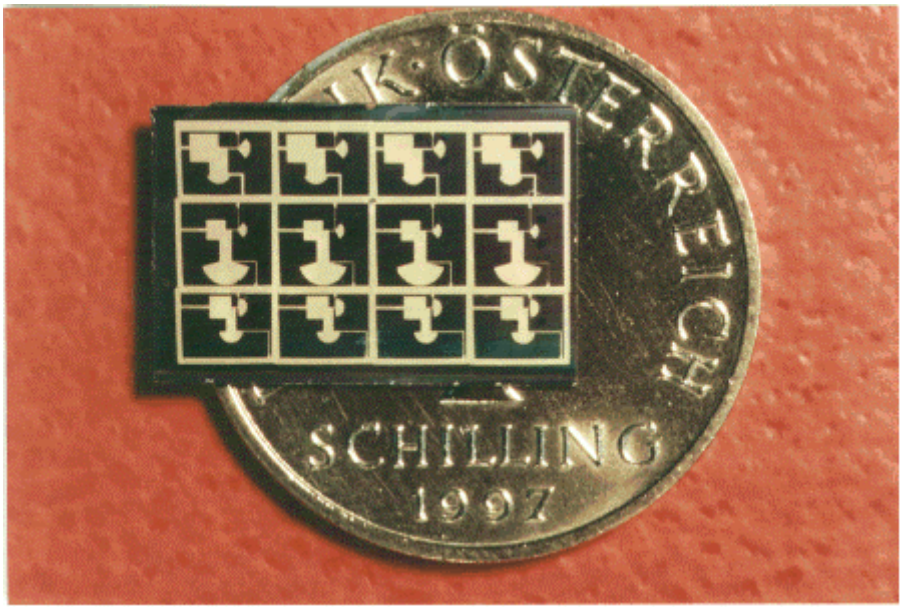

Fig. 7: Chip with three different matching circuits

4. Results

The described diode is used as a mixer in the receiving path of a Doppler-radar front-end. The signal is amplified with automatic gain control to achieve a sufficiently high signal level at the A/D-converter. A digital signal processor (DSP) analyzes the sampled signal and calculates the target speed. With a corner reflector moving at constant speed an accuracy of 0.1% is possible.

Acknowledgements

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A Time-to-Voltage Converter for Accurate Measurements of Travel Time

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The circuit presented here acts as one of the major parts in a system for highly accurate measurements of the velocity of sound in fluids – it detects the simultaneity of two signals. The range of the time differences is +/–100 ns with a resolution of several picoseconds. This has been achieved by using a special circuit concept where the resolution is only limited by noise.

1. Introduction

A circuit for highly accurate measurements of the velocity of sound in fluids has been developed at the Department of Electronics, Technical University Graz [1], [2], [3]. Based on the principle of the delay locked loop (DLL), a control loop sets the period of an oscillator equal to the travel time needed by an acoustic pulse to travel through a known distance in a fluid (Fig. 1). One of the major parts in that loop is the time-to-voltage converter. Compared to a standard phase locked loop (PLL) phase detector the demands for the circuit needed here are quite high, as the resolution should be within picoseconds. In this paper a circuit will be presented which satisfies these requirements. It has been proven to work in a range of +/–100 ns with a resolution of several picoseconds. The first version of the converter was built with standard discrete components. But it is also well suited to be built into an integrated circuit, as the second part of the paper will show. The implementation in CMOS is currently under development at the department.

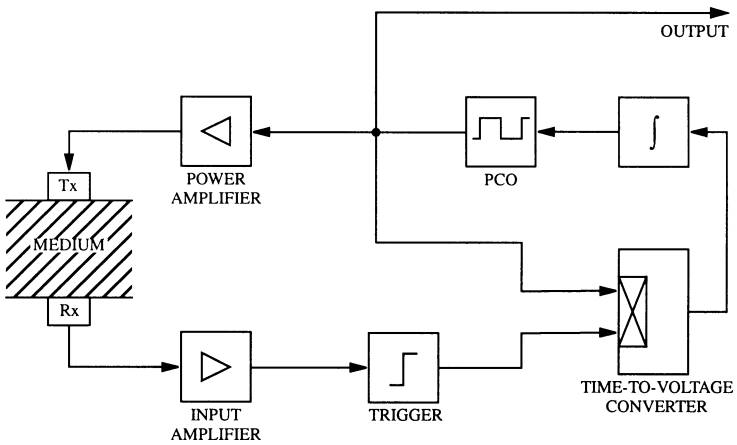

Fig. 1: The delay-locked-loop (DLL).

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1.1 The Limitation of Time Resolution

The quality of timing is determined by the accuracy of the representation of time. In the domain of electrical signals time is represented by a state transition of a signal, always keeping in mind that the finite slopes of such signals can only be an approximation of a point in time.

As a time interval always needs two signals to be defined, the systematic structure of the signals can match very well, and thus be suppressed after subtraction. If the two signals are generated on the monolithic substrate of an integrated circuit not only the systematic structure but also internal delay time drifts due to aging and temperature changes as well as supply voltage dependencies can be suppressed. Studies of CMOS circuits with delay times in the order of nanoseconds showed that time differences vary only within picoseconds. This can be understood by taking into account that the noise voltage at the input of a CMOS inverter is in the order of millivolts whereas the rise time of the input signal has a slope of 10^9 V/s.

2. The Time-to-Voltage Converter

The known principle of the charge pump phase detector [4], as used in digital PLL circuits, suffers from a dead zone if both timing signals are nearly simultaneous [5]. Although some improvements have been reported [6] this would not satisfy our requirements. Fig. 2 shows a circuit which has been developed at our department and is used in a well working system.

Switching off two currents (by Tr1 and Tr2) which are complementary but of equal value was found to be a good solution of this problem. Before being switched off, these currents flow into and out of a capacitor (C1) without charging it. The charge in the capacitor will also stay unchanged if both signals are simultaneous and thus the currents disappear at the same time. If, let's say, the signal t_1 changes its state before t_2, then the current through Tr2 charges C1 till t_2 changes state. A discharge of C1 will occur if t_2 precedes t_1. The capacitors C2 and C3, the switches S1 and S2 and the amplifier OP are used for auto zero and sample & hold of the output voltage V_a, which is referenced to 2.5 V to allow single supply.

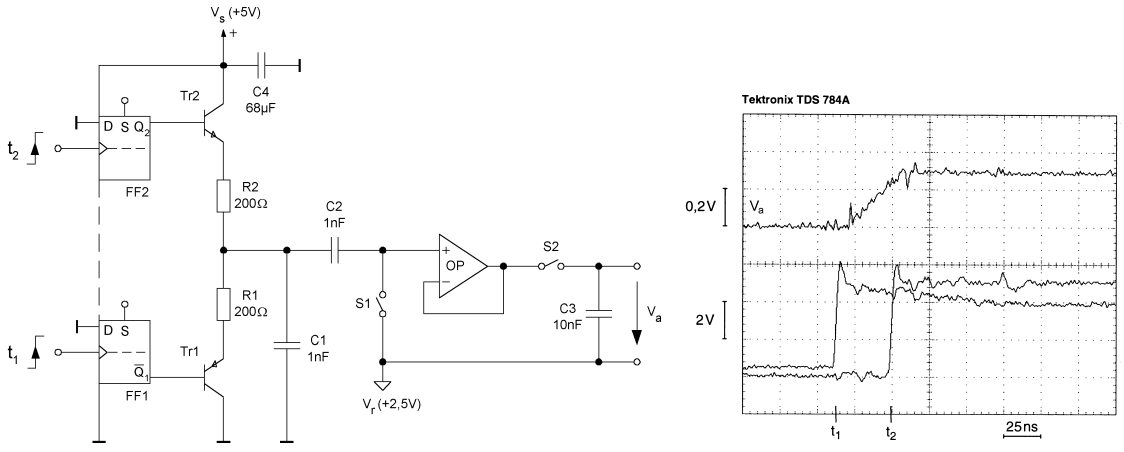

Fig. 2: The time-to-voltage converter transforms the time difference $t_2 - t_1$ into the voltage V_a.

The current set by R1 and R2 is roughly 10 mA. With a value of C1 = 1 nF this makes a factor of 10^7 V/s by which a time difference is transformed into a voltage. Thus 1 ns is represented by 10 mV – a good value compared to the observed variations of about 10 µV caused by noise.

A screen shot taken from a digital sampling oscilloscope (Tektronix TDS 784A) shows that a time difference of 37.3 ns results in a voltage V_a of 295 mV (Fig. 2, right).

2.1 The Time-to-Voltage Converter at Work

In the system shown in Fig. 1 an acoustic pulse will not be triggered at the beginning of each oscillator period. A time of about 128 oscillator periods is needed to allow acoustic resonance to fade away. This means that the oscillator can only be retuned approx. 1000 times a second, if the travel time of the pulse is in the range of 10 µs. Fig. 3 shows the output voltage V_a of the time-to-voltage converter in the steady state of the control loop. The changes observed are mainly due to the jitter of the oscillator and from acoustic interference, which are much larger than the uncertainty of the time-to-voltage converter itself.

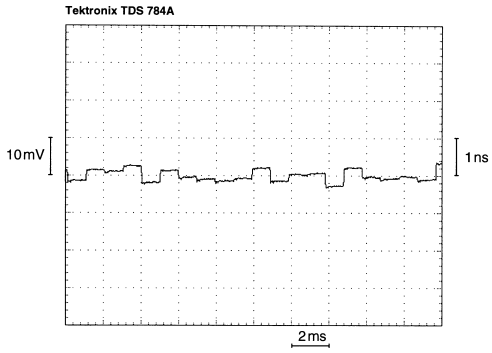

Fig. 3: Voltage V_a from a closed loop DLL which will be retuned 1000 times a second.

The output voltage is then integrated with a time constant of 1 s. This is not shown here as it is too flat. Counting the frequency of the oscillator allows to digitize the velocity of sound with a precision of 10^{-5}, which is well suited for analytical needs.

3. Implementation in CMOS

A project to design an integrated circuit of the whole system for measuring the velocity of sound in fluids is currently in work at our department. Two details of the circuit, which are of special interest in this context, are the current switches (Tr1 and Tr2) and the switches S1 and S2. As fast complementary bipolar devices are not available in standard CMOS technology a solution with MOS devices had to be found. In contrast to bipolar transistors, for MOS transistors saturation does not mean low speed. Charge injection is the more important issue here. By taking this into account a CMOS implementation of the time-to-voltage converter has been developed (Fig. 4 shows the layout). A test chip is currently fabricated by Austria Mikrosysteme International AG.

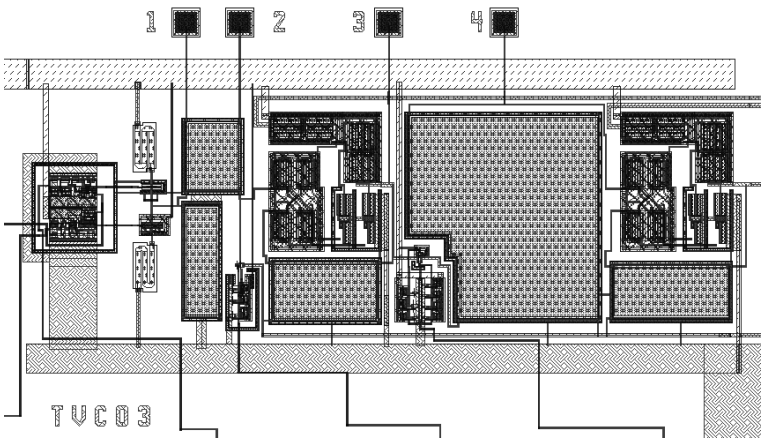

Fig. 4: Layout of the time-to-voltage converter in a 0.8 µm CMOS technology.

4. Conclusion

A novel time-to-voltage converter and its implementation in CMOS has been presented. The converter features a very high time resolution by using the systematic structure of two digital signals. A conversion factor of 10^7 V/s has been achieved and thus a resolution in the range of picoseconds has been realized. Furthermore, the circuit uses auto zero to suppress the influences of part value variations, temperature changes, and supply voltage variation.

Acknowledgements

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Internal Characterization of IGBTs Using the Backside Laserprobing Technique

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This work presents the time-resolved measurement of charge carrier concentration and temperature profiles in IGBTs by Backside Laserprobing. Calibrated numerical device simulation is employed for investigating the effects of the sample preparation on the device under test and for supporting the interpretation of the experimental results.

1. Introduction

The high operating temperature due to extensive heat dissipation has become a severe and critical issue in the optimization of modern power semiconductor devices as the blocking voltage and forward current are steadily increasing [1]. Time-resolved measurements of carrier concentration and temperature during dynamic device operation provide valuable information for the verification and calibration of the electrothermal models [2] implemented in device simulation tools. In this paper we present the thermal characterization of Insulated Gate Bipolar Transistors (IGBTs) during transient switching under shorted load conditions.

The interpretation of the results is supported by calibrated numerical device simulation. Moreover, the relevance of effects on the measurement results introduced by the sample preparation are studied by multi-cell simulation.

2. Backside Laserprobing

The Backside Laserprobing technique makes use of the dependence of the refractive index of silicon on temperature (thermo-optical effect [3]) and on carrier concentration (plasma-optical effect [4]). The modulation of the refractive index is measured by detecting the phase shift of an infrared laser beam ($\lambda = 1.3\mu m$). The laser beam propagates in vertical direction and is reflected at the top metallization layer (as illustrated in Fig. 1). Thereby, its phase is shifted by

$$\varphi(t) = 2 \cdot \frac{2\pi}{\lambda} \cdot \int_0^L \left(\frac{\partial n_{Si}}{\partial T} \Delta T(z,t) + \frac{\partial n_{Si}}{\partial n} \Delta n(z,t) + \frac{\partial n_{Si}}{\partial p} \Delta p(z,t) \right) dz, \tag{1}$$

where $\partial n_{Si}/\partial T$ is the temperature coefficient of the refractive index, $\partial n_{Si}/\partial n$ and $\partial n_{Si}/\partial p$ describe the dependence of the refractive index on the concentration of electrons and holes, respectively. ΔT, Δn and Δp are the changes of the temperature and the electron and hole density, respectively. L is the thickness of the substrate. Note that the influence of the temperature increase and the increase of the charge carrier density on the refractive index are opposite in sign.

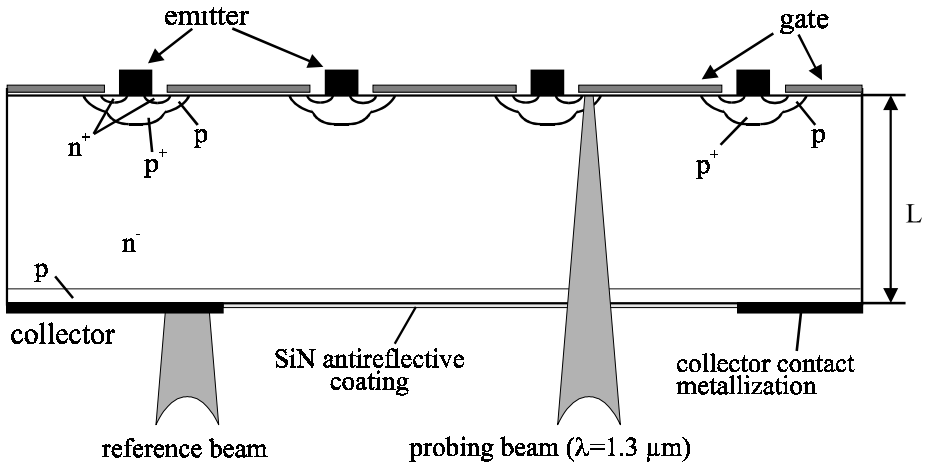


Fig. 1: Cross section view of an IGBT with probing and reference laser beam. The probing beam can be placed at different positions within the window area.

To detect the phase change we use a modified version of a heterodyne laserprober setup [5] outlined in Fig. 2. A probe and a reference beam with slightly shifted wavelengths are positioned inside and outside the device active area, respectively, as shown in Fig. 1. The lateral resolution is determined by the laser beam spot size of approximately 3 µm. The beams reflected from the device surface metallization interfere on the detector yielding a signal of the form $\sin(2\Delta\omega t+\varphi(t))$, where $\varphi(t)$ is the phase evolution according to Eq.1. The beat frequency $2\Delta\omega=2(\omega_1-\omega_2)$ determines the lateral distance of the two laser beams within the device structure and their wavelength shift. The phase signal $\varphi(t)$ is obtained from the time domain analysis of the detector signal.

The measurement technique requires to etch a window of 70 µm x 70 µm in size in the collector contact metallization. This window opening is done by a photolithographically structured etching in a two step process using HNO_3 and HF acids. Thereby, the contact metallization, which consists of a few different layers, can be removed without etching the silicon. To suppress multiple reflections within the silicon substrate (Fabry-Perot-interference), the window area is coated with an antireflective layer of Si_3N_4 by a PECVD deposition process.

The devices used in this study are vertical IGBTs with 1200 V blocking voltage. The schematics of the cross section is given in Fig. 1. The devices are operated under shorted load conditions with U_{CE} up to 500 V. Thus, operating conditions with high power dissipation as they typically occur in industrial applications can be investigated.

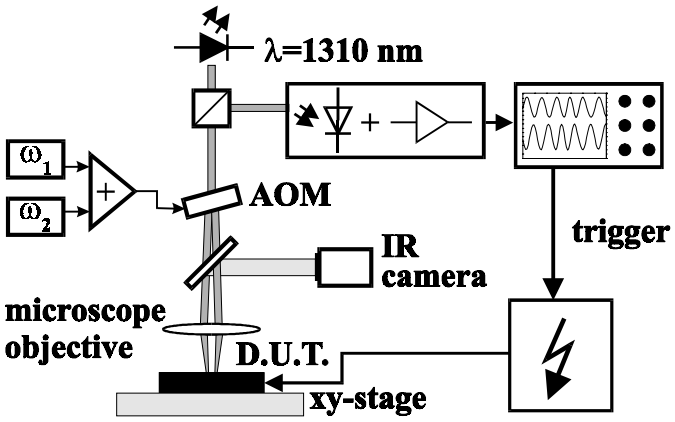


Fig. 2: Experimental setup of the Backside Laserprobing technique.

3. Numerical Modeling

For the quantitative evaluation of the experimental results, the device performance is simulated using a self-consistent electrothermal extension of the drift-diffusion model, as it is implemented in the general-purpose device simulator DESSIS^{ISE} [6]. The electrothermal models for the transport parameters have been calibrated with reference to the forward characteristics and the internal carrier concentration and temperature profile, which have been determined by Internal Laser Deflection measurements [2].

By simulating several IGBT cells, the effect of the window in the collector metallization on the device behavior is investigated. A current crowding causes a local increase of the carrier concentration at the edges of the window. Due to this current crowding the MOS structures, which can be seen through the window, feature a higher power dissipation. The resulting inhomogeneity of the lateral temperature profile is about 15% at the topside, whereas the temperature rise at the bottom due to the window preparation is negligible (see Fig.3).

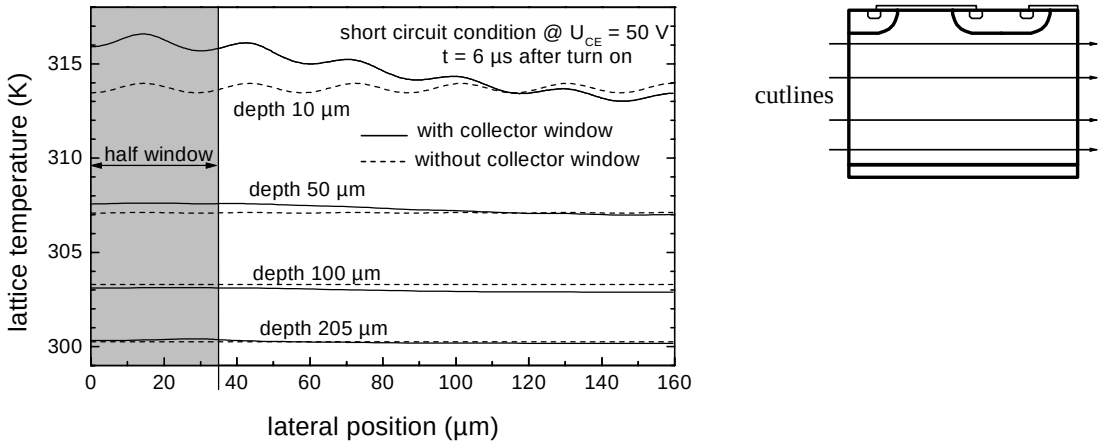
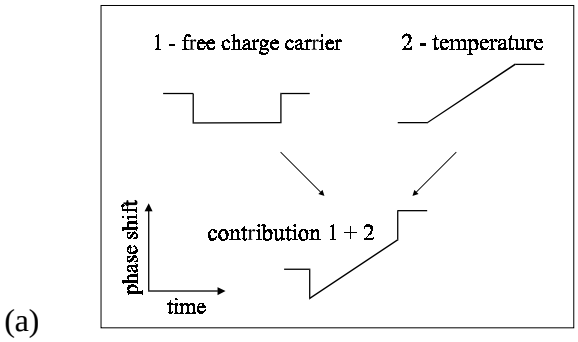


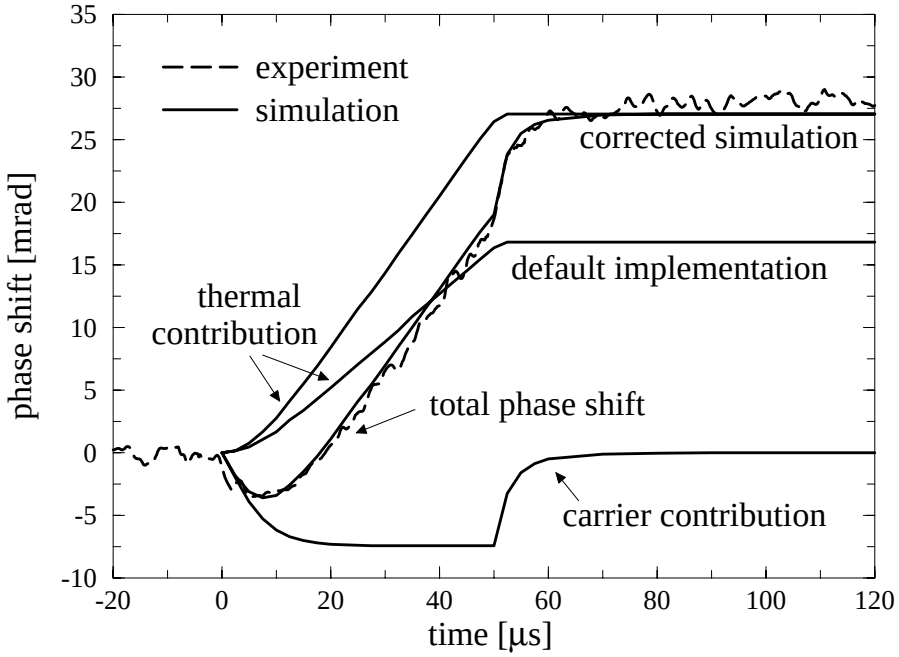
Fig. 3: Lateral temperature profiles at different depths of the prepared IGBT device (short circuit operation at U_{CE} = 50 V). Due to symmetry only one half of the structure is simulated. Thus, the center of the window is located at the lateral position of 0 µm. The schematics on the right hand side shows the 4 cutlines.

4. Experimental Results

In order to investigate the contribution of the carrier concentration on the phase shift signal, the device is investigated at low power dissipation (U_{CE} biased at 2 V). The measured phase shift for a pulse duration of $\tau = 50\ \mu s$ is shown in Fig. 4. The contributions of carrier concentration and temperature are of the same order of magnitude. When the pulse duration is increased, the contribution of the carrier concentration does not change, as the current remains unaffected. The contribution due to the temperature increase, however, changes according to the varying power dissipation.



(a)



(b)

Fig. 4: Phase shift at low power dissipation under short circuit condition ($U_{CE} = 2$ V, pulse duration $\tau = 50\ \mu s$). (a) Schematics of charge carrier and temperature contribution to the total phase shift. (b) Comparison of measured and simulated phase shift. The default implementation of the device simulator does not take into account the Peltier heating at the semiconductor/metal interface of the collector contact [7]. Adding this extra heat source yields the correct thermal contribution.

In the case of short circuit operation at high collector emitter voltages the thermal contribution becomes dominant. The phase change due to a change of the charge carrier density can be neglected. Therefore, the phase shift $\varphi(t)$ is a measure of the integral of the temperature change along the beam path.

The IGBTs are designed to withstand shorted load conditions for 10µs. According to this specification gate pulses of 15 V height and length of 10 µs are applied. The power dissipation is controlled by varying the collector emitter voltage U_{CE} between 50 and 500 V. The current is nearly independent of the applied voltage as it is confined by the MOS-structure of the IGBT. For different voltages U_{CE} the measured phase shift is shown in Fig. 5. The constant power dissipation during a current pulse causes a linear rise of the phase shift. A small increase of the phase shift is observed after pulse turn-off for about 40 µs. This is due to heat conduction from the edge of the window to the center of the window [8]. After this short time effect the cooling of the device is visible on a time scale of several 100 µs.

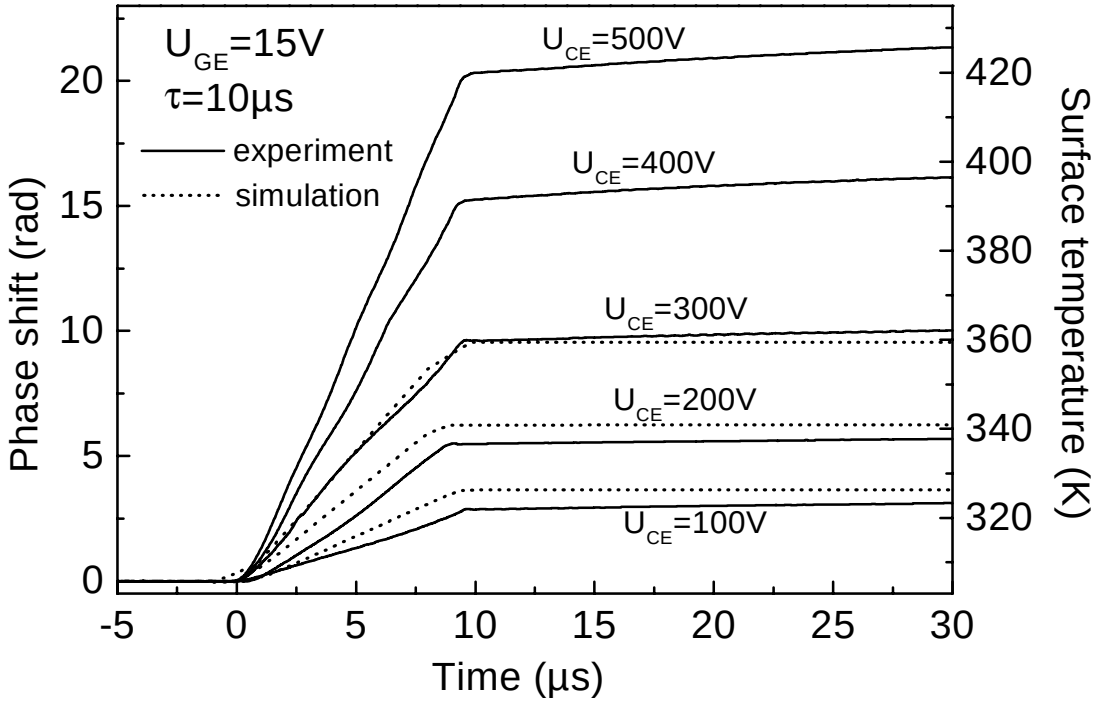


Fig. 5: Phase shift for short circuit operation at high collector emitter voltages U_{CE} with a pulse duration of 10µs. The surface temperature is calculated assuming a linear vertical temperature distribution.

The vertical temperature profile (in direction of the beam propagation) during the current pulse is dominated by the power dissipation in the channel region. Therefore, a linear decrease of the lattice temperature with increasing depth can be assumed. Thus, the phase shift can be interpreted as a measure for the maximum temperature in the device during the heating pulse (cf. scaling on the right hand side in Fig. 5). A temperature increase of $\Delta T = 120$ K is obtained at $U_{CE} = 500$ V at the end of the heating pulse. This temperature is far below the critical values assumed for latch-up, thus verifying safe operation at short circuit bias.

5. Conclusion

The internal transient behavior of vertical IGBTs under short circuit conditions has been studied by employing the Backside Laserprobing technique. Charge and temperature induced phase signals are analyzed in order to determine the temperature variation in the surface region. The influence of the preparation of the samples has been investigated by accurate numerical simulations, which have shown to be indispensable for the correct interpretation of the experimental results.

Acknowledgements

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A Novel Technology for the Assembling of ASIC's and MEMS

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A miniaturized air bag sensor system with a completely novel connecting technology of the micro machined component and the ASIC part was developed, in order to allow a significant increase of the production yield and reliability in comparison with the technologies currently used by e.g. BOSCH or MOTOROLA.

This connecting technology, which is based on a soldering technique, avoids the problems associated with the combination of the micro machining technology with the conventional semiconductor technology, by allowing a completely separated production of both components. Additionally, the required vacuum sealing of the micro mechanical component is performed. An ideal electrical shielding of the device as well as a electrical contact between the micro mechanical part and the ASIC unit are obtained simultaneously. Among others, one of the key solutions introduced with this technology is to form a metal solder ring onto the micro machined unit which is very fragile and has a difficult surface topography. This is done using the float off technique in combination with a special patterned double layer dry resist evaporation mask.

After successful technological development this device is ready for industrial pilot production now.

Optoelectronics

3D-Laser-Entfernungsbildaufnahme

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Nowadays our world becomes more and more a digitized world in almost every aspect (speech, sound, imaging, communications, etc.). At present one major effort is to achieve a more or less complete digital 3D representation of natural as well as man-made objects such as workpieces, art's work, buildings, complete scenes, or even whole landscapes.

Various methods for achieving 3D images have been developed, e.g., mechanical touch probes mounted on co-ordinate measuring machines (contouring), laser-based triangulation, 3D reconstruction from multiple images and projection of light fringes. 3D imaging laser sensors based on the time-of-flight principle deliver high productivity and accuracy. 3D data acquisition is accomplished by fast line scanning based on angular deflection with a number of rotating reflective surfaces for one dimension. Rotating the whole scanning device or moving the whole scanner platform (e.g. by airplane, airship, helicopter, or by car) provides the second dimension. This new tool provides a compelling alternative to traditional techniques by accurately measuring structures, even when they are inaccessible or in an unsafe area, due to the high measurement capability up to ranges of hundreds of meters to naturally reflecting objects.

3D laser imaging facilitates 3D data acquisition in a vast area of application: 3D-imaging of buildings for architecture and preservation of cultural heritage (castles, ruins, relics of the past), reverse engineering (plant as-built records), scene acquisition for virtual reality modeling, acquisition of digital terrain models of residential areas, whole districts or even towns, including vegetation and structures, topographic mapping of quarries or open pit mines, cliff faces, and dimensional measurements of all kind of vehicles.

Die Laser-Entfernungsbildaufnahme ermöglicht die Erstellung von räumlichen 3D-Modellen realer Objekte und damit die digitale Beschreibung von Objekten. Ein Entfernungsbild setzt sich aus einer Vielzahl von einzelnen Entfernungsmeßergebnissen zusammen. Die einzelnen Meßergebnisse bestehen zumindest aus der Entfernung zwischen Sensor und Objekt und der Raumrichtung, in der die Entfernungsmessung durchgeführt wurde. Darüber hinaus dienen Meßgrößen wie zum Beispiel Reflektivität des Objektes, Farbinformation, etc. der weiteren Beschreibung und damit der Verfeinerung des Modells.

Zur Gewinnung von Entfernungsbildern stehen unterschiedliche Verfahren zur Verfügung: die mechanische Abtastung der Oberfläche von Formen ist auf eher kleine Objekte beschränkt und stellt teils einschränkende Anforderungen an die Oberfläche (Festigkeit). Die laser-basierte Triangulation bzw. verschiedene Lichtschnittverfahren in Kombination mit Präzisionsdreh- und Verschiebetischen ergeben eine hohe Meßrate und eine hohe Genauigkeit, sind aber wieder auf kleine Meßvolumina beschränkt. Die Rekonstruktion von Entfernungsinformation aus zwei oder mehr 2D-Aufnahmen aus

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unterschiedlichen, definierten Positionen erfordert zum einen eine gewisse Strukturierung der Objektoberfläche und spezielle Beleuchtungsverhältnisse, zum anderen einen beträchtlichen Rechenaufwand.

Die Laser-Entfernungsbildaufnahme nach dem Prinzip der Laserpuls-Laufzeitmessung ermöglicht die rasche und genaue 3D-Datenerfassung in einem großen Entfernungs- und Winkelbereich unabhängig von den Beleuchtungsverhältnissen. Nachfolgend wird ein kommerzieller 3D-Entfernungsbildsensor beschrieben, der in einer kompakten und robusten Bauweise für den Einsatz auch unter schwierigen Umgebungsbedingungen geeignet ist.

Mögliche Anwendungen und Einsatzgebiete der 3D-Entfernungsbildaufnahme nach dem Laserpuls-Laufzeitverfahren sind unter anderem:

- 3D-Bilderfassung von Gebäuden in der Architektur, Archäologie und im Denkmalschutz (Burgen, Schlösser, Ruinen, Ausgrabungsstätten etc.)
- Reverse Engineering: Erfassung von Industrieanlagen und anderer Objekte zur Planerstellung und zum Vergleich mit den ursprünglichen Erstellungsdokumenten (z.B. in Chemiewerken, Atomkraftwerken, Bohrinseln, Zwischendecken und Verkabelungen in Wolkenkratzern, etc.)
- 3D Modellierung von realen Szenen für virtuelle Räume (Virtual Reality) für Telepresence, Virtual Filmstudios, 3D Animationen, etc.
- Erstellung von digitalen Höhenmodellen von Wohngebieten, Wohnbezirken bis hin zu kompletten Städten einschließlich der Vegetation und der Gebäude
- Geländevermessung im Bergbau, speziell im Tagbau, z.B. zur Volumsbestimmung vor und nach einer Sprengung
- Vermessung von Lawinenhängen zur Verbesserung der Vorhersage
- Vermessung von Fahrzeugen aller Art

Die primären Meßdaten eines Entfernungsbildes stellen zunächst eine sogenannte Punktewolke im lokalen Koordinatensystem des Sensors dar. Über die Definition der Eigenposition und der Orientierung des Sensors in einem „globalen“ Koordinatensystem kann die Punktewolke auch in diesem globalen Koordinatensystem dargestellt werden. Bei einer einzelnen Entfernungsbildaufnahme bleiben im allgemeinen durch Abschattung einzelne Teile des Objektes unerfaßt. Durch die Aufnahme mehrerer Entfernungsbilder aus unterschiedlichen Positionen können die Abschattungslücken gefüllt werden. Die Registrierung der einzelnen Bildaufnahmen im globalen Koordinatensystem ergibt dann eine umfassende Charakterisierung der Oberfläche des Objektes.

Bei der 3D-Repräsentierung eines Objektes ist im allgemeinen eine Darstellung durch Flächen gewünscht, die das Objekt hinreichend genau mit minimalem Speicheraufwand beschreiben. Der effiziente und automatisierte Übergang von der Repräsentation durch eine 3D-Punktewolke auf eine Modellierung durch Flächen bzw. 3D-Primitive ist ein aktuelles Gebiet der Forschung.

Der 3D-Entfernungsbildsensor der Type RIEGL LMS-Z210 (Abbildung 1) beruht auf der Laser-Entfernungsmessung nach dem Puls-Laufzeitverfahren und der optomechanischen Ablenkung der Meßstrahlen zur Abtastung des Aufnahmebereiches.

Abb. 1: 3D-Entfernungsbildsensor RIEGL LMS-Z210.

Beim Puls-Laufzeitverfahren wird die Zeit zwischen dem Aussenden eines kurzen Laserpulses und dem Empfangen des Pulses nach der Reflexion am Zielobjekt gemessen und daraus die Entfernung zum Zielobjekt errechnet. Durch den Einsatz modernster Mikroelektronik kann dabei eine Meßgenauigkeit für eine Einzelmessung im Zentimeterbereich erzielt werden bei einer gleichzeitigen Meßrate von bis zu etwa 20.000 Messungen pro Sekunde. Die zum Einsatz kommenden Laser emittieren im nahen Infrarot, die Strahlaufweitung beträgt einige wenige Millirad und die Pulsdauer liegt im Bereich einiger Nanosekunden.

Zur Bildaufnahme muß die Meßrichtung des „eindimensionalen“ Laser-Entfernungsmessers abgelenkt werden. Dies kann entweder in langsamer Weise durch mechanische Rotation des gesamten Laser-Entfernungsmessers um zwei oder mehrere Achsen erfolgen, oder aber durch Vorsetzen einer optomechanischen Ablenkeinrichtung. Im 3D-Sensor LMS-Z210 werden die Meßstrahlen durch ein kontinuierlich rotierendes Polygonrad linear abgelenkt, wodurch eine schnelle Zeilenablenkung mit einer Zeilenfrequenz bis zu 40 Zeilen pro Sekunde realisiert wird. Generell kann die zweite Ablenkung auf unterschiedliche Weise erfolgen: durch lineare Bewegung des zeilenabtastenden Sensors über das Meßobjekt z.B. auf einem Hubschrauber, durch Vorsetzen einer weiteren, langsamen optomechanischen Ablenkeinrichtung, oder durch Rotation des Sensors um eine zur Zeilenablenkung orthogonale Achse. Im 3D-Sensor LMS-Z210 wird durch Rotation der Zeilenablenkeinrichtung und Teile des Laser-Entfernungsmessers die zweite Ablenkung realisiert. Durch diese Kombination ergibt sich eine kompakte und robuste Bauform mit einem weiten, jedoch variablen Bilderfassungsbereich von bis zu 80 mal 340 Grad.

Das Entfernungsbild setzt sich aus einer Vielzahl von einzelnen, unabhängigen Meßergebnissen zusammen, die zeilenweise organisiert sind. Jedes Einzelmeßergebnis besteht aus der Meßentfernung, zwei Meßwinkeln im sensoreigenen polaren Koordinatensystem, und der Intensität des empfangen Laser-Echopulses.

Die Spezifikationen des 3D-Sensors sind in den Tabellen 1 und 2 zusammengefaßt. Eine Zusammenstellung von Aufnahmezeiten für unterschiedliche Aufnahmebereiche und Auflösungen ist in Tabelle 3 enthalten.

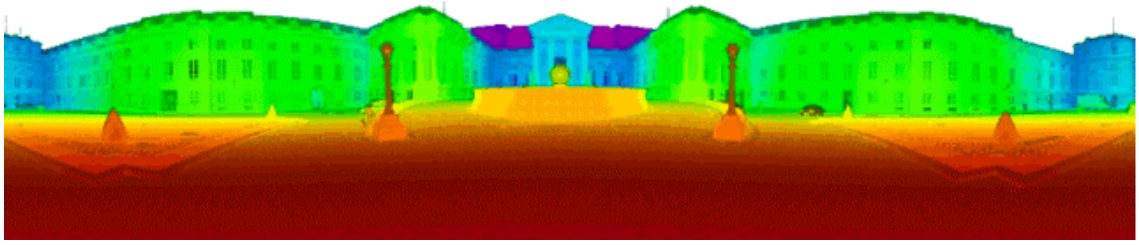


Abb. 2: Beispiel eines farbkodierten Entfernungsbildes, Bilderfassungsbereich 80° x 340°; das Bild zeigt das französische Parlament in Paris (Assemblée Nationale).

Measurement range [1]	up to 350 m for natural targets, reflectivity ≥ 80 % up to 150 m for natural targets, reflectivity ≥ 20 %
Minimum range	typ. 2 m
Measurement accuracy [2]	typ. ± 2.5 cm, in the worst case ± 10 cm
Measurement resolution	2.5 cm
Measurement rate	20 000 Hz (peak)
Laser wavelength	0.9 µm (near infrared)
Beam divergence [3]	approx. 3 mrad
Eye safety	Class 1 for the scanned beam
Interfaces	Parallel interface, Serial interface RS232

1) typical values for average conditions. In bright sunlight, the operational range is considerably shorter than under an overcast sky. At dawn or at night the range is even higher.
2) standard deviation, plus distance depending error ≤ 20ppm
3) 1mrad corresponds to 10 cm beamwidth per 100 m of distance

Tab. 1: Spezifikationen – Entfernungsmesser.

Line scan (fast scan)	
Scanning range [1]	± 40° = 80° total
Scanning mechanism	rotating polygonal mirror
Scanning speed [2] [5]	nominal 20 scan per second
Frame scan (slow scan)	
Scanning range [3]	up to ± 170° = 340° total
Scanning mechanism	motor-driven optical head
Scanning speed [4] [6]	nom. 5 deg per second

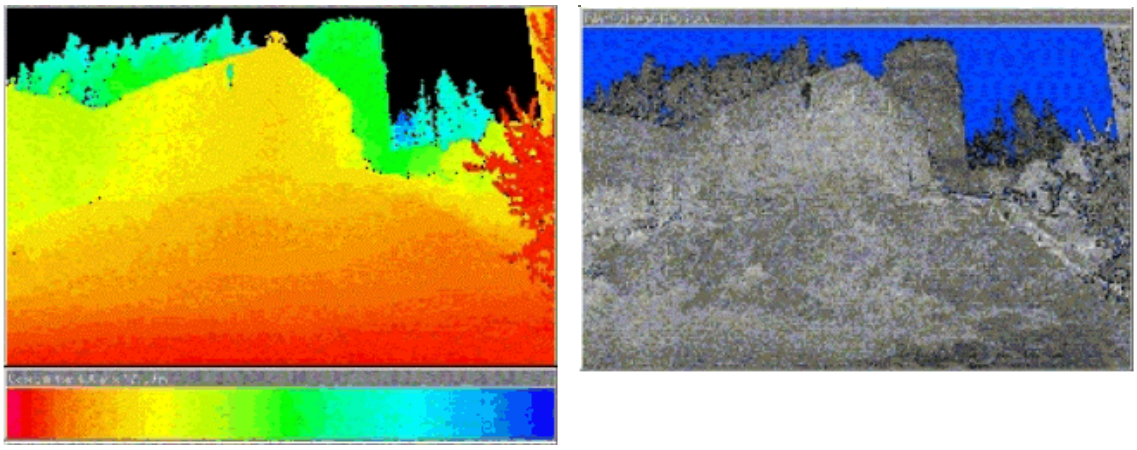
1) scanning range can be reduced, if desired, without impact on scan speed
2) can be set by software commands between 10 scans/sec and 40 scans/sec
3) can be set between 0 deg and 340 deg
4) can be set to speeds up to 20 deg per seconds
5) scan speed and angular scan resolution has to be set not to exceed the maximum measurement rate of the rangefinder
6) defines together with scanning speed of polygonal mirror wheel the angular resolution of the vertical direction

Tab. 2: Spezifikationen – Optomechanische Abtasteinrichtung.

Abtastbereich	Anzahl der Messungen	Anzahl der Messungen	Winkelschritt-weite	Datenmenge	*Aufnahmezeit*
80 x 80 deg	222 x 222	49.284	0.36 deg	385 kB	8 sec
80 x 80 deg	444 x 444	197.136	0.18 deg	1.5 MB	30 sec
80 x 80 deg	740 x 740	547.600	0.10 deg	4.2 MB	1 min 34 sec
80 x 40 deg	222 x 111	24.642	0.36 deg	193 kB	5 sec
80 x 40 deg	444 x 222	98.568	0.18 deg	771 kB	15 sec
80 x 340 deg	222 x 900	219.780	0.36 deg	1.5 MB	23 sec
80 x 340 deg	444 x 1800	799.200	0.18 deg	6.1 MB	2 min 00 sec

Tab. 3: Beispiele für die Aufnahmezeit und die Datenmenge bei unterschiedlichen Bilderfassungsbereichen und Auflösungen.

Die Entfernungsbilddaten werden an Standardschnittstellen zur Verfügung gestellt, so daß eine Datenübernahme auf einen Standard-PC oder Laptop in einfacher Weise möglich ist. Eine einfache Visualisierung der Entfernungsbilder erfolgt durch Farb-Kodierung, bzw. durch Verwendung der Intensitätsinformation. Einfache Meßaufgaben wie zum Beispiel der Abstand zweier Objektpunkte im Raum können direkt über die farbkodierten Bilder durchgeführt werden. Der Export der Daten in standardmäßigen 3D-Datenformaten ermöglicht die Weiterverarbeitung der Daten zur Modellerstellung.



(a) (b)

Abb. 3: Burg Kollmitz: (a) farbkodiertes Entfernungsbild, (b) Intensitätsbild.

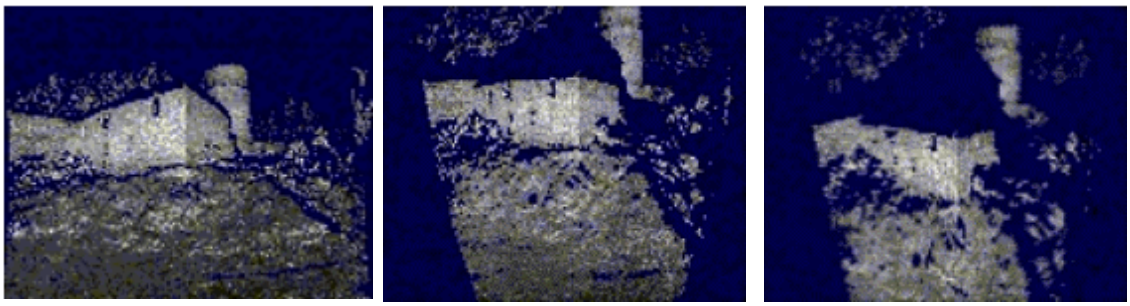


Abb. 4: Burg Kollmitz – verschiedene VRML Ansichten.

Ein Beispiel für die farbkodierte Visualisierung zeigt Abbildung 3. Das Objekt ist die Burgruine Kollmitz, NÖ. Der Enternungsbereich für die Farbkodierung ist 4 m (rot) bis 123 m (blau). Eine einfache 3D-Repräsentation ist durch Exportieren der Daten im VRML-Format (virtual reality modeling language) und Betrachtung der Szene mit einem sogenannten VRML-Browser. Die Abbildung 4 zeigt diese Visualisierung mit unterschiedlichen Standpunkten der virtuellen Kamera. Deutlich zu erkennen ist die Abschattung mancher Teile des Objektes. Zur vollständigen Modellierung sind daher weitere Aufnahmen erforderlich.

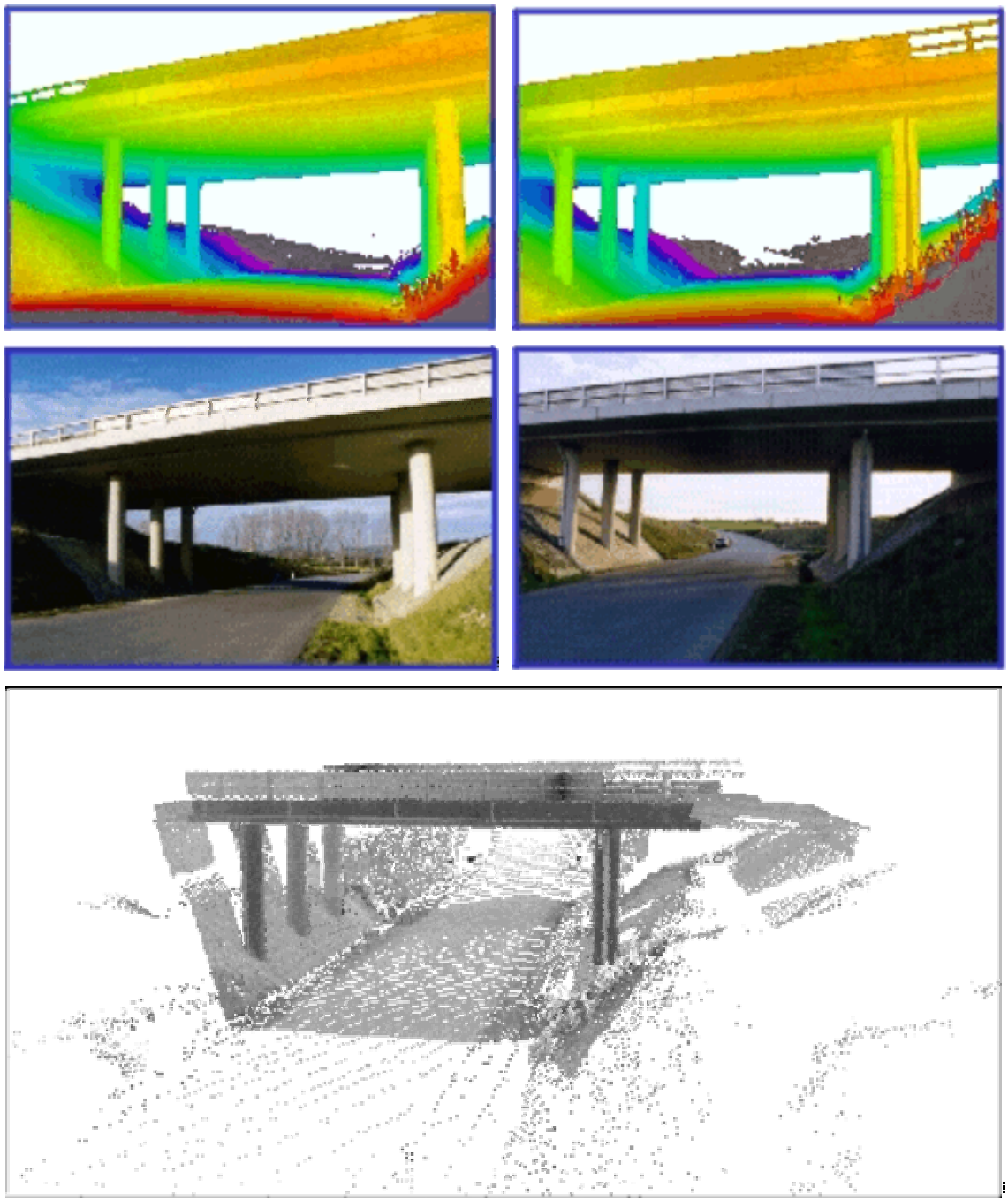
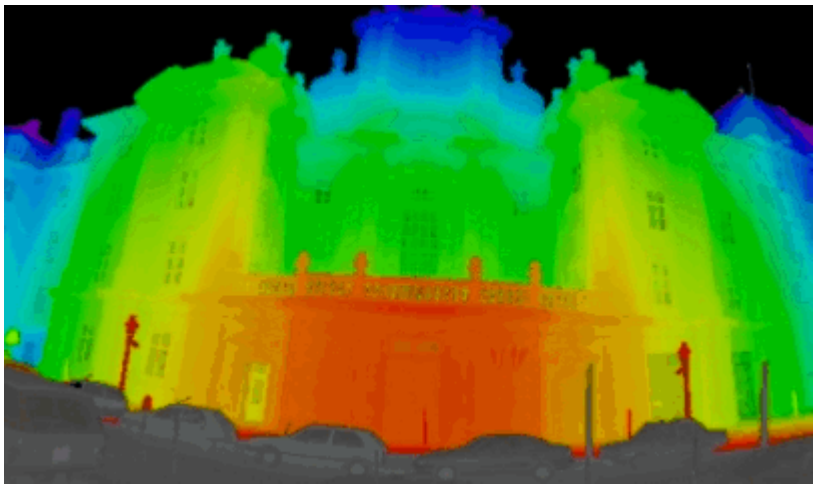


Abb 5: 3D Modell einer Brücke - zusammengesetzt aus zwei einzelnen Entfernungsbildern: (a) Entfernungsbilder, (b) Intensitätsbilder, (c) VRML 3D Modell.

Ein Beispiel für die Registrierung mehrerer Entfernungsbildaufnahmen in einem gemeinsamen Koordinatensystem zeigt die Abbildung 5. Eine Brücke wurde von zwei Seiten aufgenommen und die Daten mit der Kenntnis der Aufnahmepositionen und der Orientierung des Sensors in ein Koordinatensystem im VRML Format exportiert. Das entstehende 3D Model kann nun von beiden Seiten betrachtet werden, und ein „virtueller Flug“ unter der Brücke hindurch ist möglich.


(a)


(b)


(c)

Abb. 6: Außenaufnahme der Kirche am Hof: (a) Konventionelles Farbbild, (b) Entfernungsbild, (c) Normalprojektion.

Ein Beispiel für die Erfassung von Kulturdenkmälern ist in der Abbildung 6 wiedergegeben. Sie zeigt die Außenansicht der Kirche am Hof, Wien, als Farbbild und als farbkodiertes Entfernungsbild. Aus diesem Entfernungsbild kann in effizienter Weise eine Normalprojektion der Fassade erstellt werden, wobei der Abstand zur Normalebene wiederum farbkodiert wiedergegeben ist.

Die Abbildung 7 zeigt einen Teil des Innenraums der Kirche wieder als farbkodiertes Entfernungsbild. Die Normalprojektion des Gewölbes (oben farbkodiert, unten Intensität des Laserechos) zeigt klar die Abweichung des Gewölbes von der Rechtwinkeligkeit.

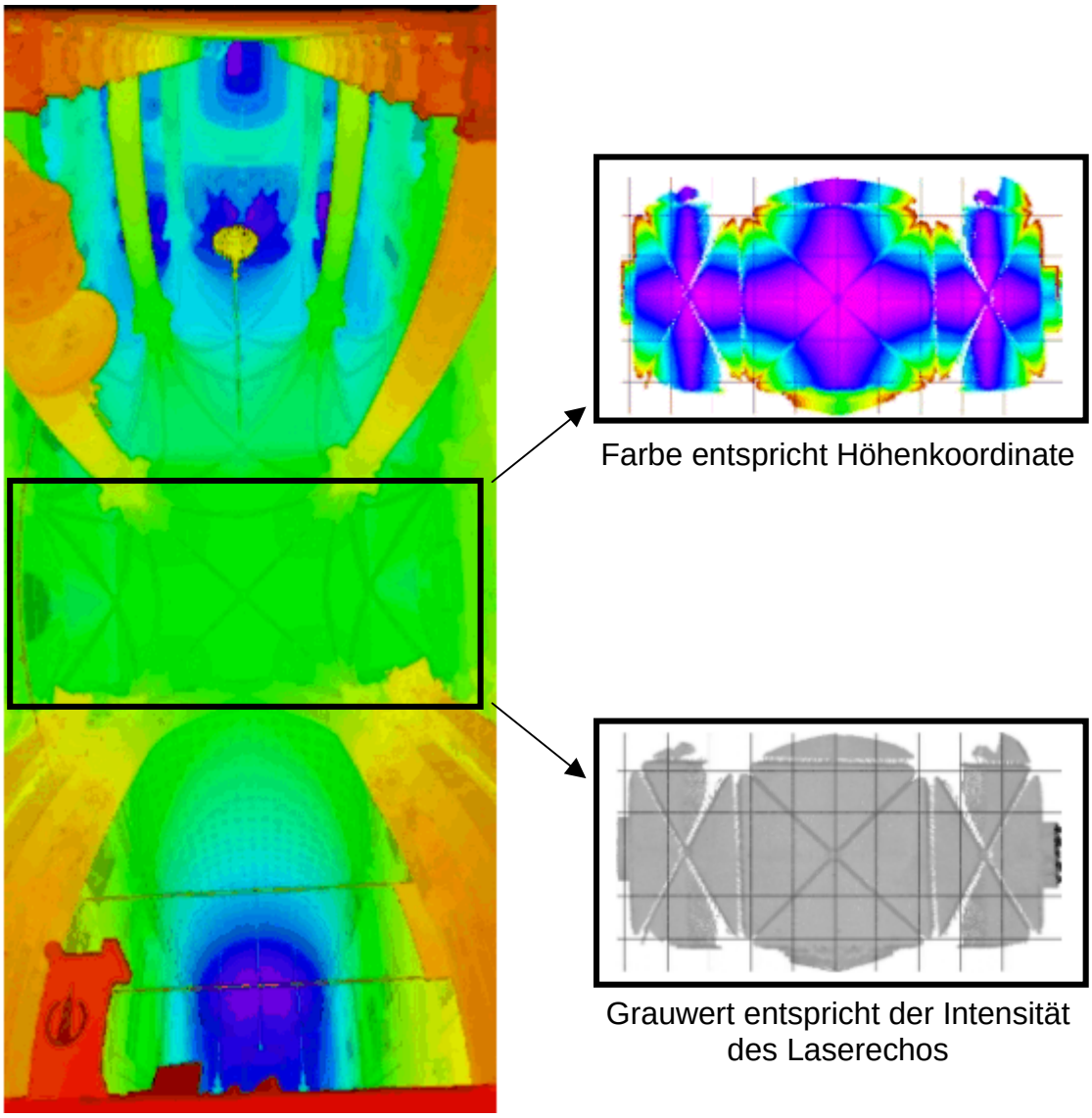


Abb. 7: Innenaufnahme der Kirche am Hof – Normalprojektion des Gewölbes.

Recent Developments on III-V Heterostructure Laser Diodes

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Recent advances in materials technology and device design now allow the fabrication of laser diodes from the mid-IR to the UV spectral regions. This paper presents some of the latest progresses on the technology of the III-V semiconductor materials and reviews the present status on advanced device concepts, such as vertical cavity surface emitting lasers (VCSELs) and quantum cascade lasers.

Significant developments in wide-gap III-V nitride semiconductors have recently led to the improvement of the lifetime of short-wavelength InGaN multi-quantum-well lasers. An essential step towards higher reliability has been the ELOG technique (epitaxially laterally overgrown GaN), by which the lateral growth of GaN over a masked area produces areas with a reduced number of threading dislocations, above which high-performance heterostructures can be grown [1]. With this method an estimated lifetime of more than 10000 h under cw operation at room temperature has been demonstrated. A further progress is expected by replacing the hitherto used sapphire substrates by epitaxially grown GaN substrates, which are made with the ELOG technique, and the subsequent removal of the sapphire substrate [2]. This also will markedly improve the thermal conductivity, and cleaved mirror facets may easily be achieved. The schematic structure of the corresponding InGaN laser diode for a 400 nm wavelength is shown in Fig. 1.

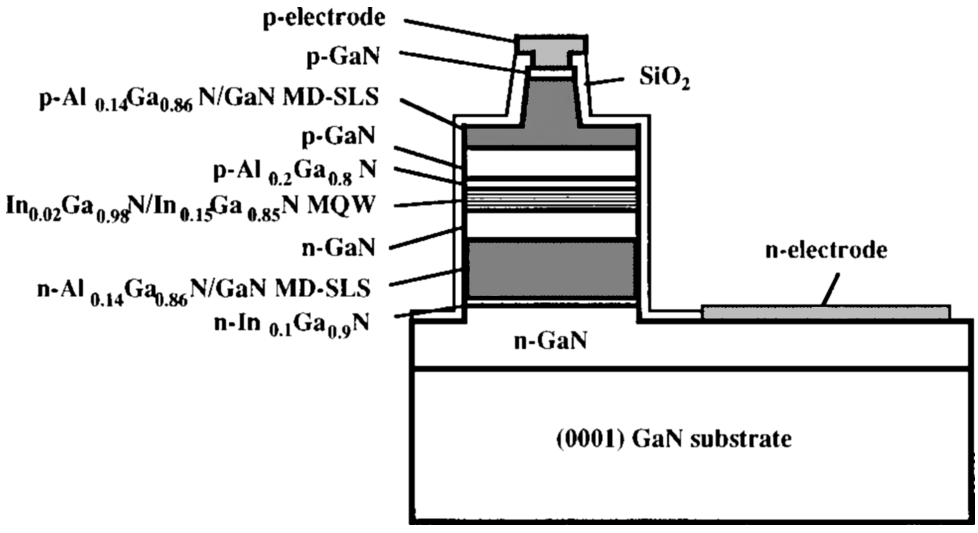

Fig. 1: InGaN laser diode on a GaN substrate (@ *Appl. Phys. Lett.* **72** (1998) 2014).

While the laser diodes made so far with this technique showed a relatively large threshold current density of the order 7 kA/cm^2, the lifetime at cw room-temperature operation is around 800 h being four times longer than for laser diodes made on sapphire substrates with equal threshold current density. The reduction of the threshold current density to below 4 kA/cm^2 is therefore expected to improve the lifetime to above 10000 h [2].

Presently, much effort is being paid to realize vertical cavity surface emitting lasers (VCSEL) for the wavelength range of 1.3 to 1.55 µm. While the Al(Ga)As/GaAs VCSEL shows excellent performance for wavelengths around 0.8 – 1 µm [3], [4], it reveals difficult to fabricate electrically pumped VCSELs for longer wavelengths that operate cw at room temperature. This striking difference with respect to the short-wavelength devices is mainly because the Al(Ga)As/GaAs material system exhibits several features that enable the laser oscillation with gain medium lengths of the order of only 100 nm, which are required in VCSELs. First of all, AlAs and GaAs show a large refractive index contrast around 0.5 for wavelengths around 0.9 µm, so that epitactic Bragg mirrors with a high reflectivity (>99 %) may easily be prepared with a moderate numbers of layer pairs (> 15) yielding total thicknesses of the order 2 – 3 µm with low refraction losses. Secondly, the binary lattice-matched AlAs/GaAs Bragg mirrors exhibit low specific thermal resistivity, which together with the relatively low pair number yields low thermal resistance, which is essential for the cw operation at room temperature. Thirdly, the application of isolating and waveguiding aluminum oxide apertures made by steam oxidation of AlAs layers [5] leads to strong transverse waveguiding in narrow devices with sub-mA threshold currents. On the other hand, InP-based heterostructures for 1.3 to 1.55 µm wavelength consist of quaternary InGaAsP, Al(Ga)AsSb, or AlGaInAs compounds that show an order of magnitude larger specific thermal resistivities [6] and – with the exception of the antimonides [7] – a significantly smaller refractive index contrast (0.25 – 0.3) than AlAs/GaAs [8]. Consequently, higher pair numbers (>30) are required for the Bragg mirrors yielding higher diffraction losses and markedly higher thermal resistances. Finally, the waveguiding oxide apertures have not yet been applied, because no suited compounds exist in the GaInAsP and AlGaInAs material systems that are lattice-matched to InP and can be steam oxidized to form the aperture. However, by the use of AlAsSb, which can be lattice-matched to InP, oxide apertures may be feasible also in long wavelength VCSELs [9].

Besides the investigation of InP-based VCSEL structures, therefore, also the application of GaAs-based VCSEL structures for 1.3 to 1.55 µm is being considered. In the latter case, approaches are investigated to maintain the superior AlAs/GaAs Bragg mirrors and the oxide aperture but to replace the active region with a material of smaller bandgap energy. To this end, InAs and InGaAs quantum dot structures have been developed [10], [11], and a 1.15 µm quantum dot VCSEL on GaAs has been demonstrated [12]. A second approach is the application of the new compound GaInAsN, which principally can be grown lattice-matched to GaAs and should cover the bandgap energy range from 0 to 1.42 eV [13]. The band gap energy versus lattice constant diagram of this compound is displayed in Fig. 2 showing a strong bowing and the possibility to fabricate GaInAsN lattice-matched to GaAs. Also with this concept a VCSEL was demonstrated at 1.18 µm wavelength [14], however, with a rather large threshold current density. Optimum performance at 1.55 µm wavelength has been achieved so far with the wafer-fusing technique [15] by which an InGaAsP/InP active region is being sandwiched between wafer-fused GaAs-AlGaAs Bragg reflectors as shown in Fig. 3. Cw threshold currents are as low as 0.8 mA at room temperature. The maximum cw lasing tempera-

ture achieved today with wafer-fused VCSELs at 1.55 µm wavelength is 64 °C, and pulsed operation has been obtained up to 100 °C [16].

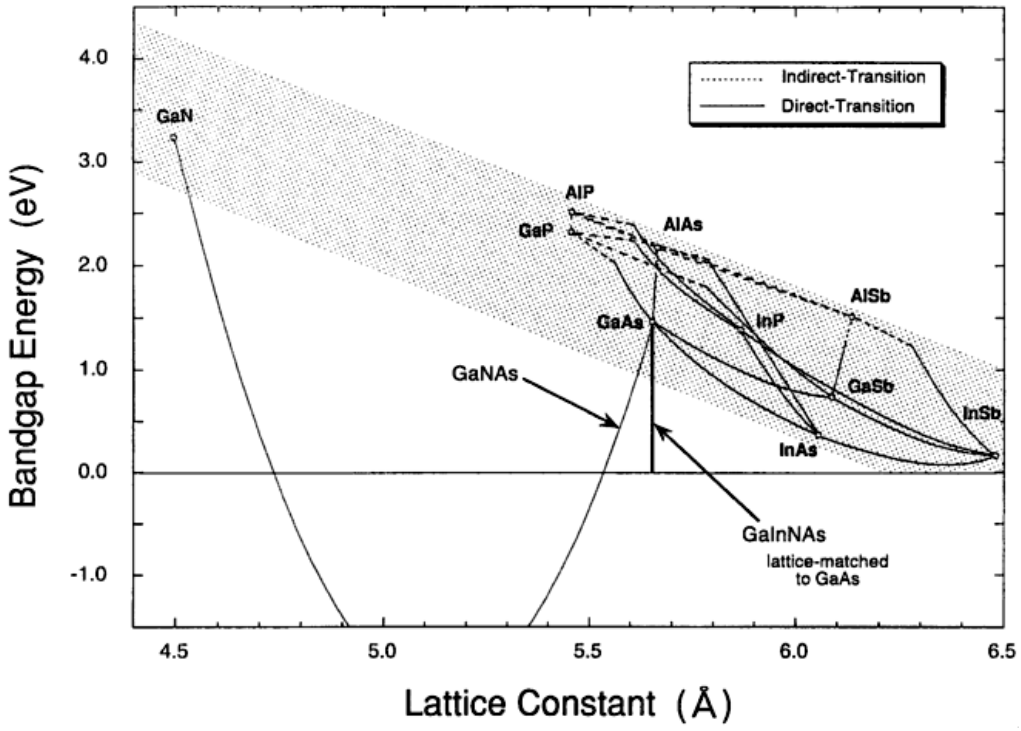

Fig. 2: Band gap energy vs. lattice constant of various III-V compound semiconductors (*@ IEEE J. Sel. Top. Quantum Electron.* **3** (1997) 719).

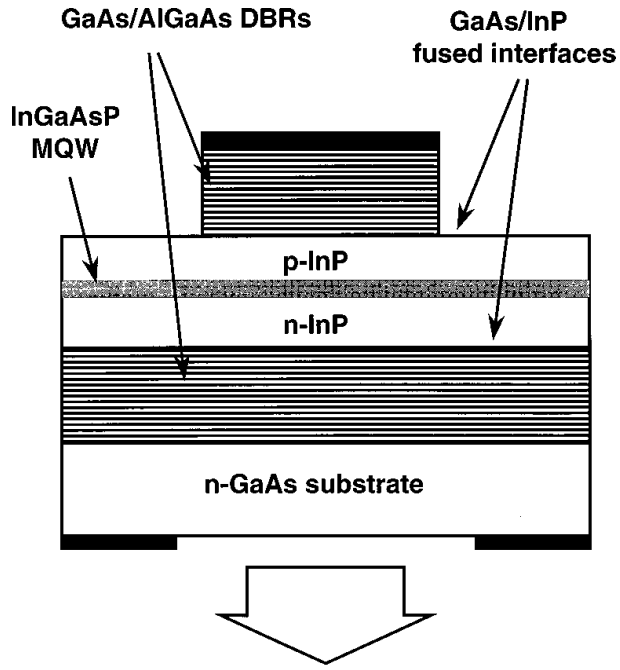

Fig. 3: Wafer-fused InGaAsP VCSEL for 1.55µm wavelength (*@Appl. Phys. Lett*. **72** (1998) 1814).

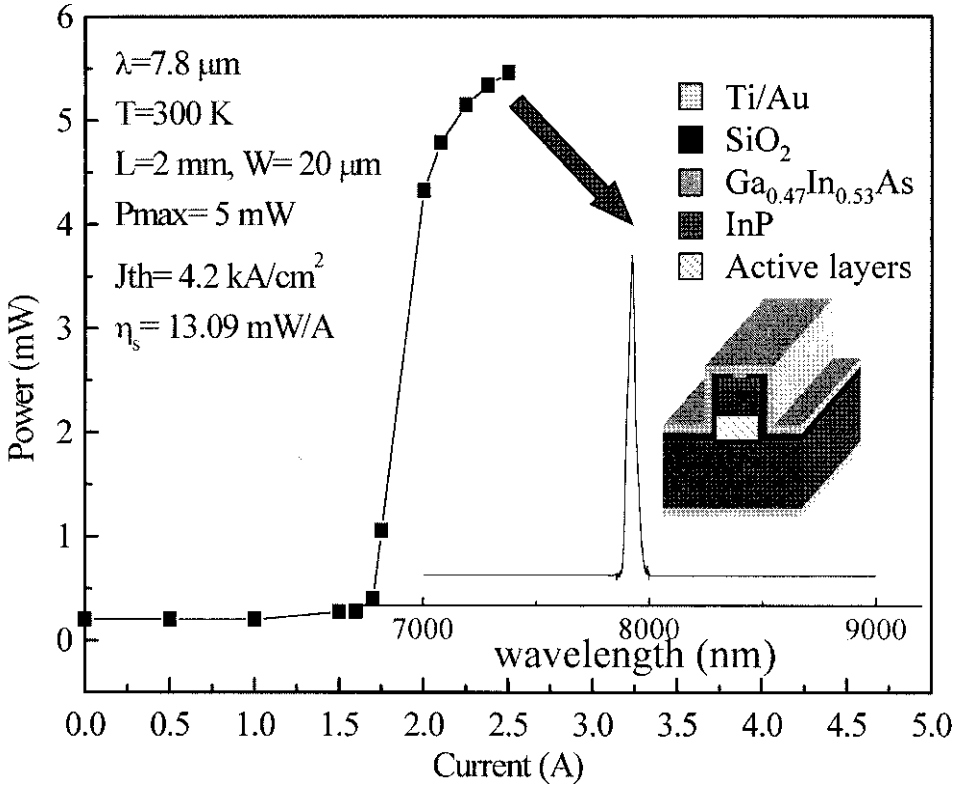

Fig. 4: Room-temperature pulsed operation of a 7.8µm QC laser (*@Appl. Phys. Lett.* **74** (1999) 173).

As spectroscopic and sensing applications become more attractive, particularly with respect to compactness and cost, if semiconductor light sources for wavelengths larger than 2 µm are available, much effort is being paid for developing suited laser diodes. While the well-established InGaAsP/InP material system is still capable for wavelengths just above 2 µm, the wavelength range from 2 to 4 µm will mainly be covered by antimony-based devices. For wavelengths larger than 4 µm novel laser diode concepts, such as the quantum cascade (QC) laser [17], become interesting. The QC laser, which is a unipolar device based on intersubband transitions in the conduction band of multiple quantum well structures, therefore, has intensively been studied worldwide and gained considerable progress. Today InP-based QC lasers are available with wavelengths from about 3.4 µm [18] to 17 µm [19]. At a wavelength of 7.6 µm QC lasers can be operated up to 160 K in cw and 325 K in pulsed mode [20], and first sensing applications have been reported [21]. A recent result on a 7.8 µm QC laser [22] operated in pulsed mode at room temperature is shown in Fig. 4. Also distributed feedback QC lasers have been presented exhibiting single longitudinal mode operation [23], and first devices on GaAs substrates were reported [24], [25]. The performance of the QC laser is strongly affected by the LO phonon relaxation between the intersubband levels, which mainly determines the threshold current and temperature dependence of QC lasers.

A different type of QC lasers, the interband cascade laser (ICL), has also been reported as a promising optical source for wavelengths beyond 2.5 µm, which is based on interband transitions in type II superlattices [26] that particularly occur in antimony-based compounds. A representative conduction and valence band structure of an ICL is shown in Fig. 5. Laser operation at 4 µm was reported up to temperatures of 285 K [27]. Due to the large band offsets in these compounds a considerable degree of freedom principally

exists to adjust the wavelength, and the shortest wavelength achieved so far with these lasers is 2.9 µm. Theoretically, the wavelength range between 2.5 and 7 µm should be covered with this approach [27]. Differing from the QC laser, the ICL devices do not suffer from phonon relaxation, however, Auger relaxation is the dominant nonradiative relaxation path. Considering the early stage of development, essential progress can be expected with these novel approaches for long-wavelength semiconductor lasers. In particular, a further increase of the maximum temperature for cw operation at wavelengths beyond 2 µm will greatly enhance the applicability of laser diodes in the future and will lead to new applications in sensing and spectroscopy.

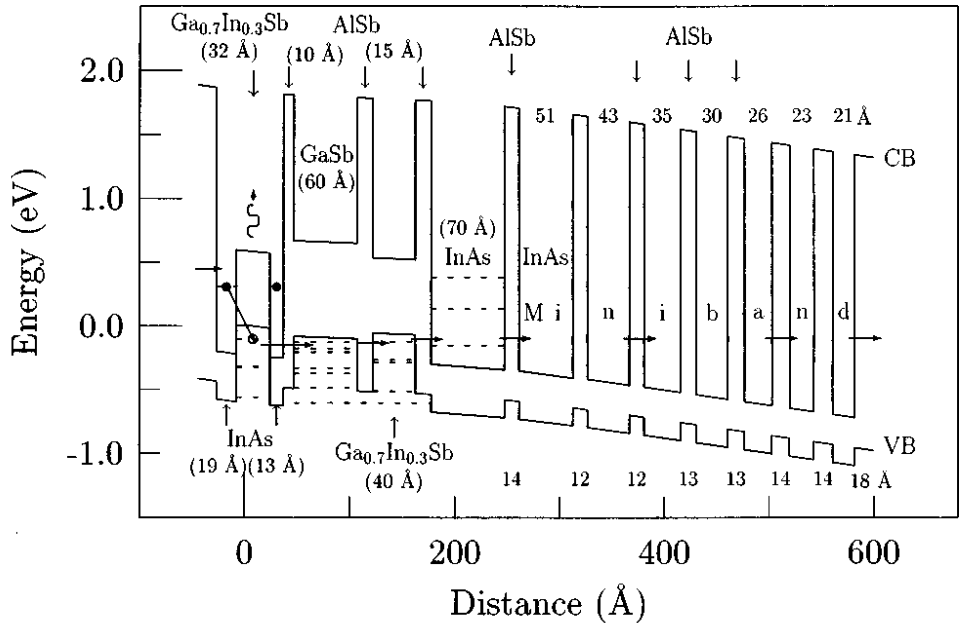

Fig. 5: Interband cascade laser conduction and valence band structure (@ *Appl. Phys. Lett.* **72** (1998) 2370).

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In-situ-Spurenüberwachung mit abstimmbaren MIR Diodenlasern

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1. Spektroskopische Eigenschaften von MIR-Diodenlasern

1.1 Spektrale Abstimmbarkeit und Helligkeit

Die Anwendbarkeit von Diodenlasern läßt sich aus deren Eigenschaften erkennen. Die spektralen Merkmale einer Bleisalz-Laserdiode werden in der folgenden Modenkarte dargestellt:

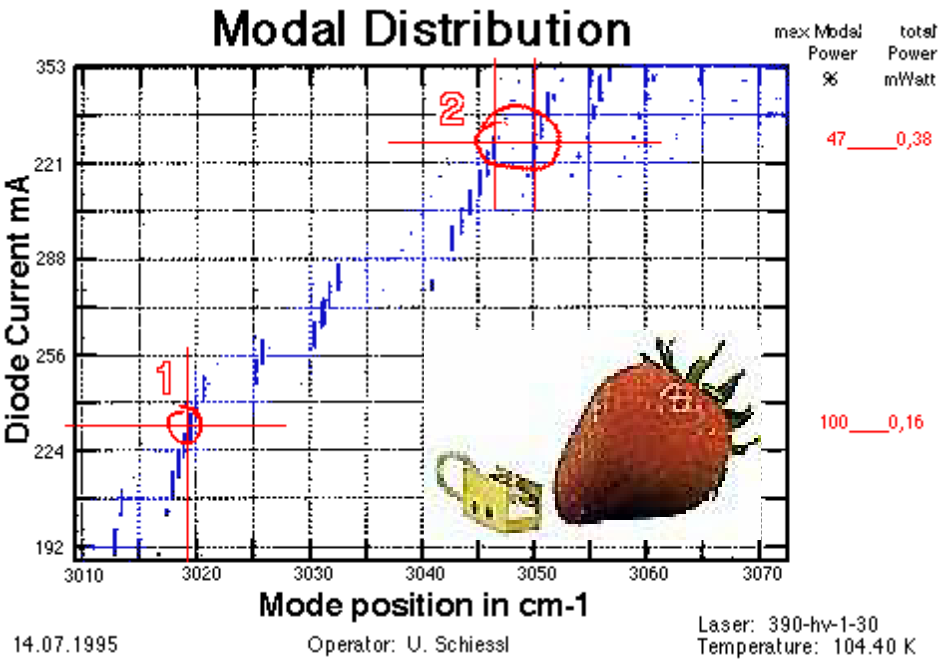

Abb. 1: Modenkarte: Leistung und Abstimmbarkeit einer Bleisalz-Laserdiode von *Laser Components.*

Es gibt keinen Laser, der einem anderen gleicht. Sowohl Leistung als Modenspektrum sind unterschiedlich. Die Emissionsfrequenz der Diodenlaser ist durch die Temperatur und den injizierten Strom gegeben. Die Temperatur ist nur langsam einstellbar, während

[1] www.muetek-infrared.de

die Diode dem Strom unmittelbar folgt. Bei den kommerziell angebotenen Bleisalz-Diodenlasern liegt die optimale Betriebstemperatur für spektroskopische Anwendungen zwischen 20 und 120 K. Für Wellenlängen zwischen 3 und 10,5 µm genügt eine Kühlung mit flüssigem Stickstoff.

1.2 Betriebsweise der Bleisalz-Diodenlaser

Die Frequenz des Lasers läßt sich mit Hilfe des Stroms schnell durchstimmen, sodaß in den meisten Anwendungsfällen der Strom als Steuerelement fungiert, hingegen die Temperatur als feste Betriebsgröße eingestellt wird. Einige ausgesuchte Stellen im Modenspektrum können *mono-mode* sein. Falls diese *mono-mode*-Stelle genau mit einer Molekülabsorption zusammenfällt, werden solche Diodenlaser gerne zum Monitoring von Molekülen ausgesucht, da sich diese eine Mode genau über die Moleküllinie abstimmen läßt. Meist wird die Frequenz des Lasers durch eine Stromrampe schnell und wiederholt durchgefahren. Bei *Lock-in*-Verfahren wird der Laser zusätzlich moduliert. Bei der *Rapid Scan*-Methode wird das direkte Spektrum mit Hilfe von Transientenrecordern aufgenommen und aufaddiert..

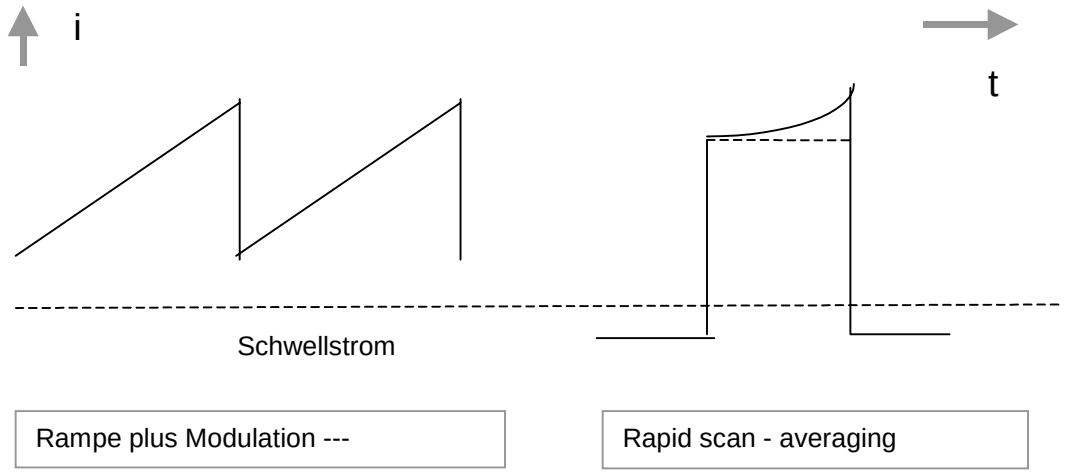

Abb. 2: Die zwei am häufigsten angewendeten Ansteuerungsarten mit der dazugehörigen Datenverarbeitungsmethode.

1.3 Vergleich zur konventionellen Spektroskopie

Beim Vergleich der spektroskopischen Eigenschaften konventioneller MIR-Spektrometer und abstimmbarer Diodenlaser sind die Hauptunterschiede in der nachfolgenden Abbildung (Abb. 3) und der Tabelle 1 übersichtlich dargestellt:

1.3.1 Strahlführungseigenschaften

Die Emission des Laserstrahls rührt von einer fast punktförmigen Fläche mit einer Ausdehnung von 10 µm x 20 µm. Die Abstrahlung erfolgt in einen Kegel von etwa 60°. Die Abbildungseigenschaften nachgeschalteter optischer Elemente wirken deshalb beinahe ideal. Die Divergenz eines parallel kollimierten Bündels von 15 mm Durchmesser liegt bei ca. 1 mrad. Der Laserstrahl bleibt auf lange Strecken gut kollimiert, was ihn zur Überwachung auf lange Stecken (km) prädestiniert.

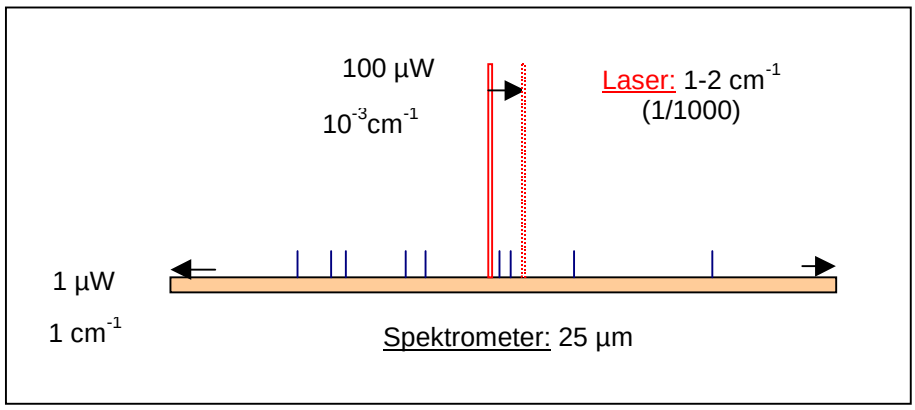

Abb. 3: Vergleich MIR-Diodenlaser mit Spektrometer.

Umgekehrt geht durch die hervorragenden Fokussiereigenschaften des Diodenlasers bei Abbildung auf Fasern von <100 µm kein Licht durch Überstrahlung verloren. Mit zunehmender Verfügbarkeit von MIR-Fasern und Raumtemperatur-Lasern erhöhen sich die Einsatzmöglichkeiten rasch.

1.3.2 Schnelle Abstimmbarkeit und Modulierbarkeit

Die Laserdiode ist etwa 0,2 mm klein, hat keinen nennenswerten Widerstand in Durchlaßrichtung, nahezu keine Kapazität und Induktivität, sodaß eine Modulation bis 1 GHz möglich ist. Praktisch wird die hohe Abstimmgeschwindigkeit der Diode angewendet. Diese ist eher durch die Ansteuergeräte begrenzt als durch den Laser. Der Laser kann in 10 µsec eine oder mehrere Molekülabsorptionslinien mit gutem Signal/Rausch-Verhältnis überstreichen.

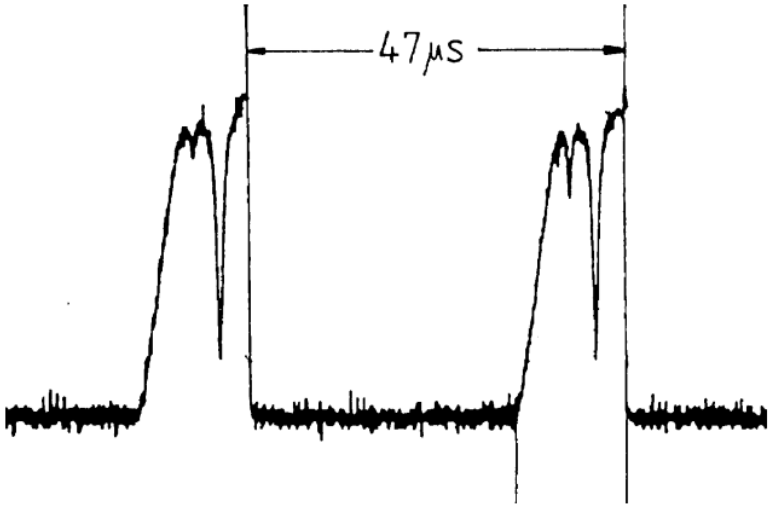

Abb. 4: CO-Absorption während des Aufbaus einer Stoßwelle: Die Absorptionslinen werden vom Laser innerhalb von 14 µsec überstrichen (Roth et al., Universität Duisburg).

Merkmal	**Konvent. Spektrometer**	**Diodenlaser**
Abstimmbarkeit	1 – 25 µm	step-tunable 100 cm^{-1}, kont. abstimmbar 1 – 2 cm^{-1}
Spektrale Helligkeit	1 µW/ cm^{-1}	100 µW/10^{-3} cm^{-1}
Strahlführung	eher divergent	Punktfokus/Parallelität
Schnelligkeit	msec	µsec

Tab. 1: Die Lasereigenschaften in der Übersicht und im Vergleich zum konventionellen Spektrometer.

2. Anwendungsübersicht der Diodenlaser im Vergleich zur konventionellen Spektroskopie

Merkmal	**Konvent. Spektrometer**	**Diodenlaser**
Anzahl Spezies	Übersichtsspektrum	Überwachung eines Zielanalyten pro Laser
Empfindlichkeit	< ppm	< ppb
Selektivität	0.1 cm^{-1} (100 mbar)	0.001 cm^{-1} (10 mbar) (Isotopen)
Strahlführung	eher konventionell	Faseranwendungen
Kinetische Vorgänge	> msec	> nsec

Tab. 2: Anwendungsübersicht der Diodenlaser im Vergleich zur konventionellen Spektroskopie.

Aus den oben dargestellten Merkmalen folgt die unterschiedliche Anwendung beider Techniken: Die spektrale Helligkeit des Lasers hat bei schmalen Absorptionslinien hohe Empfindlichkeit und Selektivität zur Folge. Dieser Vorteil gegenüber den konventionellen Techniken schwindet, je breiter Absorptionslinien oder Absorptionsbanden von Stoffen werden. Die häufigste Anwendung liegt deshalb bei Gasen. Sind die Absorptionen breit (< 50 cm^{-1}) wird der Laser jedoch immer noch vorteilhaft bei schnellen Vorgängen und Faserstrahlführung eingesetzt. Während das konventionelle Spektrometer durch seine weite kontinuierliche Abstimmbarkeit eine Menge von Molekülkomponenten erfaßt, reicht die geringe für die Spektroskopie nutzbare kontinuierliche Abstimmbarkeit des Lasers im allgemeinen nur für die Überwachung eines einzigen oder weniger Zielanalyten.

2.1 Hauptanwendungen der Diodenlaser in der *in-situ*-Überwachung

Im folgenden sind zwei grundsätzlich unterschiedliche Betriebsarten der Diodenlaser vorgestellt:

2.1.1 Messung der Konzentration von einzelnen Zielanalyten

Bei der Untersuchung der *luftchemischen Vorgänge* bei der Bildung des Ozonlochs spielt der Diodenlaser eine große Rolle. Innerhalb eines europäischen Forschungspro-

jektes kartographiert eines unserer MIR-Spektrometer von einem Flugzeug aus die HNO_3-Konzentration der Atmosphäre.

Wegen seiner spektralen Helligkeit, seiner Selektivität und der exzellenten Strahlführungsqualitäten kommt der Diodenlaser bei der *in-situ-Spurenüberwachung* zur Anwendung. Mit dem Laser können selbstverständlich auch hohe Stoffkonzentrationen gemessen werden, nur sind die meisten konventionellen Techniken wesentlich billiger.

Man rechnet heute bei Bleisalzdiodenlasern mit 30.000 – 50.000 EURO pro Analyt. Wegen der Komplexheit der Steuerung eines Lasers wird ein Raumtemperaturlasersystem kaum unter die Hälfte dieses Preises kommen.

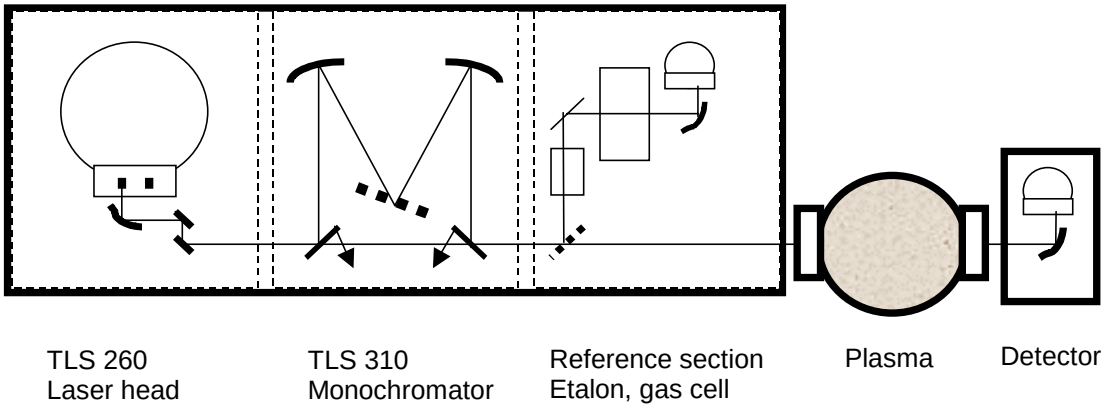

Abb. 5: Plasmadiagnostik mit MIR-Diodenlaser 3 – 25 µm.

Das Laserspektrometer leistet bei der Analyse von chemischen Prozessen in *Plasmen* und zur Messung der Partialdrücke von Molekülen und Ionen in den Plasmen wertvolle Hilfe. Der Aufbau eines solchen Spektrometers zur Entwicklung von *CVD-Anlagen der Halbleiterindustrie* ist in Abb. 5 dargestellt. Meist geht es bei diesen Anwendungen um die Messung von mehreren Molekülen bzw. Ionen. Man braucht also mehrere Laser, wobei jeder Laser auf einen Zielanalyten eingestellt wird. Da die Diodenlaser mehrere Moden gleichzeitig emittieren, dient ein nachgeschalteter Monochromator als Modenfilter.

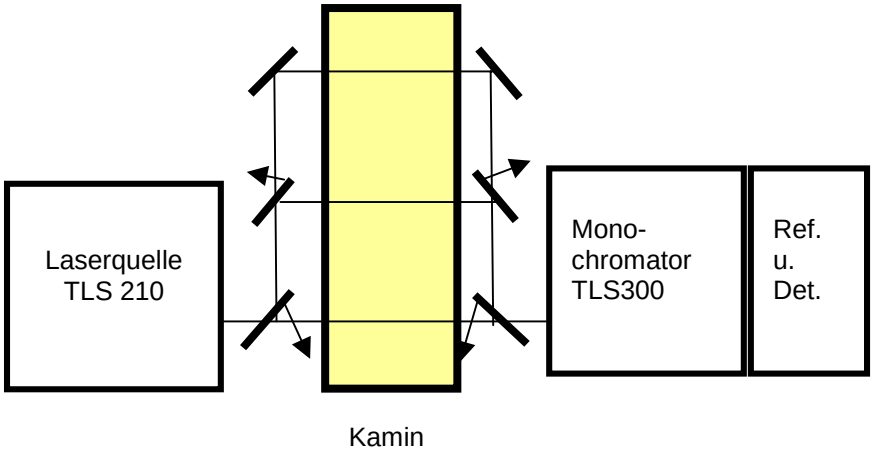

Abb. 6: *In-situ*-Gasüberwachung an drei Stellen.

Ein weiteres Beispiel ist die Bestimmung des Ammoniakgehaltes bei der Eindüsung von Urinstoff in *Verbrennungsöfen*. Damit die Anlage nicht verschlackt, sollte der Ammoniak möglichst gleichmäßig über den ganzen Verbrennungsquerschnitt zu Wasserdampf und N_2 reduziert werden. Abbildung 6 zeigt einen Aufbau zur Beobachtung der Verbrennung an 3 Stellen.

Die Bestimmung der Konzentration von (chlorierten) *Kohlenwasserstoffen in Wasser* wird in Zukunft bedeutender werden. Die Absorptionen liegen zwischen 900 und 1100 cm^{-1}. Erste Versuche wurden an der TU Wien am Institut für Analytische Chemie gefahren. Die Empfindlichkeit liegt hier im ppb-Bereich. Man kann zwischen Silberhalogenid- oder Chalcogenidfasern wählen, wobei die Chalcogenidfasern vom Sichtbaren bis ca. 9 µm und die Halogenidfasern bis über 20 µm transparent sind.

2.1.2 Beobachtung schneller Vorgänge

Molekülreaktionen in Verbrennungs- oder Katalysevorgängen werden online untersucht. Man beobachtet die Kinetik verschiedener Molekülkomponenten, kann auch Temperaturen online messen. Im obigen Beispiel (Abb. 4) mit dem CO-Spektrum in der Schockwelle rührt die linke Absorptionslinie von einem höheren Übergang, der erst durch die Boltzmann-Besetzung bei höheren Temperaturen angeregt wird. Im Verlauf der Schockwelle erhöht sich die Temperatur. Sie kann aus dem Verhältnis beider Linien abgelesen werden.

3. Ausblick in die Zukunft

Es wird nicht mehr lange dauern, bis anwendungstaugliche Raumtemperatur-Diodenlaser zur Verfügung stehen. Hauptaugenmerk wird dem künftigen Betrieb bei Raumtemperatur gewidmet. Auch Standard-Bleisalz-Diodenlaser wurden schon bei 60 °C betrieben, allerdings mit einer Pulslänge von nur 10 nsec. Die Spitzenleistung betrug beachtliche 80 mW. (Märzausgabe 99 von Laser Components). Der Betrieb bei Raumtemperatur ist für alle Anwendungen ein Vorteil, vor allem auch in Kombination mit MIR-Fasern.

Stellt man an künftige Raumtemperatur-Diodenlaser spektroskopische Qualitätsanforderungen, dann werden sie danach beurteilt werden, wie aufwendig deren Abstimmung über Absorptionslinien zu betreiben sein wird. Welche Mühe hat man bei der Temperatureinstellung, welche bei der Konstanthaltung der Temperatur und welche bei der kontinuierlichen Frequenzabstimmung? Wie zuverlässig wird der Dauerstrichbetrieb sein? Jedenfalls steht fest, daß bei der heutigen Wiederholbarkeit von Diodenlaserqualitäten, die durch die Technik der Molekularstrahl-Aufdampfanlagen gewährleistet wird, das einmal erfolgreiche Exemplar mit derselben Qualität und mit denselben spektroskopischen Eigenschaften in hoher Stückzahl zuverlässig wieder hergestellt werden kann.

Zum Abschluß wird ein Spektrum von Methan gezeigt, das mit einem Laser der Gruppe von C. Alibert am CNRS in Montpellier gefahren wurde. Es spricht für sich.

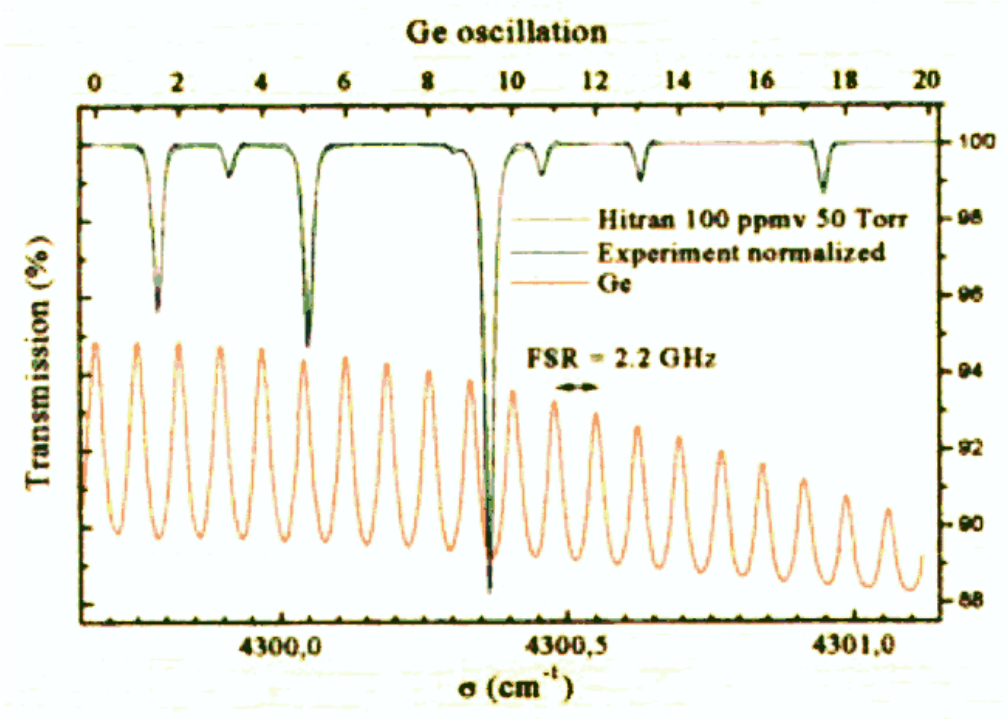

Abb. 7: Spektrum von Methan, gemessen mit einer 2,3 µm-GaInAsSb-Laserdiode des CNRS Montpellier bei 20 °C — perfekte Überlappung von Meßresultat und theoretischer Berechnung nach HITRAN.

In diesem Konferenzband sind eine Reihe von Vorträgen über neueste Laserentwicklungen zu finden. Sie werden hier nicht eigens aufgeführt.

Alleine durch die Möglichkeit des Raumtemperaturbetriebs werden sich neben den anspruchsvollen spektroskopischen Anwendungen eine Reihe von einfacheren industriellen Einsatzgebieten finden, die einem Spektroskopiker wie mir heute noch verborgen sind.

Fabrication of Highly Efficient Mid-Infrared Bragg Mirrors from IV-VI Semiconductors

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High reflectivity IV-VI semiconductor Bragg mirrors were grown by molecular beam epitaxy on BaF_2 (111) substrates. The λ/4 layer pairs consisted of a low refractive index $Pb_{1-x}Eu_xTe$ layer with x_{Eu} = 6 % and a higher index pseudoalloy $PbTe/Pb_{1-x}Eu_xTe$ superlattice with average x_{Eu} of 1 %. Mirrors with stop bands in the range between 4 and 6 µm were obtained with reflectivities as high as 99%.

1. Introduction

Due to their favorable electronic band structure [1], lead salt (IV-VI) lasers have long dominated the field of mid- and far infrared band gap lasers in the 3 - 30 µm region. The inherent wavelength tunability of these lasers have made them an ideal tool for high resolution infrared (IR) spectroscopy [2]. While these lasers are usually grown on lead salt substrates, (111) oriented BaF_2 has proven to be an excellent alternative as substrate material for lead salt heterostructures [3]. In comparison to lead salt substrates, BaF_2 exhibits a much higher thermal conductivity and mechanical hardness. This would allow significant improvements in heat dissipation during laser operation and facilitate device processing procedures. In the present work, we have explored the possibilities for molecular beam epitaxy (MBE) of highly efficient lead salt based mid-infrared Bragg mirror structures required for realization of vertical cavity surface emitting diode lasers in the 4 – 6 µm spectral region. Such devices, grown on readily available BaF_2 substrates, have great potentials for reducing threshold currents and increasing the operation temperatures of IV-VI lasers.

2. The Design of Bragg Mirrors

The basic design for high reflectivity Bragg interference mirrors is the stacking of two alternating layers with different refractive index and with a thickness equal to a quarter optical wavelength. The mirror characteristics are then governed by the refractive index contrast and the number of λ/4 pairs. In the present work we have focused on $Pb_{1-x}Eu_xTe$ of different composition for realization of MIR Bragg mirrors that are compatible with PbTe as active material. For $Pb_{1-x}Eu_xTe$ the refractive index below the fundamental absorption decreases with increasing Eu content and the energy gap E_g increases with dE_g/dx = 3.5 eV [4]. Using $Pb_{1-x}Eu_xTe$ layer pairs with alternating lower/higher Eu contents, Bragg mirrors without absorption of light emitted from a PbTe active region can be made. In order to keep the lattice mismatch as low as possible the Eu contents must be restricted to below about 10 %. Here, we have chosen a layer pair with Eu contents of 1 and 6 %. The 1 % layer was realized in the form of a short

period PbTe/$Pb_{1-x}Eu_xTe$ (x = 6 %) superlattice pseudoalloy with 50 Å period and thickness ratio of 5:1.

For the mirror design, the optical properties of the individual layers were determined by FTIR transmission measurements of a thick $Pb_{0.94}Eu_{0.06}Te$ reference layer and a 3 µm pseudoalloy superlattice.

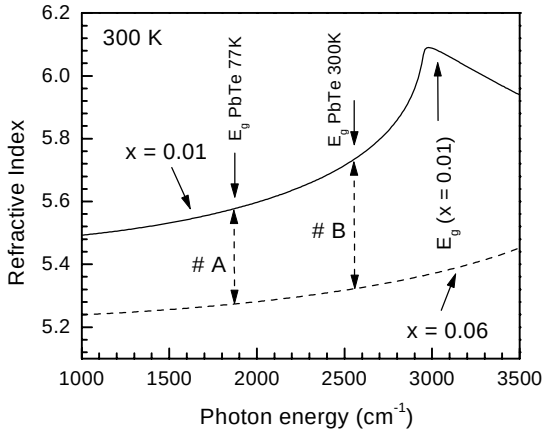
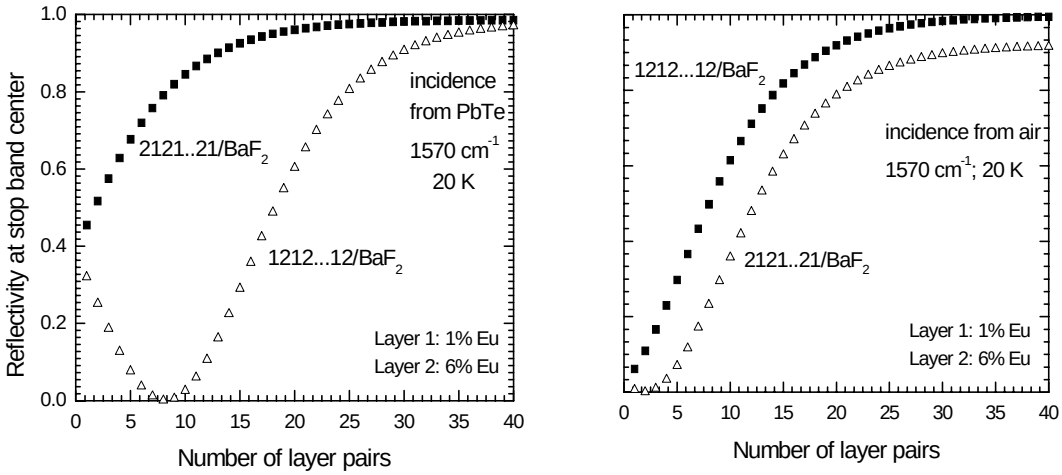


Fig. 1: Refractive index versus wavenumber at 300 K for two $Pb_{1-x}Eu_xTe$ reference layers (x_{Eu} = 1 and 6%). The arrows labeled #A and #B indicate the intended stop band positions for the Bragg mirror samples.



(a) (b)

Fig. 2: Theoretical reflectivity at the stop band center (1570 cm^{-1}) as a function of the number of λ/4 pairs for Bragg mirrors of $Pb_{1-x}Eu_xTe$ layers. (a) for incidence of the light from PbTe as active region, (b) incidence of light from air. The full and open symbols correspond to the different layering sequence where "2" corresponds to 6% Eu, and "1" to 1% Eu.

The optical constants (absorption constant α(ω) and refractive index n(ω)) were derived from the fit of the transmission spectra using a method described in Ref. [4]. As shown

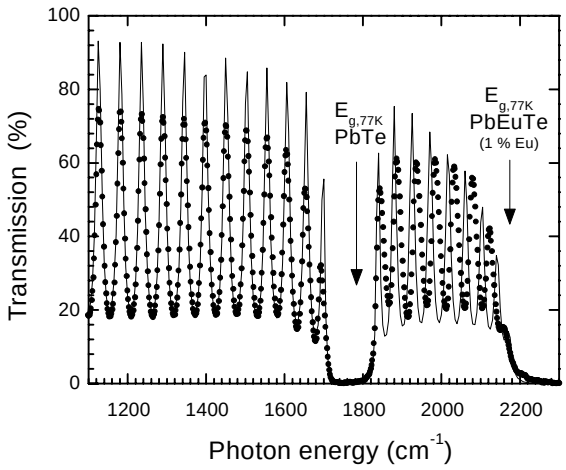
in Fig. 1, below E_g, the refractive index is determined by a constant dielectric background ε_∞ and, close to E_g, by the Kramers-Kronig contribution due to the changing absorption constant. The refractive index contrast therefore varies significantly with ω and is largest close to the band gap of the 1 % pseudoalloy layer.

For the mirror design we calculated the reflectivity of various mirror structures using the transfer matrix method and the experimental $\alpha(\omega)$ and $n(\omega)$ values as input parameters. As shown in Fig. 2, we find that for incidence of light from an optically denser medium (e.g. PbTe) 18 mirror pairs are required to achieve a reflectivity of 95 % and 28 pairs for R above 98 % at a wavelength of 5 µm. For incidence of light from air, due to the additional phase shift, the stacking sequence of the mirror pair has to be reversed.

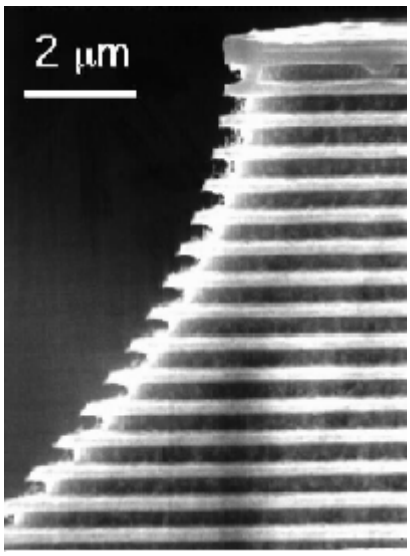
3. Results

The PbTe/$Pb_{1-x}Eu_xTe$ multilayers were deposited on cleaved BaF_2 (111) by molecular beam epitaxy. The ternary composition was determined by the PbTe to Eu beam flux ratio, and an excess Te_2 flux was used to retain the correct stoichiometry of the ternary. All flux rates were calibrated with a quartz crystal microbalance that could be moved into the substrate position. To minimize the growth time for the thick multilayer stacks, growth rates of about 2 µm/h were used.

In the following we show the results for a Bragg mirror designed to match the 77 K PbTe band gap (217 meV or 1750 cm^{-1}). The number of $\lambda/4$ pairs was 32. From Fig. 1, the refractive index contrast is 6 %, which is comparable to that for Bragg mirrors of III-V materials [5].



(a)



(b)

Fig. 3: (a) Measured (dots) and calculated (full line) transmission spectra for a 32 pairs Bragg mirror at 77 K with a stop band at ν_m = 1740 cm^{-1} (emission wavenumber of PbTe at 77 K), (b) Cross sectional scanning electron micrograph of a 20 pair Bragg mirror mesa structure. The cleavage edge was selectively etched to reveal the layers with different Eu composition.

Due to the pseudoalloy superlattices the required total number of individual layers is 3230 and the total thickness of the Bragg mirror is 16 µm. The sequence of the λ/4 pairs, starting with the 6 % $Pb_{1-x}Eu_xTe$ on BaF_2, was chosen to yield a high reflectivity for incidence of the light from air. The structural properties of the Bragg mirrors were determined by high resolution x-ray diffraction and scanning electron microscopy (SEM). The right hand side of Fig. 3 shows a cross sectional SEM micrograph of a 20 pair Bragg mirror sample with mesa structure, demonstrating the high lateral homogeneity and smooth interface structure of the samples. The cleavage edge was selectively etched to reveal the λ/4 layers with different Eu composition using a CH_4/H_2 plasma etch. The dark layers correspond to the λ/4 layers with the lower average Eu content, but the short period superlattice structure of this pseudoalloy layer can be resolved only by x-ray diffraction.

The FTIR transmission spectra of the 32 pair Bragg mirror sample measured at 77 K is shown in Fig. 3 (a). The main features are (1) the Fabry-Perot interference fringes due to the multiple reflections at the sample surface and the layer/BaF_2 interface, (2) the stop band of low transmittance of the Bragg mirror at ν_m = 1740 cm^{-1}, and (3) the high frequency cut off at around 2150 cm^{-1} due to the absorption edge of the 1 % $Pb_{1-x}Eu_xTe$ pseudo-alloy. The spacing of the fringes corresponds to the inverse optical thickness of the multilayer stack. The large refractive index jump at the BaF_2 interface also enhances the Bragg reflectivity of the samples. The transmission in the stop band region is below 0.5 %, which indicates a mirror reflectivity of better than 99 % (negligible absorption losses in the stop band region). Bragg mirrors with 20 λ/4 pairs typically exhibit a larger stop band transmission with corresponding reflectivity of about 93 %. Both values agree very well with our calculations. In spite of the large total thicknesses and large number of layers we have obtained excellent control and reproducibility of the layer thicknesses and composition. This opens promising perspectives for fabrication and applications of IV-VI mid-infrared resonant cavity light emitting diodes and vertical cavity surface emitting laser devices.

Acknowledgments

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Wavelength Adjustable Surface Emitting Single Mode Laser Diodes with Contradirectional Surface Mode Coupling

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Single-mode surface emission has been achieved from visible red GaInP/AlGaInP laser diodes by applying the contradirectional surface mode coupling technique. The emission wavelength (≈ 679.5 nm) of the laser structures was adjusted (decreased) in steps of 0.2 nm in an interval of 1.5 nm by reducing the thickness of the waveguide on top of the laser diode. The laser diodes emitted via the surface with a beam divergence of 0.10° and showed single-mode emission both in AC as well as in DC operation with a minimum spectral linewidth of 0.09 nm. The highest sidemode suppression achieved in DC operation was 26 dB.

1. Introduction

Semiconductor laser diodes in the visible regime are very suitable to be employed as powerful emitters in optical short-range data transmission (the attenuation minimum of *polymethylmethacrylate* (PMMA) fibers lies near 650 nm) and as light sources in the next generation of optical disk drives with their ability to read and write highly condensed optical information. The field of applications is widely spread, including spectroscopy, displays and optical sensing. Several red laser-diode-configurations have been successfully realized so far by using $Ga_xIn_{1-x}P/(Al_yGa_{1-y})_{0.5}In_{0.5}P$ sample structures. Excellent laser emission with low threshold current and high output power in the wavelength range between 620 and 690 nm has been reported.

Improvement of the emission characteristics and flexibility of the emission wavelength is desirable for advanced technical usage. If one achieves laser diodes with several single-mode emission spectra near the attenuation minimum of the optical fiber, the transmission bit rate of communication systems can be increased significantly by *dense wavelength division multiplexing* (DWDM) as the heart of *multiwavelength optical networking* (MONET). If surface emission (emission vertically to the epitaxially grown layers) is accomplished, the beam divergence is decreased essentially due to the expanded outcoupling window. Surface emission also eases the fabrication of two-dimensional arrays and the integration with the driving circuit on the same wafer.

Several concepts for obtaining single-mode surface emission have been presented by using second-order grating *distributed feedback* DFB lasers. They use the incorporation of a phase-shifting film [1], preferential current pumping [2], the effect of chirping the grating structure [3] or a complex-coupled grating [4]. There is no beam steering effect due to wavelength and temperature variations, since the beam direction is fixed by the DFB grating structure. Wavelength shift in DFB laser arrays is achieved by changing

the grating period of the individual elements requiring a very precise definition of the grating period to achieve a well defined emission wavelength. But there have been no papers reporting about the realization of these concepts in the red wavelength regime. In contrast the red *vertical cavity surface emitting laser* (VCSEL) diodes [5], [6], with which large-signal modulation of 1.5 Gb/s has been demonstrated. A wavelength shift can be achieved by generating a thickness gradient across the wafer during epitaxial growth [7].

2. Methods

We have developed a method to achieve single-mode surface emission from horizontal cavity laser diodes, which is based on *surface mode coupling* (SMC). The laser diode characteristics (wavelength, emission-angle) can be adjusted after the processing as a laser diode by changing only the surface parameters (waveguide's optical thickness). This leads to a straight way of creating multi wavelength laser diode arrays [8]. As SMC laser diodes can be fabricated by using the established technique of the conventional stripe-contact laser the complex fabrication process of VCSEL structures and of DFB lasers is avoided. The principle of these laser diodes is based on a coupling mechanism between the laser mode and the surface mode which exists in a semitransparent metal/dielectricum waveguide structure on top of the laser diode. Phase matching of the laser mode and the surface mode is achieved by a surface relief grating in the laser diode. The grating causes radiation losses of the laser mode, which are reduced significantly only in a narrow spectral range by the excitation and feed back process of the surface mode. The effective gain mechanism of this resonance leads to single mode emission. Recently we have shown that the SMC technique with codirectional (the laser mode and the surface mode are propagating in the same direction) coupling can be applied to GaAs/AlGaAs and to GaInP/AlGaInP laser diodes to achieve both a single-mode emission as well as a surface emission with very narrow beam divergence [9], [10]. The radiation and the longitudinal mode characteristics of the waveguide grating structures have been investigated numerically with an in-depth analysis based on the Floquet-Bloch theory. The numerical analysis shows that in case of contradirectional (the laser mode and the surface mode are counterpropagating) coupling between the laser mode and the surface mode the sidemode suppression of the emission wavelength is increased compared to the codirectional coupling mechanism due to a narrower resonance. In Fig. 1 the waveguide loss with co- and contradirectional surface mode coupling is shown. In case of contradirectional coupling the depth of the resonance increases with the gain. The contradirectional surface mode coupling concept has now been realized for the first time.

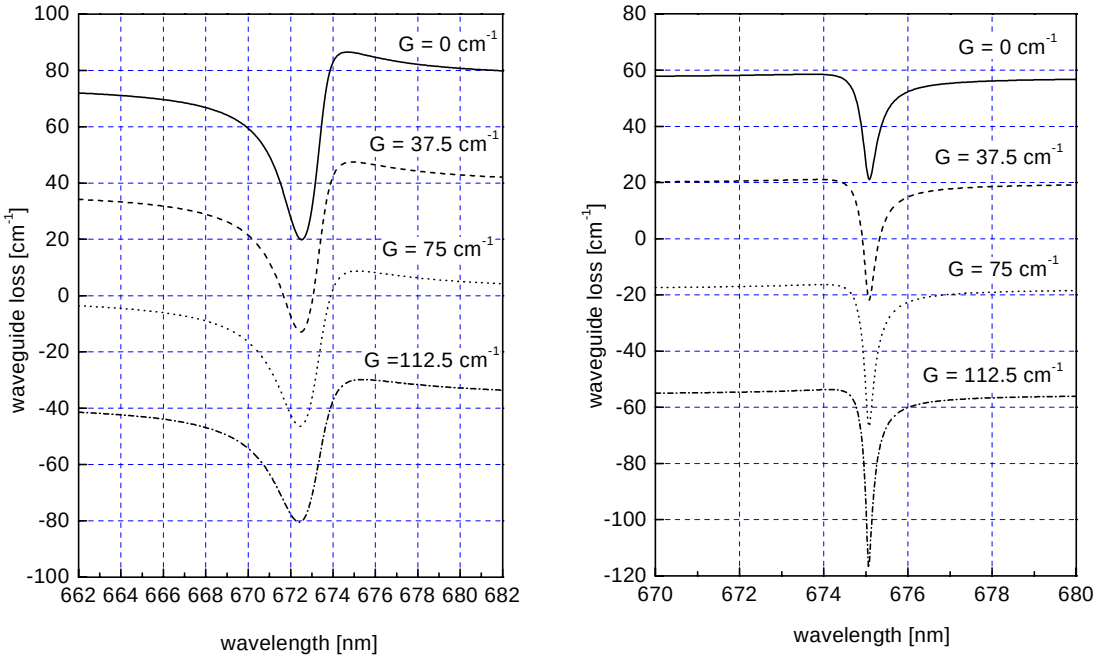
The physical background of the SMC-concept with surface emission and with contradirectional coupling is the following: the laser light propagating in the active region is exciting a transverse electrically polarized (TE_0) surface mode in a waveguide structure on the top of the laser diode through a 2^{nd} order grating coupling. Therefore the phase matching condition

$$\beta_{laser} - 2 \times k_g = \beta_{TEo} + \delta \qquad (1)$$

has to be satisfied. β_{laser} is the propagation constant of the laser, $k_g = 2\pi/\Lambda$ the grating vector (Λ is the grating period), β_{TEo} the propagation constant of the TE_0-surface mode and δ is the phase mismatch. The surface mode couples both into the vacuum light cone

resulting in surface emission and back to the active region leading to a gain mechanism and thus to single-mode emission. β_{TEo} can be "tuned" by changing the thickness of the surface waveguide. With β_{TEo} also β_{laser} and the emission wavelength of the laser diode is adjusted. The angle α of surface radiation is governed by the emission condition

$$\beta_{TEo} - k_g = \beta_{light} \times \sin \alpha \qquad (2).$$



(a) (b)

Fig. 1: Waveguide loss with codirectional (a) and contradirectional (b) surface mode coupling. In case (b) the numerical analysis shows a narrower resonance and the depth of the resonance increases with the gain (G).

3. Materials

The devices realized in this work are double-quantumwell $Ga_xIn_{1-x}P/(Al_yGa_{1-y})_{0.5}In_{0.5}P$ laser diodes grown by low-pressure metallorganic vapor-phase-epitaxy (MOVPE). Se-doped (n-doped) GaAs and $Ga_{0.51}In_{0.49}P$ buffer layers, followed by a Se-doped $(Al_{0.66}Ga_{0.34})_{0.5}In_{0.5}P$ cladding layer (1000 nm) and an undoped $(Al_{0.27}Ga_{0.73})_{0.5}In_{0.5}P$ waveguide layer (65 nm) are grown successively on a n-GaAs substrate, which is tilted 6° off towards the [111]-plane. Two compressively strained $Ga_{0.4}In_{0.6}P$ quantum wells (2×10 nm) with an $(Al_{0.27}Ga_{0.73})_{0.5}In_{0.5}P$ barrier (4 nm) form the active region. Next are a $(Al_{0.27}Ga_{0.73})_{0.5}In_{0.5}P$ waveguide layer (55 nm), a Zn-doped $(Al_{0.60}Ga_{0.40})_{0.5}In_{0.5}P$ cladding layer (400 nm), a Zn-doped $Ga_{0.51}In_{0.49}P$ layer (30 nm) and finally a Zn-doped GaAs cap layer (20 nm). Asymmetric cladding layers (by the aspect of thickness and refractive index) are designed to shift the electric field distribution of the laser mode towards the surface to achieve a sufficient coupling between the laser light and the TE_0 surface-mode.

The second-order grating (duty cycle 0.67) for surface mode coupling is defined by holographic exposure of a spin-coated photoresist (Hoechst AZ 5214) on the p-side of the laser structure. The pattern is etched into the top layers by ion milling (period Λ =

270 nm, height H = 100 nm). The evaporation of semitransparent Au/Zn/Au metal stripes (thickness 5 nm/5 nm/20 nm) with a width of 12.4 µm defines the stripe contacts of the lasers. Ti/Au contact pads (50 nm/250 nm), which overlap the laser stripe contact by 3.7 µm from both sides leaving a 5 µm wide window in the center of the laser stripe contact, are evaporated on a polymid isolation in between the single stripe contacts. Next the laser stripe is coated with two dielectric layers (~150 nm SiO_x ($\bar{n} = 1.5$) below ~250 nm SiN_x ($\bar{n} = 1.9$)) forming a slab waveguide on the top of the laser diode, which supports the TE_0-surface-mode. The combination of low-index and high-index dielectric is utilized in order to avoid excessive leakage losses into the high-index substrate. Finally, the laser bars are cleaved to a length between 350 µm and 500 µm and mounted on a Peltier element.

4. Results

The SMC laser diodes showed a threshold current density (j_{th}) of 1 kA/cm^2 at a temperature of 10°C in pulsed driven (AC) and at –5°C in continuos wave (DC) operation. The series resistance of the laser diodes was near 9 Ω.

The farfield pattern of the laser diodes was measured by scanning from one cleaved facet along the laser stripe-contact to the other facet. The surface emission was observed at ±50° with a beam divergence of 0.10°. The divergence in the perpendicular direction was 10°. The intensity emitted per solid angle into the single surface beam was three times larger than the emitted intensity per solid angle at the edges.

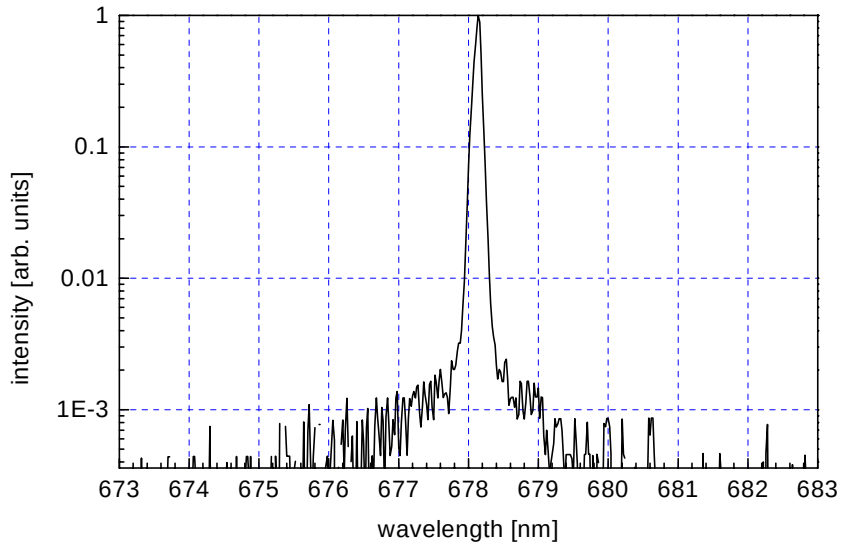


Fig. 2: Wavelength emission spectrum in DC operation. The laser diode emitted at 678.1 nm with a sidemode suppression of 26 dB.

The laser diodes showed a single mode emission in AC condition as well as in DC operation. A wavelength emission spectrum in DC operation is shown in Fig. 2 ($j_{th} \times 1.3$ = 1.3 kA/cm^2, -5°C). The laser diode emitted at 678.1 nm with a sidemode suppression of 26 dB. The minimum spectral linewidth achieved was 0.09 nm (spectrometer resolution 0.07 nm). The longitudinal mode separation of the Fabry-Perot cavity was measured to be 0.11 nm.

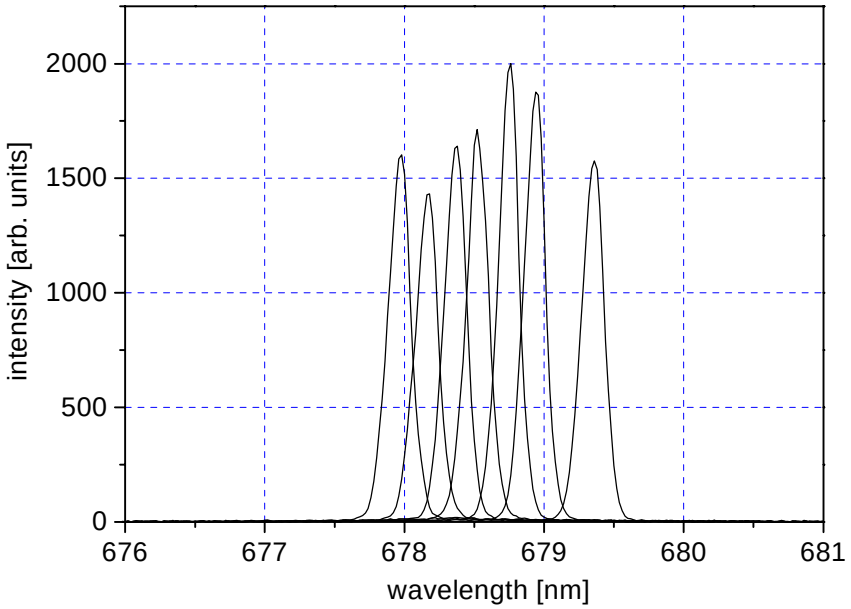


Fig. 3: The emission wavelength of the laser structures was adjusted (decreased) in steps of ≈0.2 nm in an interval of ≈679.5 nm to 678 nm by reducing the thickness of the waveguide on top of the laser diode.

As shown in Fig. 3 the emission wavelength of the laser structures was adjusted (decreased) in steps of ≈0.2 nm in an interval of ≈679.5 nm to 678 nm by reducing the thickness of the waveguide on top of the laser diode. (The surface waveguide was sequentially etched with HF 0.25%.) The temperature of the Peltier element was held constant at 25 °C. The resonance of the surface and the laser modes (and with it the emission wavelength of the laser diode) was shifted to the maximum of the laser gain spectrum (≈678.8 nm) and then to smaller wavelengths. This led to an increase and then decrease of the sidemode-suppression and of the light output intensity.

5. Conclusion

The contradirectional surface mode coupling concept has now been realized for the first time. Single-mode surface emission has been achieved from visible red GaInP/AlGaInP laser diodes by applying this technique. The emission wavelength (≈679.5 nm) of the laser structures was adjusted (decreased) in steps of 0.2 nm in an interval of 1.5 nm by reducing the thickness of the waveguide on top of the laser diode. The laser diodes emitted via the surface with a beam divergence of 0.10° and showed single-mode emission both in AC as well as in DC operation with a minimum spectral linewidth of 0.09 nm. The highest sidemode suppression achieved in DC operation was 26 dB.

Acknowledgements

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Self-Assembling Mn-Based Nanostructures

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We report on the fabrication, by means of molecular beam epitaxy, of Mn-based nanostructures on CdTe and on the possibility to obtain regular islands with different morphology during the subsequent deposition of semiconductor compounds. The processes are monitored in situ and in real time via reflectance difference spectroscopy.

1. Introduction

In the area of semiconductor materials, self-assembling nanostructures [1] are attracting considerable attention because of their potential applications in electronic and optoelectronic devices as e.g. single electron transistors and quantum dot lasers. CdTe-based semiconducting magnetic heterostructures (MH), both in the diluted semimagnetic (DMS) phase of $Cd_{1-x}Mn_xTe$ [2] and in the digital (DMH) arrangement embedding MnTe magnetic layers [3], [4], offer the unique opportunity of having electronic band structures which can considerably be tuned by the application of magnetic fields of moderate intensity [5], [6]. In addition, the introduction of magnetic clusters in a semiconducting matrix opens new perspectives for applications in spin-dependent switching devices and in storage technology [7]. Puzzling morphologies of self-assembled islands, depending on the growth conditions and due to strain and stress effects [8], [9] and surface diffusion processes, could represent, when properly controlled, interesting new systems for electronic confinement in low dimensions. In addition, with the presence of magnetic elements, they could allow for the study of non-collinear magnetic structures' formation [10] and of strain effects on magnetic phases. In the present work, we essentially focus on the formation of pure Mn nanocrystallites on CdTe and then on the possibility to obtain regular islands with different morphology during the subsequent deposition of semiconductor compounds.

2. Experimental

All structures are fabricated by molecular beam epitaxy (MBE) on GaAs(001)-oriented substrates: a 0.5 µm thick CdTe buffer layer is at first deposited in excess of Te at a substrate temperature of 280 °C. The subsequent heteroepitaxy leading to island formation is carried out on the 2x1 Te-terminated CdTe(001)-oriented surface, keeping the substrate temperature constant. The MBE system is equipped with a reflection high energy electron diffraction (RHEED) apparatus with 20 keV operating voltage, suitable to follow changes in the surface reconstruction during the growth process.

With the aim of making the various formation stages reproducible, we follow the deposition phases via *in-situ* reflectance difference spectroscopy (RDS): this real-time tech-

nique allows to measure the difference between normal-incidence reflectances for light polarized along the two principal axes of the surface and it can be considered as a normal incidence ellipsometry, sensitive to surface and interface anisotropies [11], [12]. For the (001)-oriented surface we are interested in, symmetry considerations show that the optical eigenstates are $[\bar{1}10]$ and [110], thus the complex reflectance coefficients for light polarized along these axes are $r_{\bar{1}10}$ and r_{110}. The parameter measured is the relative difference: $\Delta r/r=(r_{\bar{1}10}-r_{110})/[(r_{\bar{1}10}+r_{110})/2]$. Our *in-situ* RDS system is similar to the one reported in [13]. In our study, we consider the real-time kinetic mode of RDS, where $\Delta r/r$ is monitored as a function of time. All data are acquired at the fixed energy of 3.26 eV, corresponding to the E_1 electronic transition for CdTe at the considered temperature.

By following the growth process simultaneously by means of RDS in kinetic mode and RHEED, we are able to detect the significant phases of islands' formation and to obtain the reproducibility of the structures. After major changes in RDS kinetics (Fig.1), the growth process is interrupted and the surface morphology examined *ex-situ* via atomic force microscopy (AFM).

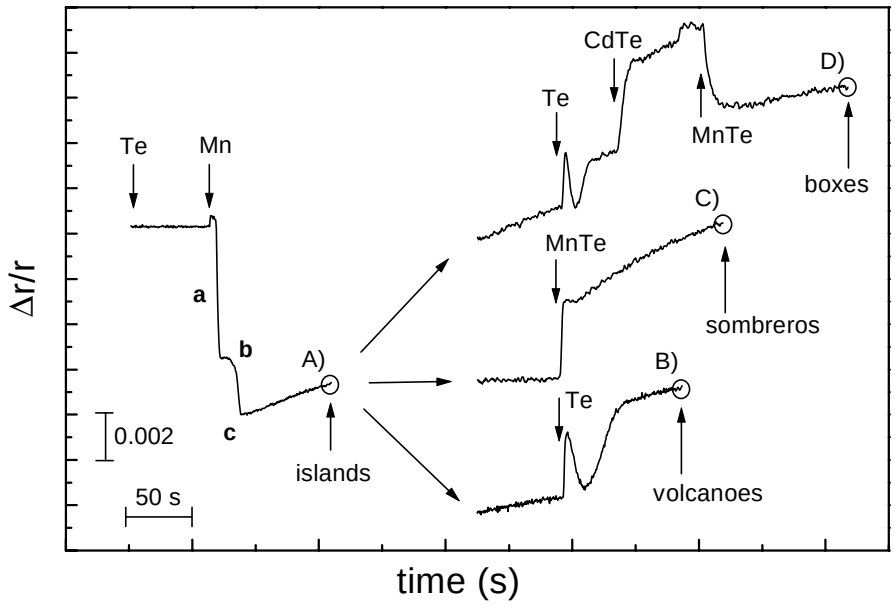

Fig. 1: Reflectance difference spectroscopy spectra in kinetic mode

The first step in our experiment is the deposition of pure Mn with a beam equivalent pressure of $0.3\text{x}10^{-8}$ Torr, on the Te-terminated CdTe(001) surface. As soon as the Mn nucleation starts, the RDS signal shows (region **a** in Fig.1(A)) an abrupt drop during the time corresponding to the growth of the first monolayer (ML). Successively (region **b** in Fig.1(A)), for the next two Mn MLs, the signal keeps constant, suggesting the formation of a wetting layer. After an additional steep decrease of the signal during the deposition of the fourth ML, we observe (point **c** Fig.1(A)) a sudden rise of the RDS signal and, simultaneously, a change in the RHEED pattern (till this moment stable at the 2x1 reconstruction typical for the Te-terminated CdTe surface): regular spots appear between the streaky features of the original reconstruction. From these facts we can infer that Mn has been deposited in crystalline phase and with a lattice constant greater (smaller in the

reciprocal crystallographic space mapped by RHEED) than CdTe. The surface morphology studied at this stage by means of AFM shows an arrangement of well defined islands like the one shown in Fig.2(A). For coverages from 6 to 15 MLs, we could distinguish a bimodal size distribution of nanocrystals with the smaller crystallites growing till a maximum of 20 nm in height and 150 nm in diameter and the bigger islands showing a narrow size distribution and an average height of 50 nm and average diameter of 200 nm. The average density on the surface is of 10 μm^{-2}. When we follow the same procedure described before, but instead of ending the growth after the formation of Mn islands, we proceed depositing Te, the evolution of RHEED pattern results in spots aligned along the 2x1 reconstruction with a distance corresponding to the lattice constant of MnTe. In addition, as soon as the Te deposition starts, the RDS signal produces an oscillation (Fig.1(B)) before saturating. By analyzing real ($\Delta r/r$) versus imaginary ($\Delta\theta$) part of the difference in anisotropy for the interval relative to the oscillation in $\Delta r/r$, we obtain a spiral-like trend (not shown), which is explained as the developing of a buried interface [14], in our case ascribed to diffusion of Te in Mn. AFM studies of the surface morphology at this stage, show 'volcanoes' (Fig.2(B)) with an average base diameter of 200 nm, a height of 20 nm, and cone-shaped craters with a maximum diameter of 50 nm. In this context, the effect can be explained in terms of strain induced by the presence of the Mn islands and having as a consequence the migration of adatoms along the side-walls of the crystallites and concomitant lack of dangling bounds in correspondence of the upper most region of Mn nanocrystals. We underline that the anti-dot-like shaped craters seem to be, because of morphology and size, promising candidates as hosts for 0-dimensional quantum structures.

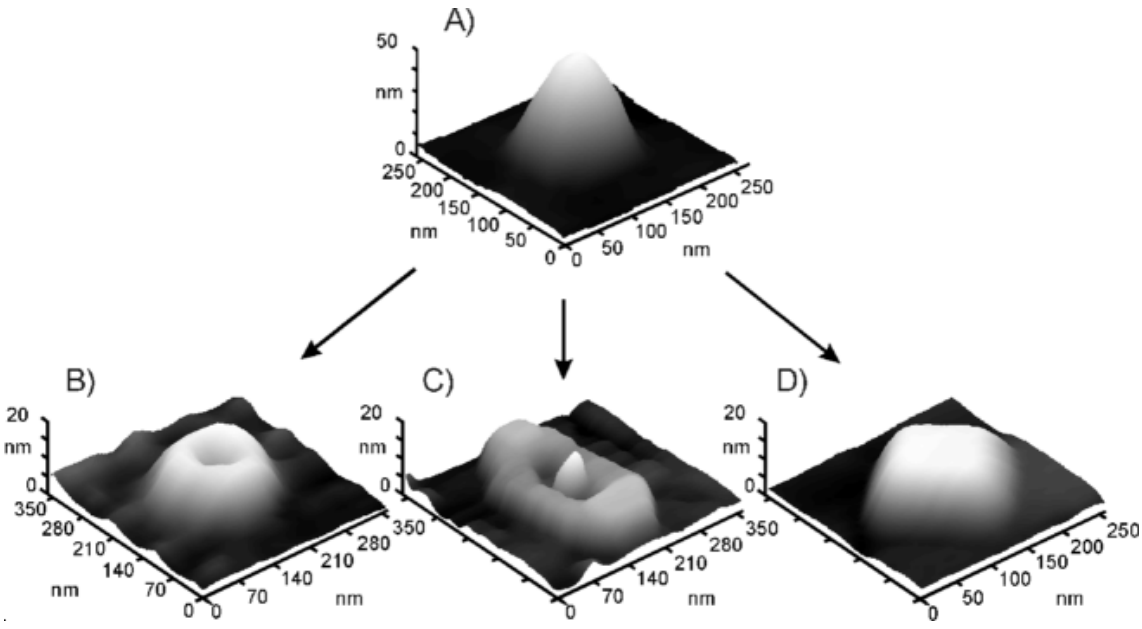

Fig. 2**:** AFM topographies.

In our search for different well controlled morphologies, we deposit 8 MLs of MnTe instead of pure Te on the precursor Mn crystallites (Fig.1(C)). After a Mn island is nucleated, the strain ε caused in the island by lattice mismatch is partially relaxed at the price of inducing an extra strain in the substrate and increasing the strain in the wetting layer near the crystallite edge. Therefore, adatoms deposited on the wetted surface will

have to overcome an energy barrier $\Delta\mu_s$ before they can attach to the island [15]. During successive growth, the evolution of the morphology is also influenced kinetically by surface stress, since adatoms tend to diffuse on the surface away from sites with high strain [16]. The strain concentration at the island edge increases monotonically with the island size; when it exceeds a critical value, the free energy for atoms to occupy a position at the island edge may become higher than that for atoms to occupy a crystallographically unusual, but less strained site [15]. These considerations explain why the growth of MnTe is hampered at the edges of the crystallites and tends to develop far from the borders of precursor Mn islands and generate the 'sombrero'-like features shown in Fig.2(C).

Finally, after the deposition of Te and successive 15 MLs of CdTe followed by 8 MLs of MnTe on the precursor Mn island (Fig.1(D)), we obtain a quasi-periodic arrangement of equally shaped 'boxes' with very regular squared bases of 200 nm x 200 nm and height of 20 nm (Fig.2(D)). Despite the presence of these features on the surface, the RHEED pattern appears streaky 2x1, due to the high density and the ML-scale flatness of the islands' top. The structures show the tendency to arrange along the [100] and [010] crystallographic directions, as predicted [17] for a stable array of islands on a (001)-oriented surface. Thermodynamic calculations have shown that after an island is nucleated the system free energy decreases monotonically with increasing island size [10]. Thus, a free energy minimum at a certain size is required in order to explain why observed islands' sizes tend to be so uniform. One should bear in mind not only the energetics, but also the kinetics, which implies that the islands' height grows slowly compared to the basis and may be treated as roughly constant. The kinetics can be incorporated by minimizing the total island energy with respect to width and length of the crystallite keeping the height constant. The result is that, in thermodynamic limit, with high density of islands, they should grow until each nanocrystal is square-based. This morphology represents the optimal trade-off between surface energy and strain. In our case the 'boxes', after reaching the squared-basis configuration, do not undergo further ripening and shape and basis size keep constant. Additional growth of MnTe leads to an increase of the crystallite height.

3. Conclusions

In conclusion, we achieved the reproducibility of self-assembling Mn-based nanocrystals, by monitoring in real time the subsequent stages of the growth process. The extension to other material systems and growth techniques would be straightforward, the RDS being suitable for MBE as well as for non-ultra-high-vacuum systems like chemical vapor deposition (CVD) reactors.

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Analysis of Single-Mode Grating Coupled Twin Waveguide Laser Structures

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An analysis of semiconductor laser structures with adjustable single-mode emission based on a contradirectionally grating coupled twin-waveguide structure consisting of an ITO/low-index dielectric waveguide on top of a corrugated active laser waveguide is presented. At resonance between the laser mode and the surface mode the grating-coupled radiation losses show a sharp drop with a linewidth comparable to the Fabry-Perot-mode spacing of the laser cavity, thus preferring a single longitudinal mode. Intermodal discrimination of up to 20 cm^{-1} and moderate threshold gain of ~50 cm^{-1} can be obtained. Since the resonance wavelength depends on the optical thickness of the surface waveguide, a simple post-processing adjustment of the emission wavelength with a tuning range in excess of ~15 nm can be achieved.

1. Introduction

For the realization of highly integrated wavelength division multiplexing (WDM) transmitter devices monolithic laser diode arrays are considered as a compact choice due to their capability of simultaneous transmission of several channels into a single optical fiber, thus decreasing system size and costs. Efforts on multiwavelength laser diode arrays have focussed on DFB [1] and VCSEL laser arrays. Wavelength shift in DFB laser arrays is achieved by changing the grating period of the individual elements which, however, requires a very precise definition of the grating period to achieve a well defined emission wavelength. In VCSEL arrays the wavelength shift can be achieved by generating a thickness gradient across the wafer during epitaxial growth [2]. Recently a five wavelength laser diode array [3] has been reported which utilizes the surface mode emission (SME) technique [4]. This technique provides the advantage of a simple post-processing adjustment of the emission wavelength of the individual laser diodes by adapting the surface waveguide thickness on top of the structure. A drawback of the SME technique, however, is the relatively low side mode suppression of about 20 dB. The laser structures suggested in this paper combine both the simple post-processing wavelength adjustment of the SME technique and considerable intermodal discrimination.

2. Laser Structures

The laser structures under consideration are based on a GaAs/AlGaAs DH-Laser structure utilizing an InGaAs/GaAs-MQW active region (at λ = 980 nm) embedded in highly asymmetric cladding layers in order to shift the mode field pattern towards the surface. The n-type cladding layer on top of the GaAs-substrate (refractive index $\bar{n}$ = 3.523) is formed by $Al_{0.3}Ga_{0.7}As$ ($\bar{n}$ = 3.333, thickness 1200 nm). The active layer with a thickness of 250 nm ($\bar{n}$ = 3.523) is followed by a typically 300 nm thick p-$Al_{0.2}Ga_{0.8}As$ layer ($\bar{n}$ =3.393) and a p-GaAs top layer which is 250 nm thick. The top layer is corrugated

by a trapezoid shaped grating with the period Λ = 192 nm, duty cycle 0.5, slope angle of 70° and a height of 80 nm. The grating is covered with a 120 nm indium tin oxide (ITO, $\bar{n}$ =1.6 + 0.04*i*) film which is needed for current injection. The SWG is made of ~200-400 nm SiO_x ($\bar{n}$ = 1.5) below a ~300 nm SiN_x layer ($\bar{n}$ =1.9). This combination of high-index and low-index dielectric is utilized in order to avoid excessive leakage losses into the high-index substrate.

3. Waveguide Modes

Since the WGS is basically a twin waveguide structure, two modes — a laser mode "a" and a surface mode "b" with the propagation constants β_a and β_b, respectively — exist. The grating causes grating coupled radiation into the substrate thus creating additional losses. In case of surface mode resonance (SMR), i.e. when the phase matching condition $\beta_a - \beta_b \approx 2\pi/\Lambda$ is satisfied, contradirectional coupling between the mode "a" and "b" occurs. (Note that $\Re\beta_b < 0$ since mode "b" is counterpropagating.) This means that energy is transferred from the LWG to the SWG and in turn back again. This energy transfer is accompanied by a resonant decrease of the grating coupled radiation loss into the substrate for both modes. Another benefit of this coupling is the effective increase of gain which a wave travelling over a certain in the active LWG experiences, since power is coupled into the SWG where it is transferred into the opposite direction and in turn coupled back into the LWG where it is amplified again.

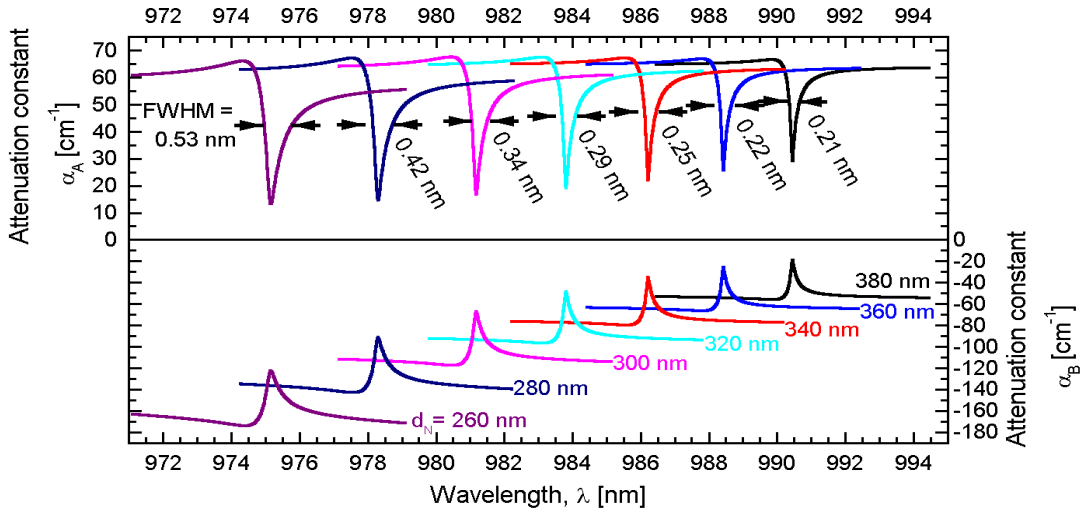

Fig. 1: Attenuation curves for a WGS with a 120 nm ITO/350 nm SiO/SiN SWG for different SiN thicknesses ranging from 260 to 380 nm. α_A and α_B are the attenuation constants of the laser mode and the surface mode, respectively.

The analysis used for the calculation of the waveguide properties follows the numerical approach presented in [5]. It is a coupled mode theory which is based on a rigorous Floquet-Bloch analysis of the grating waveguide problem yielding accurate results even for strong gratings. The governing equations relating the slowly varying amplitudes of the waves propagating in the LWG and the SWG $a(z)$ and $b(z)$, respectively, are obtained as $da/dz = (i\kappa_{11} + G)a + i\kappa_{12}\exp(-i\delta z)b$ and $db/dz = i\kappa_{21}\exp(i\delta z)a + i\kappa_{22}b$, where the coupling coefficients κ_{ij} (i, j = 1, 2) provide information about absorption loss, radiation

loss and coupling between mode “a” and “b”. The influence of gain is described by G; $\delta = \beta_a - \beta_b - 2\pi/\Lambda$ is the phase mismatch between modes “a” and “b”.

Figure 1 shows the (power) attenuation curves of a WGS with a 250 nm p-$Al_{0.2}Ga_{0.8}As$ layer and a 120 nm ITO/350 nm SiO/SiN SWG with SiN-layer thicknesses varying from 380 to 260 nm. Since the dispersion of the SWG depends on the SWG thickness the resonance wavelengths range from 990.4 to 975.2 nm. The linewidth of the SMR increases from 0.21 nm to 0.53 nm due to increasing leakage losses of the SWG. However, due to the stronger penetration of the SWG field into the grating region a moderate increase of the mutual coupling coefficient from 27 + 8.4i cm^{-1} to 45.1 + 21.3i cm^{-1} is observed.

4. Finite Length Resonators

The finite length resonators are formed by the WGS terminated by as cleaved facets located at $z = \pm L/2$ (cavity length L) with amplitude reflection coefficients $r_a = \sqrt{0.3}$ and $r_b = \sqrt{0.05}$ for the LWG and the SWG. The laser structures are basically Fabry-Perot (FP) cavities with an intrinsic narrow-band wavelength filter favoring to lase just one FP mode coinciding with the resonance wavelength. In order to obtain single mode operation two requirements must be met: 1) The linewidth of the SMR has to be comparable or yet better smaller than the FP mode spacing and 2) a proper matching of the SMR and the FP mode spectrum must be achieved. The former requirement is fulfilled since both the SMR and the FP mode spacing are in the sub-nm regime. The latter requirement, however, needs to be discussed in detail: An effective mode selection only occurs if one of the FP resonances is near the wavelength with minimum losses. If the wavelength of minimum loss is between two FP modes, single mode emission cannot be expected since both FP modes suffer almost equal losses. The relative position of the FP modes and the SMR, however, can be adjusted thermally since the FP modes shift with a rate of $\Delta\lambda_{FP}/\Delta T \approx \lambda/n_a \cdot \Delta n_a/\Delta T = 0.067\,\text{nm/K}$, whereas the SMR shifts more slowly ($\Delta\lambda_{res}/\Delta T \approx \lambda/(n_a + n_b)\cdot \Delta n_a/\Delta T = 0.045\,\text{nm/K}$). This is a consequence of the much smaller temperature dependence of the effective index of the SWG (n_b) than that one of the LWG (n_a). For a cavity length L= 600 µm a temperature deviation of 10 K shifts the FP mode spectrum from one optimum position with respect to the SMR to the next one. Thus in order to avoid mode hopping a temperature stabilization allowing maximum deviations of ~1 K is necessary.

Figure 2 shows the longitudinal mode spectrum of a laser structure (length 600 µm) with an ITO/SiO/SiN SWG (layer thicknesses 120, 350 and 300 nm; the p-$Al_{0.2}Ga_{0.8}As$ layer thickness is 300 nm). Additional losses of 10 cm^{-1} were assumed for both subwaveguides. The lowest threshold mode has a mode gain $2G$ =45.2 cm^{-1} and a threshold gain difference of about 14 cm^{-1} which is suitable for single mode operation with a side mode suppression of more than 30 dB. A clear resonant decrease of the power radiated into the substrate is observed whereas the power emitted via the facets peaks. However, due the resonant increase of optical power in the absorbing ITO layer, also the absorbed power peaks at the SMR.

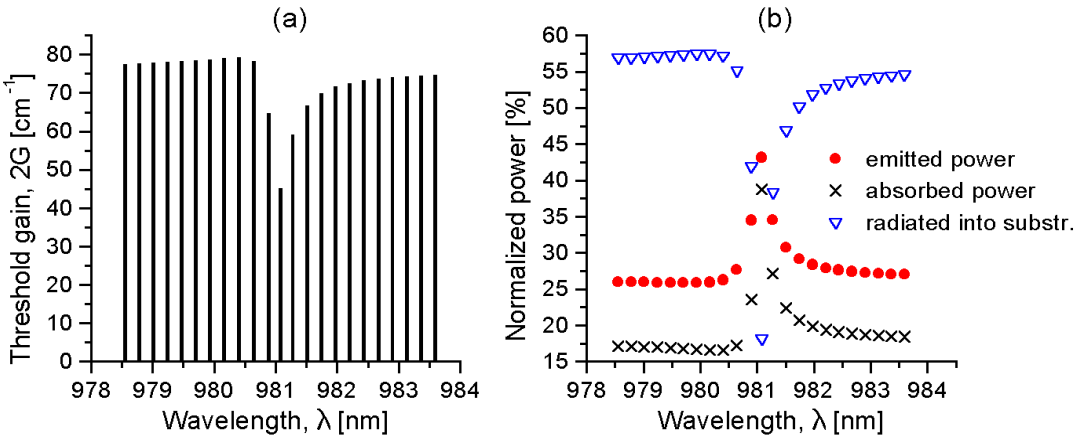

Fig. 2: Longitudinal mode spectrum (a) and normalized powers (b) for a 600 µm long device with an ITO/SiO/SiN SWG. The powers are normalized with respect to the stimulated emission power.

5. Conclusion

We have suggested a novel design for single-mode laser diodes with adjustable emission wavelength. The mode selection mechanism is based on a narrow-band suppression of radiation loss of an active/passive twin-waveguide structure. Intermodal discrimination can be as high as 20 cm^{-1} while maintaining relative low threshold gain (~50 cm^{-1}) and moderate differential output efficiency (~40 %). Simple and precise post-processing wavelength adjustment with a range in excess of ~15 nm is feasible, since changing the SWG thickness yields a shift of the SMR at a rate of $\Delta\lambda_{res}/\Delta d_{SWG} \approx 0.12$.

Acknowledgements

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Investigation of Local Ions Distributions in Polymer Based Light Emitting Cells

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Polymer based light emitting electrochemical cells have been analyzed by means of SIMS revealing a strongly inhomogeneous ions distribution that leads to an asymmetric behavior of such elements. This work shows that the separation of the ions already happens during the production of such cells.

1. Introduction

Light-emitting electrochemical cells (LECs) have a great potential for industrial applications due to their capability of blue color emission at low voltages. Such cells would be extremely cheap to produce and can also be designed to fill large scale areas. All in all those cells promise to be part of tomorrow's flat panel displays.

The typical behavior of the LECs is realized by adding an ionic salt to a conjugated polymer, often blended with a ionically conducting polymer to enhance the transport of the ions. For the cells investigated, m-LPPP (methyl substituted poly(para phenylene)) was used as semi-conducting polymer with PEO (Poly Ethylene Oxide) as ionic conductive and lithium trifluorsulfonate as ionic species, other set-ups for LEC's use lithium salt/crown ether complex as the solid electrolyte [1] or poly(1,4-phenylene-vinylene) (PPV) as polymer semiconductor [2]. This ionic species acts as counter ions for electrochemical doping during operation, where at the cathode the polymer is reduced (n-type doped) and on the anode oxidized (p-type doped) leaving a non doped region in-between. This doping is evidenced by absorption measurements of a LEC under operation [3]. The homogeneity of the polymer layer is most important for the quality of such devices, especially phase separation between the ionic conductive and the electronic conductive polymers strongly influences the performance of LEC's [4].

However, mLPPP based LECs show a different behavior than reported for LECs up to now, with ITO used as cathode. In forward direction with the ITO as anode the turn on voltages are significantly higher or no light emission can be observed [3]. We investigated the element distribution within the active layer by secondary ion mass spectroscopy (SIMS) depth profiling using both negative as well as positive secondary ions showing that already during the production of those cells the ionic species separate within the active layer thus pre-defining the direction in which those cells are to be operated.

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2. Experimental

The SIMS instrument used throughout those investigations was an enhanced CAMECA IMS 3f. The modifications refer mainly to the primary column to which a CAMECA Cs^+ fine focus ion source as well as a duoplasmatron for O_2^+ ions, extended lens systems and a digital raster generator have been added. The usage of a CAMECA Cs^+ Fine Focus ion source as well as O_2^+ duoplasmatron has been provided by the installation of a primary magnet. Furthermore the application of the primary magnet guarantees the purity of the primary ion species [5], [6].

As for the measurement of the local ions distribution in the LECs strongly electropositive species (Li^+ ions) as well as strongly electronegative species (F^- ions as tracer for the triflate ion) had to be detected to characterize the local ions distribution, the use of both primary ions was advisable. Thus, for each cell two measurements were necessary and the signals of the matrices (carbon for the polymer layer, indium for the ITO layer and aluminum or gold for the metallic top electrode, that could be observed in both measurements, were then used to fit the two measurements together resulting in a depth profile containing the information for both the lithium as well as the triflate distribution.

Within the scope of this work, Cs+ ions, accelerated to energies of 14.50 keV and focused to a spot diameter of some 10 µm resulting in a primary current of 15 nA have been used for the detection of negative secondary ions, the primary ion beam was projected onto an area of 350 x 350 µm in square with an analyzed area of 60 µm in diameter selected by the use of an aperture diaphragm. For the detection of positive secondary ions, O_2^+ primary ions accelerated to energies of 5.50 keV and focused to a spot diameter of some 10 µm resulting in a primary current of 500 nA have been used, the primary ion beam was projected onto an area of 250 x 250 µm in square with an analyzed area of 150 µm in diameter. Those conditions were chosen by trial in order to obtain optimum conditions for sputter removal rate, depth resolution and secondary ion yield.

The m-LPPP based LECs were prepared at the Institute for Solid State Physics, TU Graz, by L. Holzer. They were made by spincoating a cosolution of m-LPPP, PEO (molecular weight 5000 kDa) and $LiCF_3SO_3$, weight ratio 20:10:3 in cyclohexanone on an ITO coated glass substrate under argon atmosphere. The samples were annealed for half a day at 60 °C, and aluminum resp. gold was evaporated on top of the films under a pressure of about 10^{-6} Torr. This resulted in a 100 nm thick ITO base electrode, approximately 120 nm of polymer layer and 50 nm of metallic top electrode. Still, the actual thickness of the layers varied remarkably which resulted in short circuits on many of the pads as well as of course varying profile depths. Still this was no problem for the measurements as the criteria for the fitting of the depth profile was the thickness and position of the polymer layer, so the different depth profiles were stretched and shifted until the carbon distribution was in good agreement. To prevent the samples from oxidation and contamination under ambient air, they were operated and stored under argon atmosphere until they were transferred into the vacuum system of the SIMS instrument.

3. Results and Conclusion

Figure 1 shows a depth profile through a “standard” LEC system that has already been in use for some minutes. On the left hand (on top) the aluminum contact is situated, followed by the polymer layer and the ITO base electrode. Under operation, the ITO base electrode was set to negative potential. The relative thickness that can be observed

in the depth profile is not proportional to the actual thickness ratios in the samples due to differences in the sputter removal rates between the three layers; the polymer layer had the highest sputter removal rate. The profiles has been recorded until the interface to the glass substrate was reached where strong charging effects occurred. During measurement of the active layer the conductance was sufficient, so no charging effects could be observed. The profile broadness results mainly from the initial roughness of the samples and sputter induced effects.

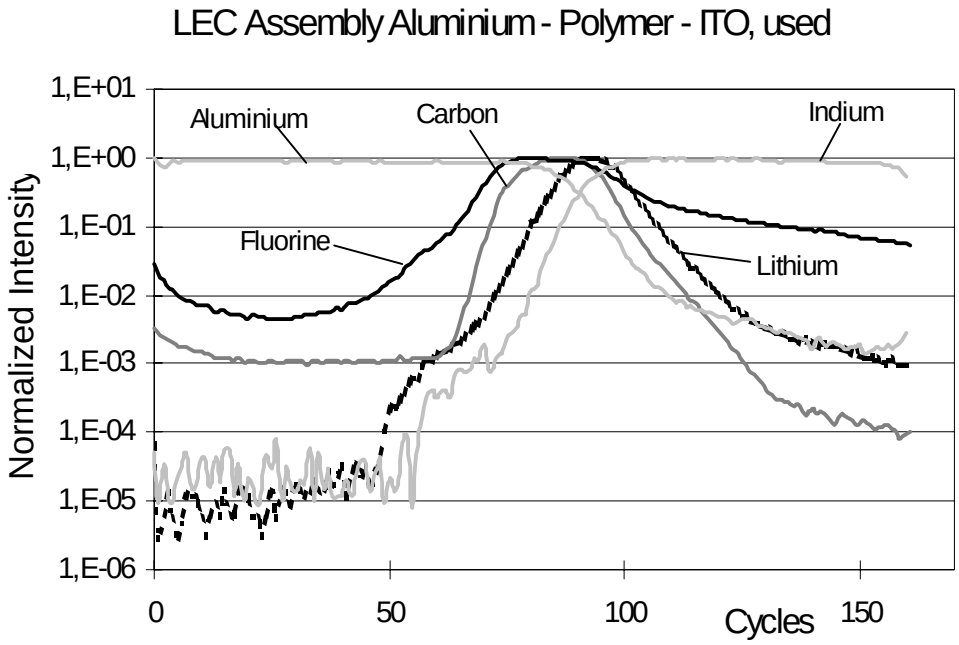

Fig. 1: Depth Profile through a used LEC.

One can clearly see that the ionic species have been separated under the influence of the applied electric field (some volts drop off over approximately 120 nm which results in an electric field of approximately $3 \cdot 10^7$ V/m) and that the lithium distribution is clearly shifted towards the interface ITO-polymer whereas the triflate distribution (represented by the fluorine ion) is shifted towards the interface aluminum – polymer. Especially remarkable, the fluorine and lithium distribution differ considerably from the carbon peak and they are of similar mass, so the observed shift of the peaks is most likely not an artifact of the sputter process. As no charging effects occurred, no effects of a local electric field from surface charging that would have driven the ions apart during measurement can be expected as it was reported for measurements on insulators [7], [8].

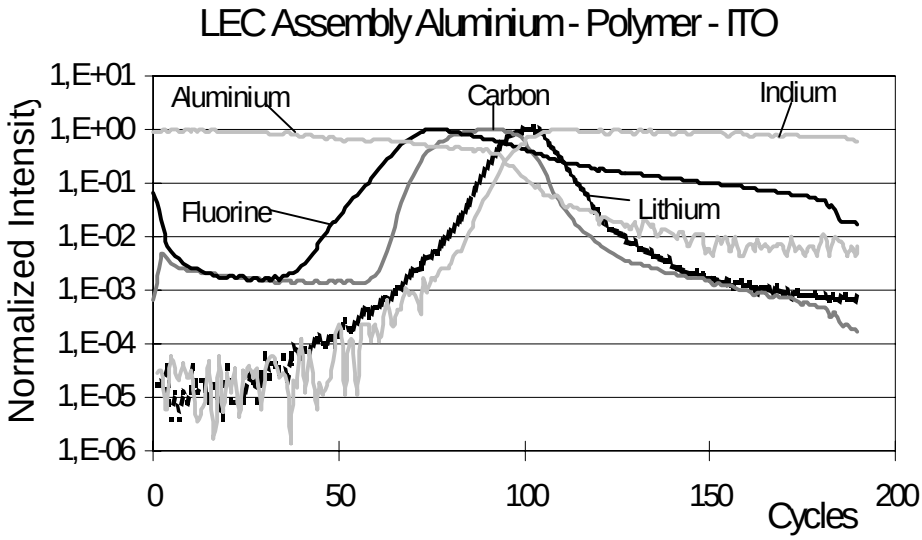

Fig. 2: Depth Profile through an unused LEC.

Figure 2 gives the depth profile for the identical LEC assembly, but this cell has not been used before so that one would expect the ions to be distributed homogeneously throughout the active layer, as no applied field could have driven them apart. But actually, the depth profile shows a separation of the ionic species, again lithium ions are enriched towards the interface polymer-ITO and the triflate ions at the opposite interface aluminum-polymer. This reveals, how the effect of an initial "polarity" of these devices comes up: as the ionic species separate already during production and the lithium ions enrich at the interface towards the ITO base electrode, the devices work properly with the ITO base electrode set to negative potential as many lithium ions are available for charge compensation. Reversing the polarity of this device would first afford to transport ions to the counter electrodes, and no light emission can be achieved. This explains the behavior of the devices, but still the question remains how this separation happens. For example different Fermi levels of the electrode materials build up an "inner" field: the energy difference of the Fermi levels of the two electrode materials is about 0.7 eV which could be the driving force for this process. when the two electrodes are in electric contact, the Fermi levels are equalized resulting in a built in field gradient within the polymer layer [9]. Further measurements on similar cells with other electrode materials resp. without top electrode attached showed that especially effects of solubility in the ITO electrode and fractional deposition of the components play an important role in the development of inhomogeneities on such cells [10].

It has been shown by depth profiling SIMS that within LEC's based on the system m-LPPP/PEO/$LiCF_3SO_3$ a significant separation of the ionic species happens. Different mechanisms can be held responsible for this effect: during spincoating, fractional deposition of the components happens leading to separation of the ionic species close to the electrode materials. During the following annealing the ions diffuse leading to broad, shifted peaks. To some extent also the solubility of lithium ions in the ITO base electrodes can be held responsible for this separation, and, last but not least, the built-in field that occurs when electrode materials with different Fermi levels are used leads to a separation of the anionic and cationic species. All in all those effects lead to an inhomogeneous distribution of the ionic species and thus to a more or less pre-set polarity of these devices.

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ZnCdSe/ZnSe Quantum Wires by Epitaxy on Prepatterned GaAs Substrates

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The growth rate of ZnSe depends sensitively on the crystalline orientation. This anisotropic growth enables us to obtain lateral confinement in quantum wells grown on prepatterned GaAs substrates. We obtain blue light emitting ridge quantum wires and demonstrate the feasibility to fabricate V-groove quantum wires in II-VI compounds. The lateral confinement is studied by low temperature luminescence experiments.

1. Introduction

$Zn_{1-x}Cd_xSe$/ZnSe quantum wells can be utilized for the fabrication of laser diodes emitting in the blue-green spectral range. For III-V semiconductors it has been demonstrated that the spike-like density of states in reduced dimensions yields much narrower and higher gain peak values as compared to quantum well lasers [1]. Up to now, ZnCdSe/ ZnSe nanostructures were fabricated by post molecular beam epitaxy (MBE) structurizing and etching techniques [2]. However, these nanostructures suffer from damage induced by the etching process, and the optical properties are dominated by nonradiative recombination and strain relaxation processes [2]. For that reason, we investigate the possibility to realize quantum wires by MBE on patterned GaAs substrates, to achieve "V-groove" or "ridge" quantum wires.

2. Selectivity of the MBE Growth

As substrates we prepare (100) oriented GaAs gratings with a period of 800 nm by laser holography and subsequent preferential wet chemical etching. The etching gives trapezoidal shaped ridges, with (111) and (1-1-1) planes as side walls, embedded between grooves with various widths and depths. The substrates were dipped in HCl/H_2O before they were transferred into the MBE chamber. As reference, an unpatterned GaAs substrate was mounted on the same sample holder. The growth was performed at a substrate temperature of 350 °C in an anion enriched growth regime using elementary Zn, Cd, and Se effusion cells. To investigate the anisotropy of the growth, a sample was fabricated consisting of a stack of nominally 50 nm thick ZnSe and $Zn_{0.8}Cd_{0.2}Se$ layers. The transmission electron micrograph in Fig. 1 shows the cross section of this sample. It clearly demonstrates that the growth rate of both alloys, the ZnSe and the ZnCdSe, is smaller on the (111) side walls of the substrate grooves as compared to the (100) oriented substrate regions on the bottom of grooves and on top of the ridges.

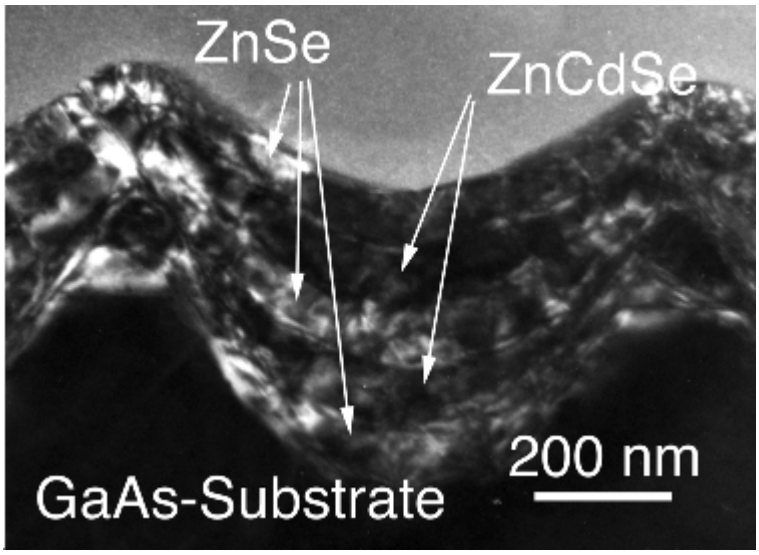

Fig. 1: Transmission electron micrograph of a stack of nominally 50 nm thick ZnSe/ZnCdSe layers grown on a patterned GaAs substrate.

According to these different growth rates, a quantum well grown on such a patterned substrate will be thinner at the sidewalls of the grooves also. Carriers in the quantum well will be confined in lateral direction by those thinner parts. The carriers will be localized in the potential minima of the well at the bottom of the grooves and on top of the ridges. Thus, quantum wires can be realized by the choice of the width of the (100) surfaces of the patterned GaAs substrates and by the choice of the buffer thickness under the quantum well.

3. Fabrication of Quantum Wires

In order to obtain quantum wires the following layer sequence was chosen: a 5 nm wide $Zn_{0.8}Cd_{0.2}Se$ quantum well was grown on top of a 150 nm thick ZnSe buffer layer and was capped by 120 nm ZnSe. This layer sequence was grown on two differently patterned substrates simultaneously. For both substrates the depth of the grooves was 160 nm. In sample no. 1 the width of the (100) planes on top of the ridges was 340 nm while for sample no. 2 this width was reduced below 20 nm. Fig. 2 (a, b) shows scanning electron micrographs of the sample cross sections. The surface height profiles are measured with an atomic force microscope (AFM). The results presented in Fig. 2 (c) and (d) demonstrate quantitatively the differences between these two samples. For sample no. 1, the surface shows narrow ridges with steep side walls restoring the initial (111) planes of the GaAs substrate. The ridges are separated by flat parts in the grooves. From the surface profile and the cross section (Fig. 2) it can be concluded that in this particular sample a quantum wire could be formed on top of the ridge while the lateral dimensions of the quantum well in the groove are to large to yield quantum confinement effects.

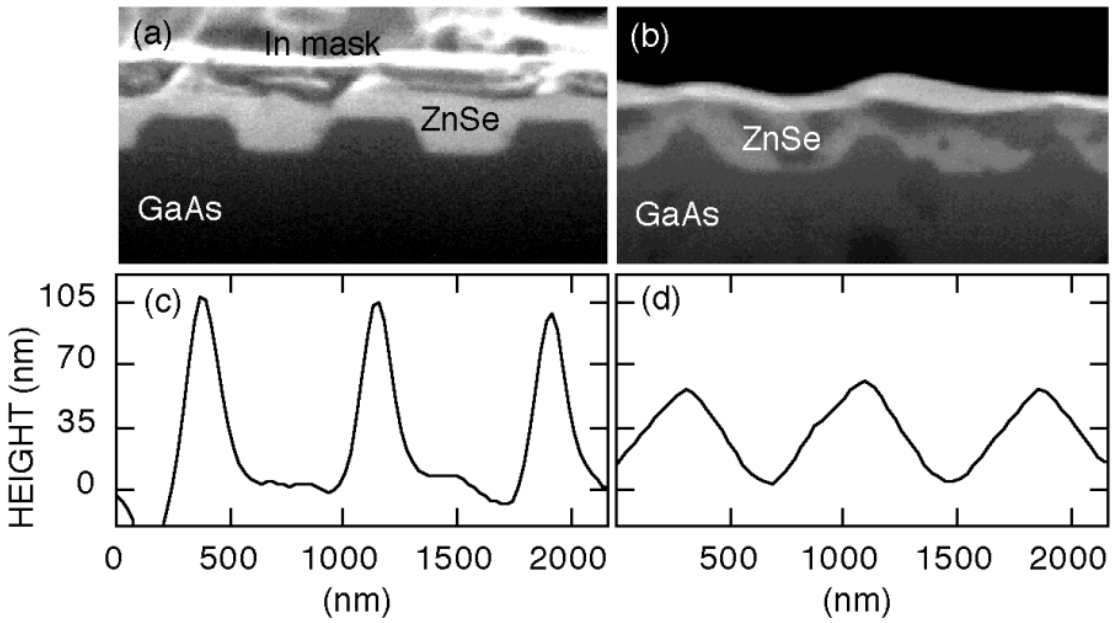

Fig. 2: Cross section of sample no. 1 (a) and no. 2 (b) together with AFM-height profiles of the surface in (c) and (d).

However, in sample no. 2 the situation is completely changed. This sample shows a zigzag surface profile with a slope of the side walls much smaller than that of the substrate. This flattened surface indicates that the ZnSe grows slowest on top of the ridges. So, on such substrates quantum wires could be formed only in the grooves.

4. Optical Properties

At low temperatures the ZnSe/ZnCdSe quantum wire structures show bright luminescence in the blue-green spectral range. The two-dimensional reference sample shows a single, excitonic emission line at 2.60 eV with a width of 11 meV. However, the spectra of the quantum wire samples are much broader and exhibit a more complex shape. Sample no. 1 shows an emission maximum at 2.59 eV with a shoulder in the blue (Fig. 3 (a)). In the spectrum of sample no. 2 two distinct emission maxima are resolved. These emission spectra are a result of the anisotropic quantum well width. However, the luminescence is also affected by lateral carrier confinement [3] and strain relaxation [4]. An assignment of the photoluminescence spectra can be done only with the help of spatial resolved low temperature cathodoluminescence experiments. A detailed study will be presented elsewhere. However, for sample no. 1 the red edge of the luminescence is located on top of the ridge while in sample no. 2, in contrast, the origin of the red luminescence peak is on the bottom of the groove. So, the luminescence experiments confirm the suggestions presented above: sample no. 1 indeed represents a “ridge” quantum wire while sample no. 2 demonstrates the possibility to achieve blue light emitting “V-groove” quantum wires.

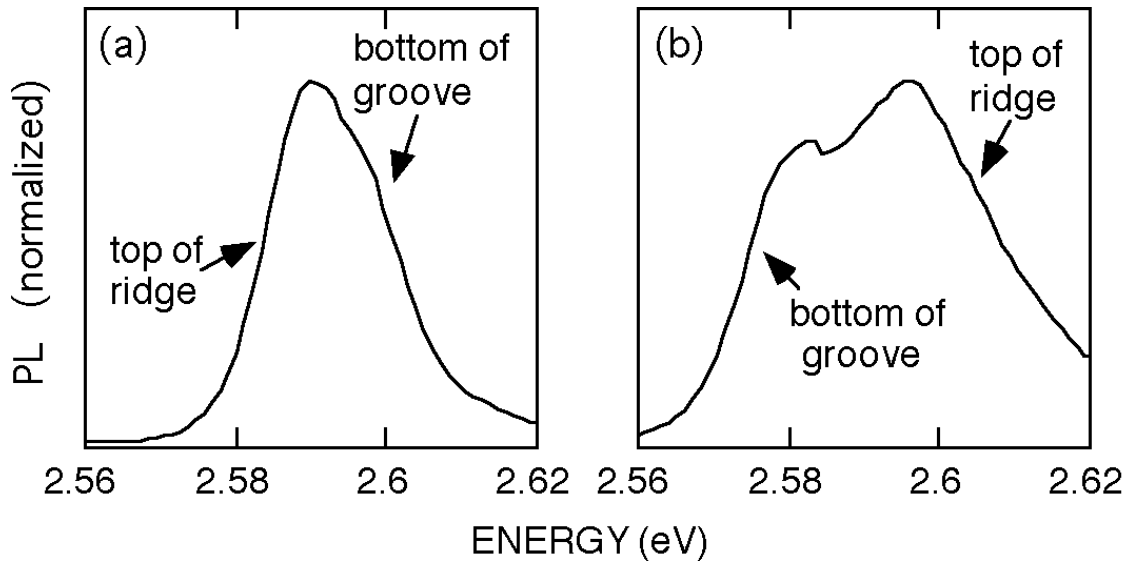

Fig. 3: Low temperature luminescence spectra of sample no. 1 (a) and no. 2 (b) excited by the 458 nm line of an Ar laser.

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GaAs/AlGaAs Based Intersubband and Interminiband Mid-Infrared Emitters

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Intraband optical transitions in the conduction band of GaAs/AlGaAs heterostructures are used to generate mid-infrared radiation. Bandstructure engineering and epitaxial growth techniques make it possible to tailor the emission wavelength of mid-IR light emitting diodes over a broad range (6 – 12 micrometer). We report on the realization of these emitters, showing two different concepts. The first, interminiband emitter is based on optical transitions across the minigap of a strong coupled superlattice. The second concept is using optical transitions between discrete states in a system of coupled quantum wells. Emission, photovoltage and transmission spectra are presented. Self consistent calculations of these structures are performed and compared to the experimental data. The structures are designed to achieve population inversion in different subbands of the conduction band.

1. Introduction

Environmental monitoring, medicine, and many other technological branches are yearning for compact light sources in Mid-Infrared (MIR) part of the spectrum. The only commercially available solid state lasers working in MIR are based on lead-salt semiconductors. Since the demonstration of the first Quantum Cascade Laser (QCL) by Faist et al (1994) [1] it became a viable source of coherent (MIR) radiation. A significant progress in the performance and operating characteristics of the QCLs has been achieved during the last five years. In 1996 operation above room temperature and peak powers of 100 mW [2], as well as CW operation at 110 K [3] was reported. A distributed feedback (single mode) QCL [4] and tunable QCL [5] were introduced in 1997. Microcylinder QCL with a bow-tie mode is reported in 1998 [6].

All these results have only been reported using a single material system, InGaAs/InAlAs lattice matched to InP. The strain requirements limit the composition of the InGaAs and the InAlAs ternaries. The GaAs/AlGaAs [7] system offers very good lattice match over the whole range of aluminum content in AlGaAs. Emitters based on this material are demonstrated [8] and lasing action at cryogenic conditions is achieved [9]. GaAs/ AlGaAs is the most common III-V semiconductor material system used in the technology. Economical aspects of its using are also not negligible, since many possible applications are cost limited which is the only obstacle in their introduction to praxis.

2. Unipolar Quantum Cascade Emitters

Radiation in common laser diodes is achieved via radiative recombination of electron-hole pairs across the bandgap. Quantum cascade emitters are using optical transitions of electrons between the discrete states within the conduction band of a semiconductor

heterostructure. Thus the emitted wavelength is significantly less temperature dependent compared to the bandgap emitter. Bandstructure engineering allows tailoring of the emission wavelength to the application requirements over a broad range.

A Quantum Cascade (QC) emitter consists of an active cell, where the radiative transitions take place, and of an injector. The injector supplies electrons into the upper state of the active cell and secure extraction from its lower states. Active cell-injector units are cascaded (typically 25 units in cascade).

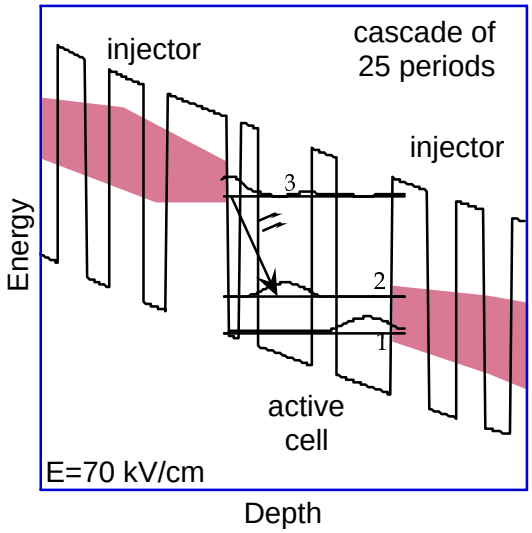

Fig. 1: Conduction band of the intersubband emitter

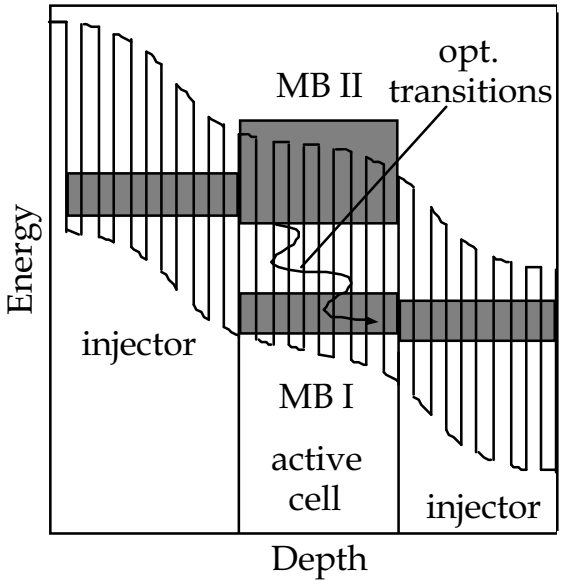

Fig. 2: Conduction band of the interminiband emitter

Two concepts of the active cells are known. The intersubband (ISB) concept is using typically three coupled quantum wells with three discrete energetic levels (Fig.1). Transition (3–2) is radiative. Transition (2–1) is tailored to have an energetic spacing around

36 meV (LO phonon energy in GaAs). It serves for fast extraction of the electrons from state two. Since the ratio of $\tau(3-2)/\tau(2-1)$ lies in the order of 10, transition (2–1) is necessary to maintain population inversion. A superlattice, where the radiative transition across the minigap is used as an active cell of the interminiband concept (IMB) (Fig. 2). The internal field arising from the doping acts against the external field across the device which results in the band alignment depicted in Fig. 2. Electrons are tunneling from the injector into the miniband MB II. Optical transitions occur from the lowest state of MB II into the highest state of MB I and the electrons are free to move via the following injector into the adjacent active cell. Optical transitions between the higher states in the minibands appear at higher bias voltages. The active cell of the interminiband emitter can be a regular periodic superlattice or an aperiodic (chirped) superlattice. These modifications are used in order to maximize the optical dipole matrix element and to suppress the tunneling of the electrons from the upper states into the continuum.

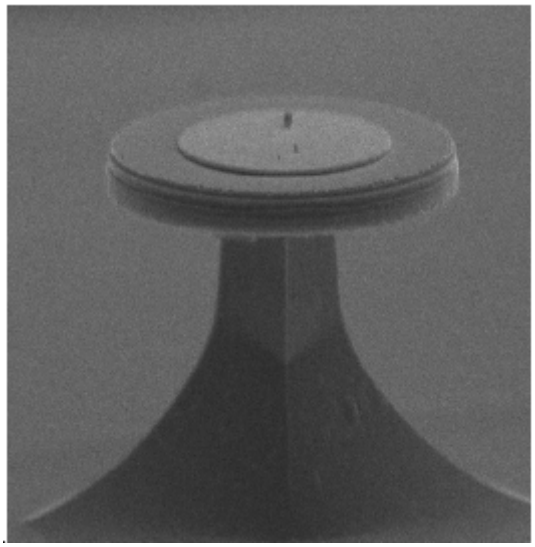

Fig. 3: SEM picture of a processed disk

The implementation of these emitters into a resonator enables lasing action. Optical confinement is achieved using cladding layers that are embedding the gain medium. An alternative concept with direct access of the current to the gain medium is a disk resonator (Fig. 3). It offers the possibility to study lasing action in the gain medium independently of any cladding layers. Lasing action can take place on the free standing periphery of the disk. Light is totally reflected on the boundaries of the disk and forms closed whispering gallery modes. Low threshold current and weak omnidirectional emission is typical for these lasers.

3. Experiment

Samples are grown using standard molecular beam epitaxy (MBE) [7]. They consist typically of about 500 layers. They are lithographically processed into ridges, mesas or disks (Fig. 3). Non alloyed metallic contacts are evaporated, before these emitters are soldered to a heat sink and bonded.

The current-voltage characteristics are measured at cryogenic conditions using both quasistatic and pulsed method. Parallel to pulsed I-Vs an integral output characteristics

is recorded. Light is collected using f/0.7 optics and focused on a LN_2 cooled MCT detector. Since the emitted power of these devices lies in the range of nanowatts, correlation techniques must be used to detect the signal. Step-scan, Fourier transform spectroscopy [10] is used for the spectral analysis of the electroluminescence. Besides the emission measurements we perform photocurrent and transmission measurements as a complementary characterization of the emitters.

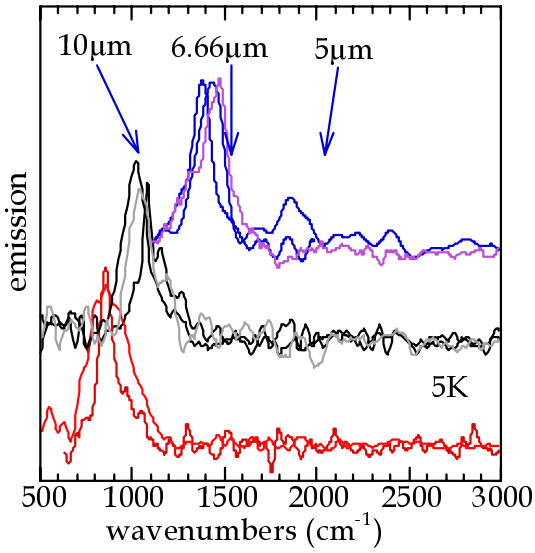

Fig. 4: Spectra of the unipolar QC emitters

Both intersubband and interminiband concepts are tested. Some of the measured spectra are depicted in Fig. 4. Emission wavelengths are covering the range between five and twelve µm. Peak quality (Position/FWHM) of 14 testifies outstanding quality of the growth and the used materials. The electroluminescent light was analyzed using a grid polarizer. High degree of TM polarization (up to 100%) was observed. Comparison of the peak maxima positions to the self-consistent calculation of the structures shows good agreement.

Trade-off between the requirement of high electrical conductivity and the optical parameters, like sufficient thickness and low absorbance of the cladding layers, appears to be the substantial problem on a way to electrically pumped laser. A disk resonator was fabricated. Measurements encountered problems with the inhomogeneous current distribution and did not allow to achieve lasing action.

4. Conclusion

GaAs/AlGaAs unipolar quantum cascade emitters have been designed, grown, and characterized. Optical and electrical methods are used for the investigation. We have demonstrated function of both intersubband and interminiband concepts as well as possibility of tailoring the wavelength from five to twelve µm. The measurement results are showing good agreement with the calculations, proving us outstanding quality of the technology.

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Light Generation by Er in Si Related Materials

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Er-doped Si is utilized for Si-based light generation in the 1.54 µm region, which is of particular interest for optical data communication. The main problem of Si: Er was so far the huge temperature quenching of the luminescence yield of forward biased diodes. It turned out that properly designed diodes driven in reverse bias avoid this temperature quenching due to different excitation and deexcitation mechanisms. The fabrication and annealing conditions for maximum luminescence yield at room temperature are presented.

1. Introduction

One of the last unsolved problems and challenges in Si technology is the integration of compatible light sources as needed for optical communication within or between chips. Although there are different approaches followed worldwide, there is no obvious solution so far [1]. One of the most promising principles proposed is the light generation by intra-4f transitions in Er, which can be integrated in very different hosts giving always the same characteristic sharp spectra. Additionally, as a consequence of the well shielded 4f-shell, the emission wavelength at 1.54 µm is temperature independent. Since the first diodes fabricated by Ennen [2] *et. al*, the temperature quenching of the luminescence yield in forward bias is still the main problem, although several groups [3], [4] were focused on Si:Er. The intensity of the room temperature emission in forward bias, however, is rather weak and comparable to the dislocation related luminescence.

For reverse bias, a completely different situation occurs. Almost no temperature quenching of the electroluminescence (EL) signal is observed indicating different excitation and deexcitation mechanisms of the Er-ions compared to forward biased diodes [5]. High resolution spectra show, that no additional emission centers are excited in reverse bias. The excitation efficiency of some specific center is very different in the two excitation modes. The efficiency for exciting isolated Er centers with a sharp emission is higher in forward bias, whereas in reverse bias mainly centers are excited with an emission similar to Er-doped silica. At elevated temperatures only the SiO_2 centers are excited, in both forward and reverse biased diodes. Therefore we investigated the preparation conditions for optimum formation of Er-doped SiO_2 centers within the Si host, which lie in a narrow region of Er and O concentrations and specific annealing treatments after ion implantation.

2. Experimental

Erbium was implanted in n-type (100)-CZ-Si with a resistivity of 10 Ωcm at room temperature. The Er-dose at an implantation energy of 300 keV was varied between 10^{12} and 10^{15} cm^{-2} producing a maximum Er concentration in a depth of 100 nm ranging

from 10^{17} to 10^{20} cm^{-3}. The dose and energy of oxygen was adjusted to reach a ten times higher O concentration than Er concentration, which was found to give maximum photoluminescence (PL) yield. In order to remove the implantation damage and to optically activate the dopants, the samples were annealed for 30 min at temperatures between 400 and 1000 °C. Si: Er diodes were implanted through a SiO_2-mask for improved diode characteristics in reverse bias. The p/n-junction in a depth of 100 nm was formed by implantation of Er with a dose of 3×10^{14} cm^{-2} at an energy of 600 keV and with B at 40 keV and a dose of 6×10^{13} cm^{-2}. Ohmic contacts were formed by implantation of B with a dose of 2×10^{14} cm^{-2} at 30 keV at an implantation angle of 80° and with P at 30 keV and a dose of 10^{15} cm^{-2} at the back side. After annealing at 1000 °C Al contacts were evaporated, the light output was enabled through an open area of the front contact.

3. Results and Discussion

At low Er concentrations an increase of the PL intensity with increasing Er concentration is observed for samples annealed at 900 °C. These samples emit atom-like spectra with linewidths of 0.5 nm. Although O co-doping increases the number of optically active Er ions, above an Er concentration of 10^{18} cm^{-3} a decrease of the PL intensity at 77 K for samples annealed at 900 °C is observed.

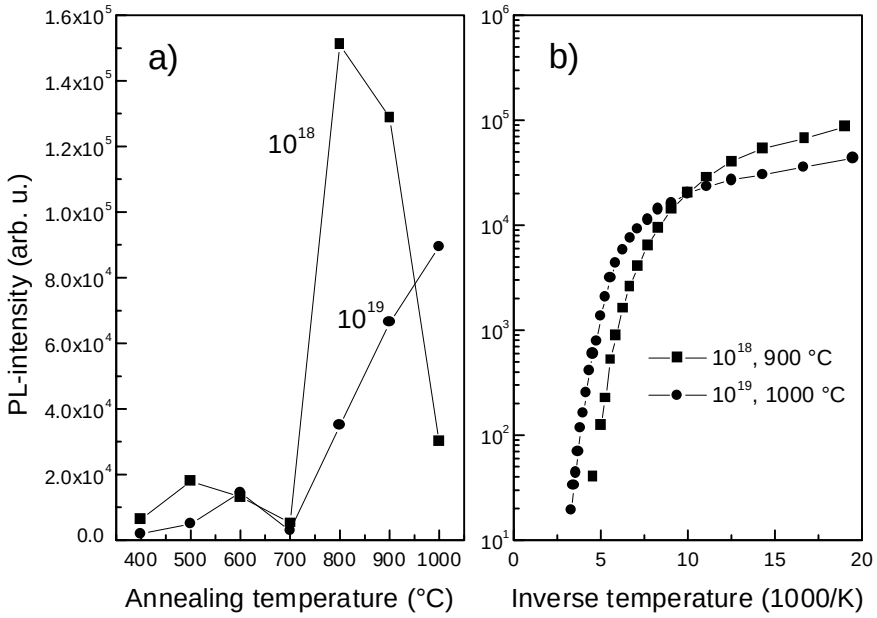

Fig. 1: a) Dependence of the PL-yield on the annealing temperature for Er concentrations of 10^{18} and 10^{19} cm^{-3} at 77 K. b) Temperature quenching of the PL intensity from samples with Er concentrations of 10^{18} and 10^{19} cm^{-3} annealed at 900 °C and 1000 °C.

An annealing treatment at 1000 °C increases the maximum emission yield to an Er concentration of 10^{19} cm^{-3}, accompanied by a change of the emission spectra. Samples annealed at 1000 °C show spectra similar to Er-doped SiO_2, independent of the particular Er concentration. The conditions for the formation of the SiO_2 center are optimized at an Er concentration of 10^{19} cm^{-3}.

The luminescence intensity of the dominating center is shown in Fig. 1a for an Er-concentration of 10^{18} and 10^{19} cm^{-3}. Between 400 and 600 °C, the emission is rather weak due to implantation induced defects depending on the Er dose. Although the PL intensity of the 1000 °C annealed sample is lower at 77 K than from the 900 °C annealed sample, the onset of the temperature quenching is shifted to higher temperatures, as shown in Fig. 1b, allowing weak room temperature emission of the 1000 °C annealed sample. Different deexcitation energies of 150 meV (Er: 10^{19} cm^{-3}, 1000 °C) and 100 meV (Er: 10^{18} cm^{-3}, 900 °C) indicate different levels in the Si bandgap participating in the energy backtransfer from Er to the host. Such a backtransfer mechanism is responsible for the temperature quenching of 3 orders of magnitude of the luminescence intensity and this amount is nearly independent of the applied sample treatment under PL conditions.

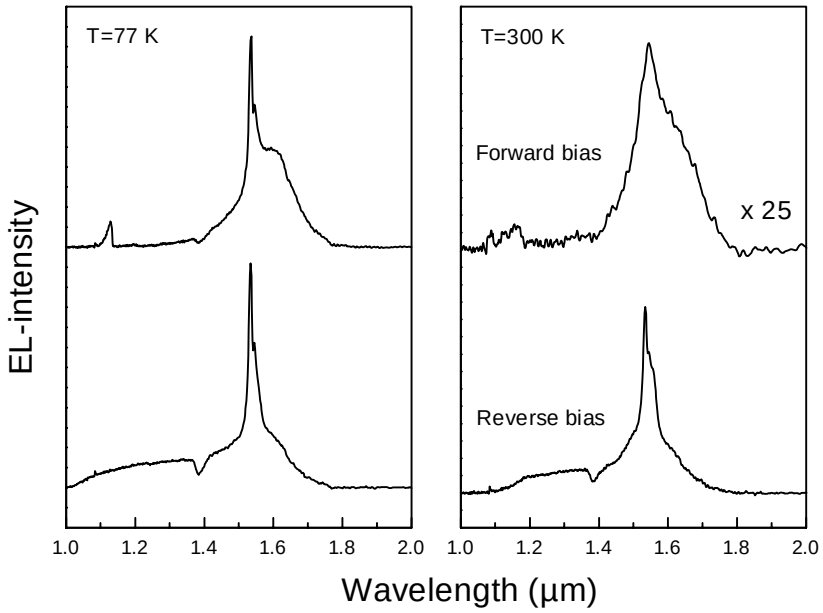

Fig. 2: EL spectra of forward and reverse biased Si:Er LEDs at 77 K and at room temperature. In forward bias, the Er emission is nearly quenched, whereas the EL yield under reverse bias conditions is practically temperature independent.

The electroluminescence (EL) yield of forward biased diodes suffers, similar to PL conditions, from backtransfer induced quenching at higher temperatures. The EL spectra at 77 K indicate that the efficiency in exciting dislocations is higher in forward bias compared to the reverse biased diode, as shown in Fig. 2. The room temperature spectrum of the forward biased diode is dominated by dislocation related luminescence, the Er-related EL is hardly visible.

In reverse bias, however, almost no difference of the EL yield is observed by increasing the temperature up to 300 K. In addition to the Er-4f-emission, a broad background extending up to the visible range is emitted from the reverse biased diode. This background is proposed to originate from scattered hot carriers, which were accelerated within the high electric field in the reverse biased p/n-junction. In contrast to the exciton mediated excitation of forward biased diodes, the Er-ions are impact-excited by hot carriers under reverse bias [6]. The absence of the strong temperature quenching of the EL yield in reverse bias indicates a different deexcitation as compared to forward bias. Ei-

ther the backtransfer path is passivated in the high electric field or only those Er ions are impact-excited which lie within silica precipitates without efficient energy transfer back to the Si host. The spectra of highly O codoped diodes are similar to Er doped silica, indicating the possibility of Er doped SiO_2 precipitates responsible for room temperature emission.

4. Conclusion

The standard annealing treatment at 900 °C after Er implantation induces the formation of isolated Er centers giving rise for sharp emission at low temperatures. The emission of those centers, however, is quenched already at temperatures below 200 K. Increasing the annealing temperature to 1000 °C removes all sharp lines, the obtained spectra are similar to those of Er doped silica. The EL spectra of Si: Er diodes indicate that mainly those Er doped silica precipitates are excited in reverse bias. Therefore, the conditions for the formation of this particular center were optimized. Strong room temperature EL was obtained from diodes in reverse bias with an Er concentration of 10^{19} cm^{-3} and an annealing treatment at 1000 °C.

Acknowledgements

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GaAs VCSELs with Dielectric Si_3N_4/SiO_2 Mirrors

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We present a procedure to fabricate GaAs based VCSELs utilizing Si_3N_4/SiO_2 Bragg mirrors. Current injection into the active region is defined by selective wet oxidation of AlAs. A CW threshold current of 800 µA is measured at 20 °C for a device with 5 µm square oxide aperture. The fabrication process presented here is suitable for integration of VCSELs and RCPDs.

1. Introduction

While the development of GaAs vertical-cavity lasers (VCSELs) is mainly driven by the need for optical data link products for short-haul communication, other possible applications such as laser printing and optical processing are being discussed. The field of application could be extended by developing the VCSEL technology further to include greater functionality, e.g. by integration of a resonant-cavity photodetector (RCPD).

Integration of VCSELs and RCPDs requires a technology allowing to simultaneously optimize the performance of the VCSELs and the RCPDs, whose bandwidth and responsivity are determined by the reflectivity of the incoupling mirror [1]. The need for integrating cavities with different Q factors (i.e. high Q for VCSELs and lower, adjustable Q for RCPDs) is difficult to fulfill with standard VCSEL technology using all-epitaxially grown cavities. Our approach is to use Si_3N_4/SiO_2 Bragg mirrors as top reflectors, allowing the Q factors of the RCPD cavity to be adjusted at will.

2. Sample Preparation

The VCSEL structure is an organometallic chemical vapor deposition (OMCVD) grown diode structure with a 30-periods AlGaAs/AlAs Bragg mirror stack on the substrate side. The 7λ/4-cavity contains three GaAs quantum wells separated by $Al_{0.2}Ga_{0.8}As$ barriers. $Al_{0.5}Ga_{0.5}As$ spacer layers are added on both sides to achieve efficient carrier confinement. The cavity is completed by a 30 nm AlAs oxidation layer embedded in $Al_{0.9}Ga_{0.1}As$, followed by 112 nm $Al_{0.2}Ga_{0.8}As$ and a 10 nm highly p-doped GaAs cap layer to obtain ohmic contacts and homogenous current spreading into the active region.

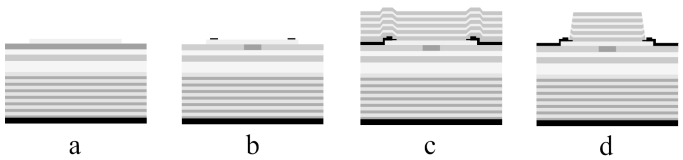

Fig. 1: Cross-sectional view of an oxidized GaAs VCSEL with Si_3N_4/SiO_2 top mirror.

A broad area Sn/Au contact is deposited at the backside of the substrate and annealed at 380 °C. The top layers are etched to form shallow square mesas exposing the AlAs oxidation layer (Fig. 1a) which is subsequently oxidized in a furnace set at 520 °C (Fig. 1b). *In situ* optical monitoring is used to stop the oxidation process. Electrical contact is made to the p-type GaAs surface using Cr/Au metallization (Fig. 1c). The top Bragg mirror is deposited by plasma enhanced chemical vapor deposition (PECVD) and consists of 16 pairs Si_3N_4/ SiO_2 (Fig. 1c). It has already been shown that these mirrors meet the demands on reflectivity for use in VCSELs [2]. A two-step etching process is used to pattern the top mirror (Fig. 1d): the first step, Ar-ion etching, is stopped approximately 50 nm above the metallization, the remaining dielectric is then removed in a reactive ion etch process which exposes the extended contacts of the devices.

RCPDs with an area of 50 µm square were integrated beside the VCSELs, but have not been investigated so far. Tuning the RCPDs to the desired bandwidth and responsivity can be accomplished by removing excessive mirror pairs in a further etch step.

3. Performance of the VCSELs

Figure 2 shows the CW-output characteristics of a VCSEL with a 5 µm square oxide aperture at room temperature. Threshold current (800 µA) is comparable to that of all-epitaxial devices [3], but due to the high drive voltage, wallplug efficiency does not exceed 7.4 %.

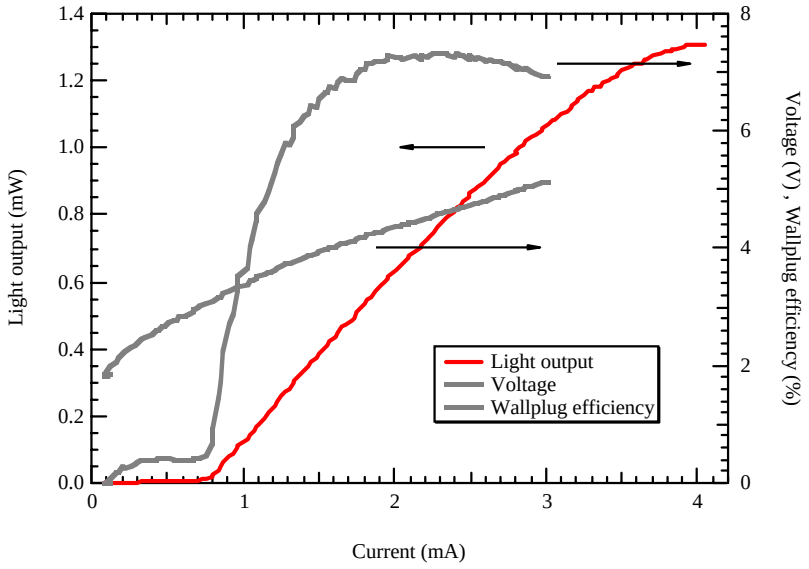

Fig. 2: Output characteristics of a 5 µm square GaAs VCSEL.

Because of the lateral current injection into the active zone, a high differential resistance is expected to be inherent in these devices [4], but we believe that the extremely high value of 920 Ω is partially caused by the technology used to fabricate the samples: we noticed that the GaAs cap layer was visibly attacked by an unplanned HCl dip which had become necessary to improve the sticking properties of the photoresist on the sample. The removal of the cap layer could well account for the poor conductive properties of the diode. A numerical simulation of the cavity shows that the resonance wavelength is blue shifted by approximately 6 nm if the cap layer is missing. This is in good agree-

ment with the observed laser wavelength of 843.5 nm as opposed to the design wavelength of 850 nm.

In Fig. 3, optical output characteristics for CW operation are shown for various temperatures. Despite the mismatch between resonance wavelength and spectral gain maximum, lasing action continues up to an operating temperature of 90 °C, threshold current increases from 750 µA at –10 °C to 2 mA at 90 °C.

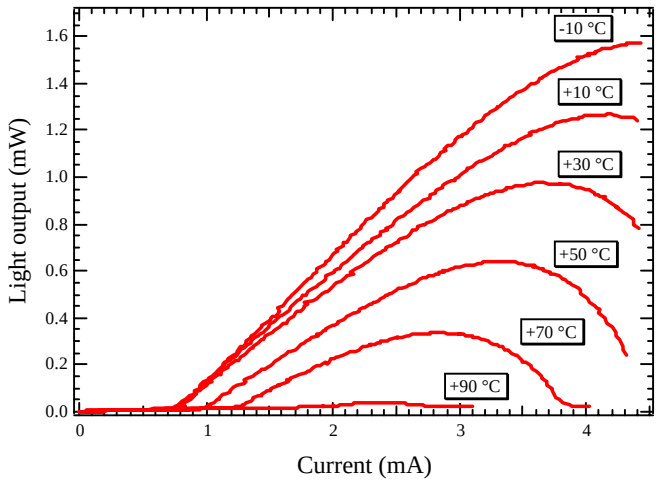

Fig. 3: Light output versus current of a 5 µm square GaAs VCSEL at different temperatures.

Due to the smaller temperature coefficients of the refractive index of Si_3N_4 and SiO_2 as compared to the GaAs/AlAs material system, the lasing wavelength of our VCSELs shows a smaller temperature dependence (Fig 4) than all-epitaxial devices [3], [4]. The spectral shift of the emission wavelength is 0.045 nm/K. The shift due to dissipated power is evaluated to 0.092 nm/mW, resulting in a thermal resistance of 2.04 K/mW.

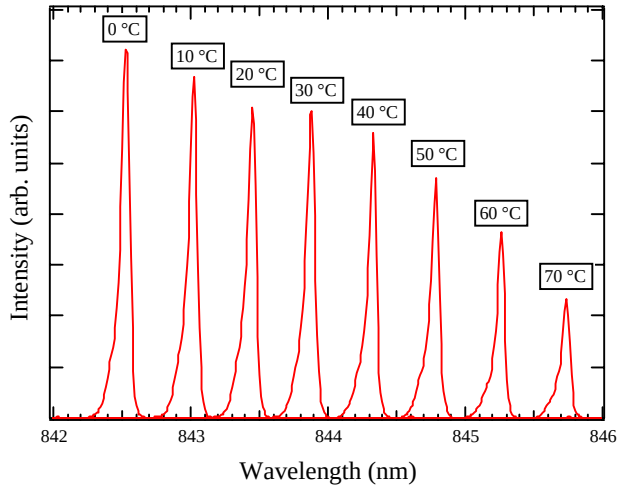

Fig. 4: Temperature dependence of the emission wavelength of a 5 µm square VCSEL. The linewidth is resolution limited.

We further investigated the influence of the oxide aperture on the transverse lasing mode. Fig. 5 shows the nearfield patterns of 7 and 5 µm VCSELs. The strong index guiding of the oxide aperture causes the 7 µm devices to lase in the TEM_{11}-mode. Aperture sizes of 5 µm or smaller are required to maintain lasing in the fundamental TEM_{00}-mode throughout the observed pumping range.

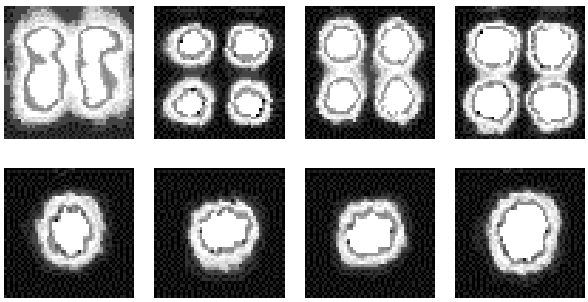

Fig. 5: Nearfield patterns of a 7 µm (top) and 5 µm (bottom) square oxide aperture VCSEL at different pumping levels. (1.5 mA, 2 mA, 3 mA and 4 mA (from left to right).

4. Conclusion

We described the fabrication of GaAs based VCSELs incorporating PECVD deposited Si_3N_4/SiO_2 top Bragg mirrors. This process is suitable for the integration of VCSELs and RCPDs. In CW operation at 20 °C threshold currents of 800 µA and wallplug efficiencies of 7.4 % were achieved in devices with 5 µm oxide aperture. Maximum light output power is 1.3 mW. Both the temperature coefficient of the emission wavelength (0.045 nm/K) and the thermal resistance (2.04 K/mW) are significantly smaller than in all-epitaxial devices.

Acknowledgements

This work was sponsored by the *Forschungsförderungsfonds der gewerblichen Wirtschaft*.

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Determination of Trace Element Distribution in Cr Sputter Targets by 3-d SIMS

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Secondary ion mass spectrometry (SIMS) is a powerful and effective approach for the characterization of the lateral and three dimensional distribution of trace elements in solids. The investigation of the trace element distribution in two chromium samples which were produced by sintering process and hot isostatic pressing is reported. By applying two-dimensional (2-d) SIMS, it is shown that in both samples the gaseous impurities O and N diffuse to the grain boundaries. Three-dimensional (3-d) SIMS measurements illustrate that there are major differences in the spatial distribution of trace elements.

1. Introduction

The microelectronics industry with its permanent search for miniaturizing and higher speed is the driving force for the development of high purity materials. Refractory metals are frequently used for metallization of electronic devices. This is due to their physical characteristics like low resistivity and high temperature stability. They derive their qualities not only from the concentration but also from the three-dimensional distribution of bulk impurities [1]. Chromium sputter targets can be produced by sintering process or hot isostatic pressing (HIP). During the hot isostatic pressing process, the raw material is encapsulated in steel containers and by applying high pressure and high temperature a homogeneous and compact material is formed. In the sintering process the chromium powder is first compressed at room temperature and then heated to 2/3 of the melting temperature. In an additional step the material is rolled for compressing and shaping into its final form.

In the flat panel display manufacturing process those two kinds of sputter targets are competition products used for the metallization of the black matrix and color filters. That is the reason why the characterization by means of GDMS and SIMS is of technological interest. Glow discharge mass spectrometry (GDMS) has emerged as a standard technique used for the quantitative bulk analysis of contaminants in the µg/g range. To achieve two- and three-dimensional elemental distribution information SIMS is a common technique supporting microelectronics technology. SIMS has analytical characteristics such as high detection power (ppm range) and the possibility of detecting all elements including hydrogen. To obtain lateral images a primary ion beam homogeneously illuminates the sample by scanning at about 100 frames per second over an area of typically 500 x 500µm. A point to point representation without loss of lateral position information is achieved by a set of ion lenses. Each pixel on the sample is imaged directly on a fluorescent screen and recorded by a CCD camera. The typical lateral resolution is 1µm. The spatial elemental distribution is achieve by creating layer by layer images as the primary ion beam sputters into the sample. 3d-SIMS can be seen as combination of imaging mode and depth profile analysis. The depth resolution is about 20 nm.

2. Results and Discussion

Figures 1 and 2 illustrate the grain boundary enrichment of the highly diffusable impurities O and N in both chromium samples. Chromium was recorded in order to detect the grain structure. This is possible because the different orientation of the grains influences the sputter coefficient and therefore the intensity of the secondary ion signal. Nitrogen is represented by CN because of the higher sensitivity of this mass compared to N. It was confirmed that no spectral interferences occurred. As result of this experiment we can see in both samples the same tendency of oxygen and nitrogen to enrich at the grain boundaries.

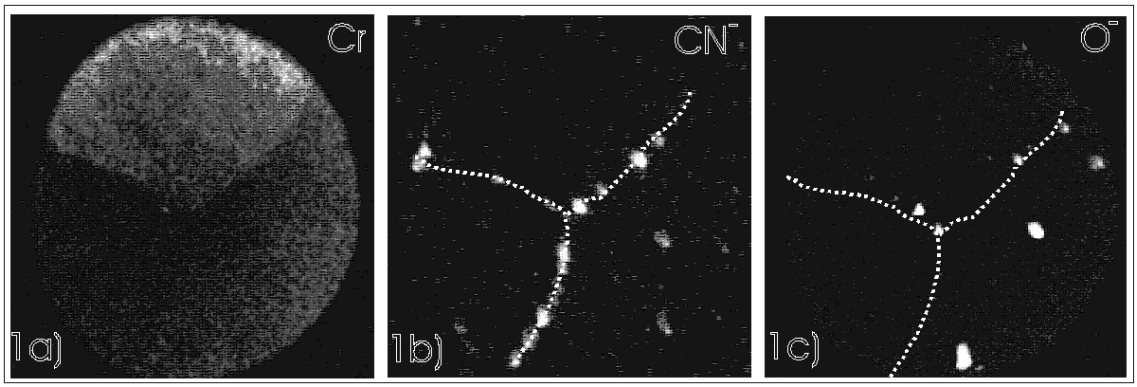

Fig. 1: SIMS images (150 x150µm) of the HIPped chromium sample (100nA Cs^+ primary ions).

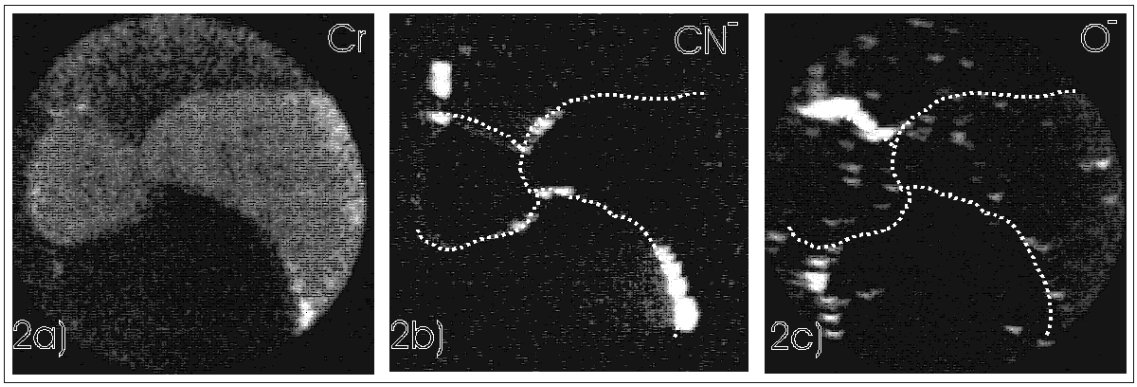

Fig. 2: SIMS images (150 x150µm) of the sintered chromium sample (100nA Cs^+ primary ions).

Fig. 3 to 6 represent the three-dimensional distribution of the elements Na, Ca, O and Cl. Two kinds of primary ions were used, O_2^+ to record the distribution of the metallic impurities and Cs^+ to investigate electronegative trace elements (O, F, Cl, S, CN^- for N).

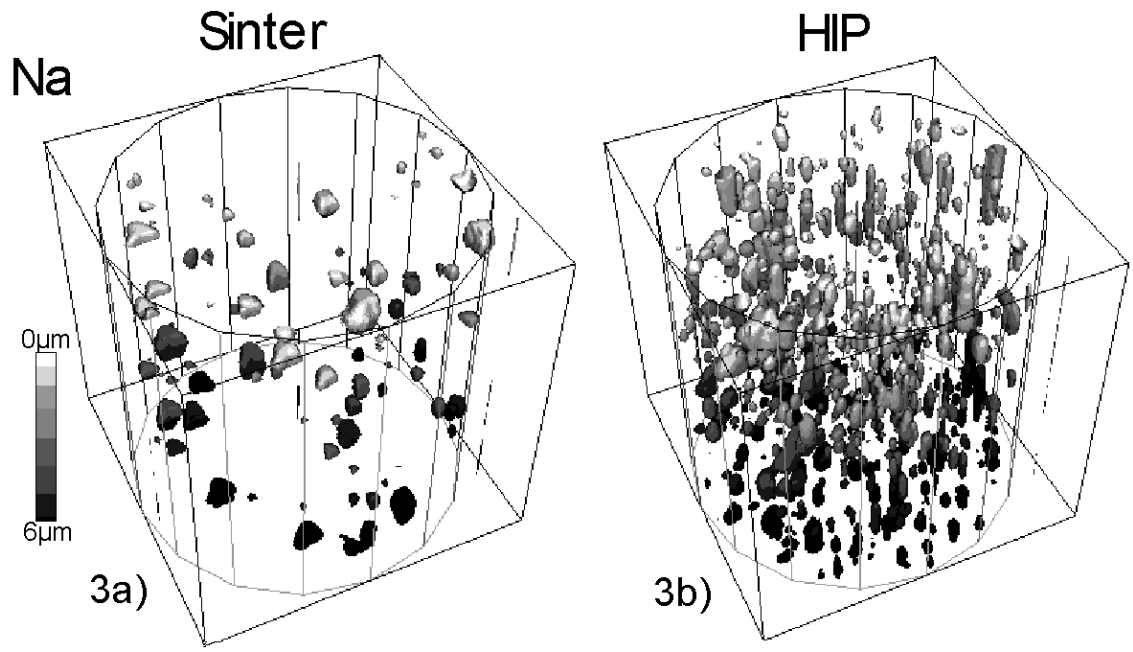

Fig. 3: 3d- images, left from sintered chromium, right from HIPped chromium: Na distribution (O_2^+ PI, 2µA, 150 x 150 x 6µm)

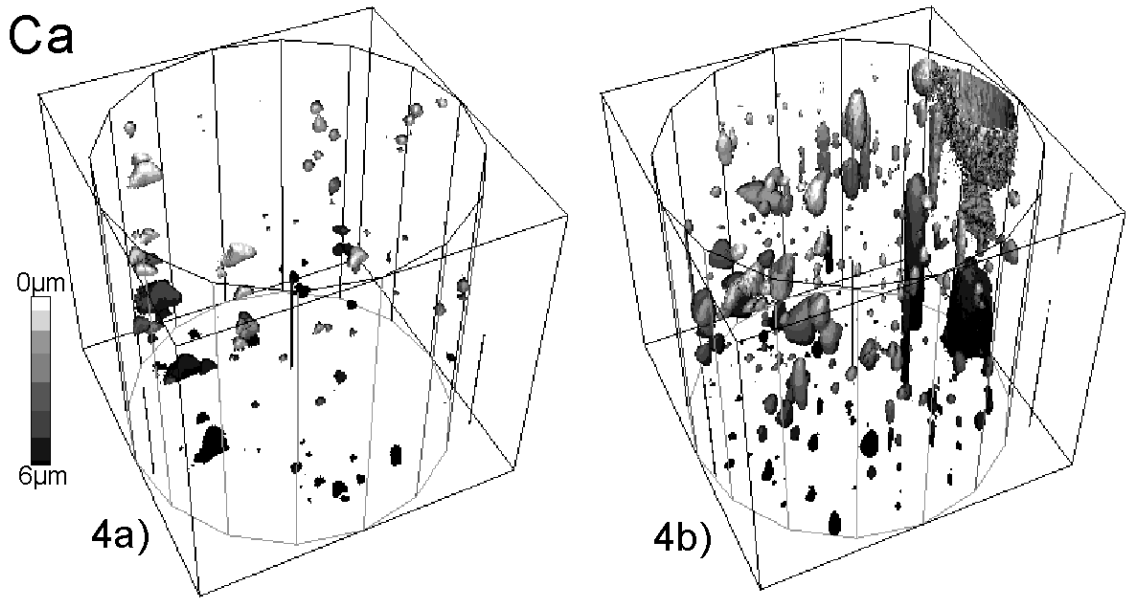

Fig. 4: 3d- images, left from sintered chromium, right from HIPped chromium: Ca distribution (O_2^+ PI, 2µA, 150 x 150 x 6µm)

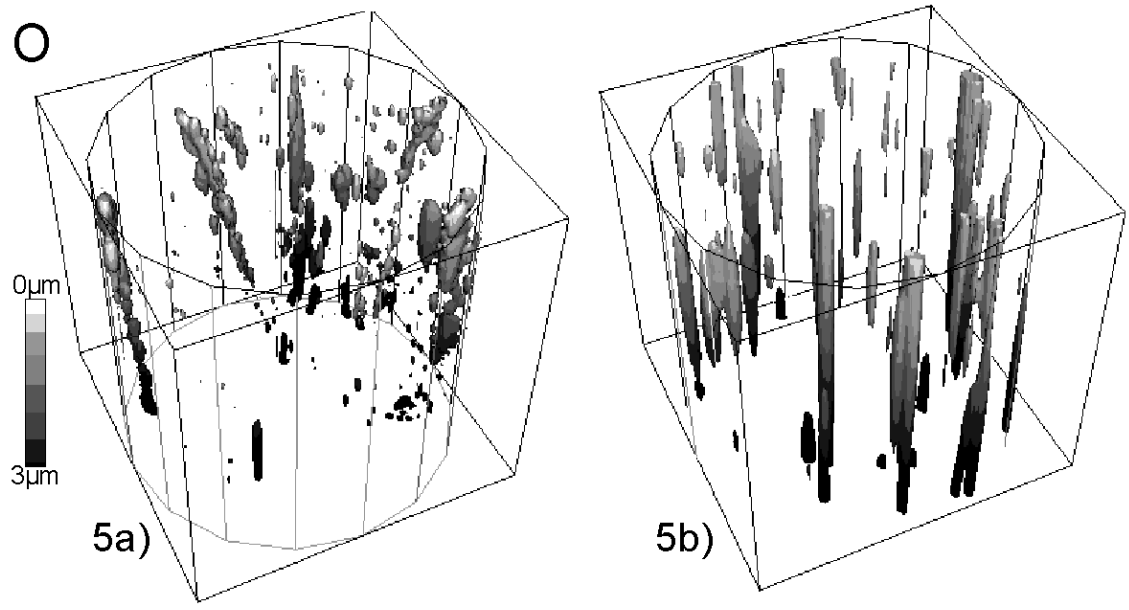

Fig. 5: 3d- images, left from sintered chromium, right from HIPped chromium: O distribution (Cs^+ PI, 50nA, 150 x 150 x 3µm)

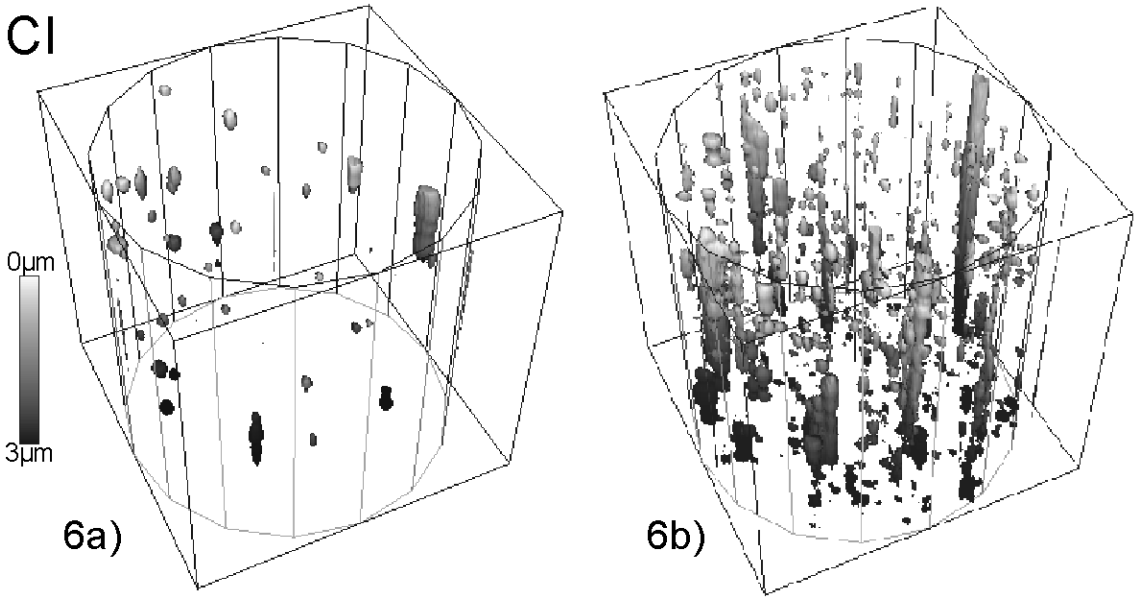

Fig.6.: Cl distribution (Cs^+ PI, 50nA, 150 x 150 x 3µm)

To obtain quantitative information GDMS bulk analysis was applied, which indicated that the average concentration of impurities is significantly higher in the HIPped chromium. The spatial distribution of trace elements is also important for the sputter deposition of the metal, because inhomogeneously distributed contaminants result in particle emission during the sputter process [2]. For the visualization of the obtained analytical data we used isosurface representation, that means that only those volume elements are drawn which correspond to an assigned intensity. 15 different element distributions were examined, 4 of them are presented. Fig. 3 and 4 show differences in the sodium

and calcium distribution. In the HIPped sample, a large amount of small precipitates occur whereas the sintered chromium shows fewer precipitates with similar volume. In the calcium image of the hot isostatic pressed chromium a large precipitate was detected whereas the sintered sample seems to be less contaminated and more homogeneous. Figure 5 illustrates the distribution of oxygen. Specially the grain boundary enrichment is better visible than in the 2d images (Fig.1.c and 2.c). The chlorine distribution (Fig.6) also exhibits major differences between HIPped and sintered chromium.

3. Conclusion

Different produced sputter targets result in different concentration and distribution of contaminants. Summarizing it can be said that sintered chromium is more homogenous and less contaminated, which can be explained by the ability of the trace elements to evaporate during the production process. SIMS supports microelectronics as well as metallurgical industry in order to optimize manufacturing processes and properties of materials.

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GaAs/AlGaAs/InGaAs Bandgap Lasers — From DH Lasers to VCSELs

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Starting from the growth of double hetero (DH) semiconductor bandgap lasers, in the material system AlGaAs/GaAs we are now optimizing laser devices such as a twin waveguide laser and a laser interferometer based on vertical cavity surface emitting lasers (VCSEL).

1. MBE

MBE (molecular beam epitaxy) technique allows the epitaxial growth of different compounds. One of the model materials for optoelectronics are epitaxial layers of III-V semiconductors, mainly GaAs and related compounds. The controlled growth of single crystalline layers on an atomic scale makes it possible to design new materials with optimized electrical and optical characteristics. A solid source MBE system (MOD GEN II) is used for the growth of AlGaAs/GaAs semiconductor lasers and InGaAs quantum well lasers; thus, this machine is further equipped with an indium cell. As doping materials we use silicon for n-doping and carbon for p-doping.

2. Lasers

We started laser growth with double hetero (DH) GaAs/AlGaAs laser structures. This material was characterized by processing broad area lasers and measuring their electrical and optical properties. The threshold current density and differential efficiency are comparable to lasers processed from industrial grown materials [1].

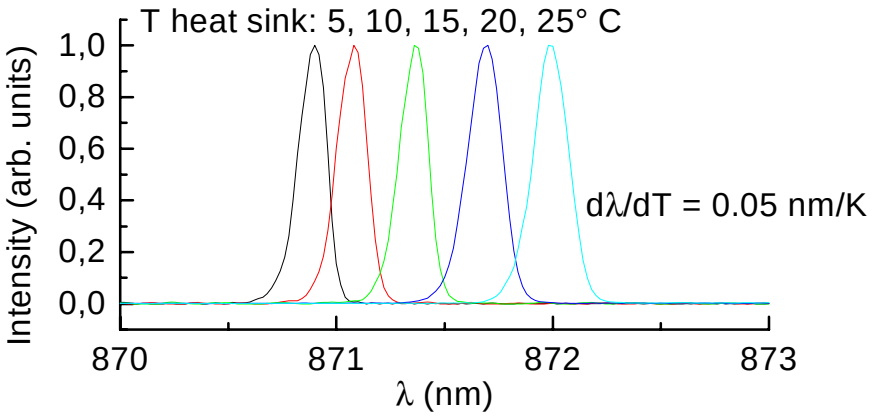

Fig. 1: Emission spectrum of dfb laser 4th order at different heat sink temperatures.

As a next step, ridge lasers were processed out of DH material. The ridge forms a lateral optical waveguide, which allows the realization of single mode lasers, where in addition a longitudinal mode control is needed. A simple model for calculating the lateral optical waveguide is the effective index model. The difference of the effective transverse refractive index and the width of the ridge determines how many lateral waveguide modes are possible and the divergence of the facet emission in lateral direction. Based on the ridge laser design we started to manufacture "single mode lasers" by incorporating a longitudinal mode control via a 4^{th} order dfb (distributed feed back) grating. The reason for choosing a 4^{th} order grating (period 515 nm) at this time was the established holographic grating definition with our HeCd laser setup for this grating period. The measured lasers showed a drift in the emission wavelength of about 0.05 nm/K, as can be seen in Fig. 1 (linewidth limited by the used spectrometer) due to change of the refractive index with temperature, which is in good agreement with literature [2].

As a next step, InGaAs SQW (single quantum well) lasers with separate confinement layers were grown. Strained InGaAs QWs show higher peak material gain than unstrained QWs or bulk material. The lattice mismatch between GaAs and InGaAs determines the so-called critical thickness for InGaAs layers on GaAs. Layers thinner than the critical thickness can be grown without relaxation effects. There are different models for calculating the critical thickness, e.g. by Matthews and Blakeslee or People and Bean [3]. One difficulty in the growth of strained InGaAs layers on GaAs is the calibration of In content and growth rate with RHEED (reflected high energy electron diffraction) measurements, originating from the lattice mismatch of the two materials. Additionally, optical problems remain in InGaAs QW lasers due to the large antiguiding effect and the nonlinear gain behavior at high current densities. E.g. the current density for narrow gain guided lasers increases dramatically for widths below 20 µm [3]. Therefore, a relatively strong index guiding is needed for narrow lasers. The grown SQW material was characterized with broad area lasers and showed threshold densities comparable to state of the art lasers [4], [5]. Ridge lasers with widths from 2 µm to 6 µm show kink-free light output (fig. 2) up to current densities of 5 times threshold density (limited by the setup) and the measured far field pattern indicates that only one lateral mode exists.

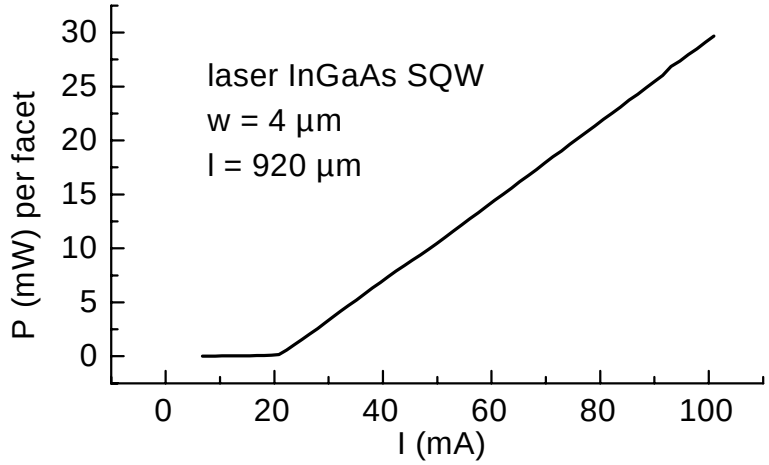

Fig. 2: Emitted power versus injected current of an InGaAs SQW laser (ridge width 4 µm).

Currently we are working on two laser projects, a twin waveguide laser and a laser interferometer.

2.1 Twin waveguide laser

The goal of this project is the realization of a grating coupled twin waveguide laser, where the two waveguides are the active laser waveguide and a passive waveguide formed by Au/SiO/SiN. The waveguide are coupled via a surface relief grating atop of the semiconductor (Fig. 3). These lasers allow postprocessing wavelength adjustment and high side mode suppression [6].

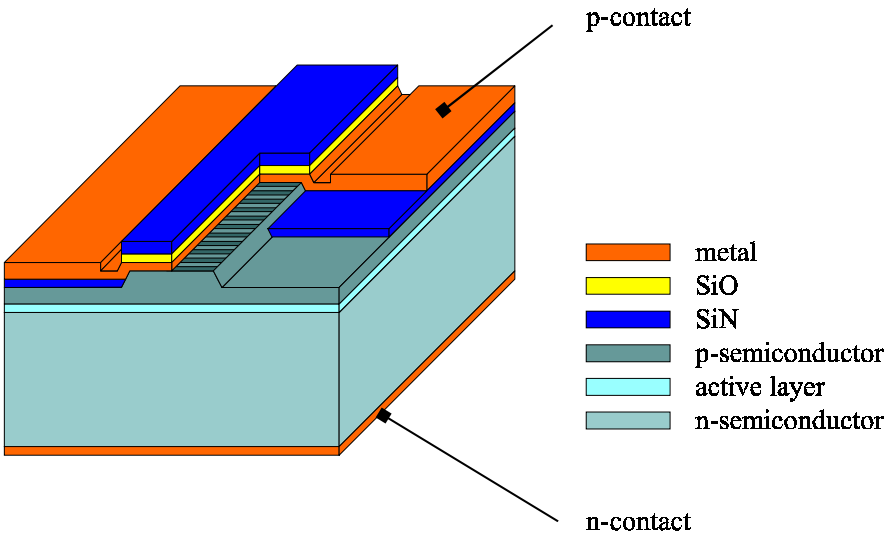

Fig. 3: Twin waveguide laser schematic.

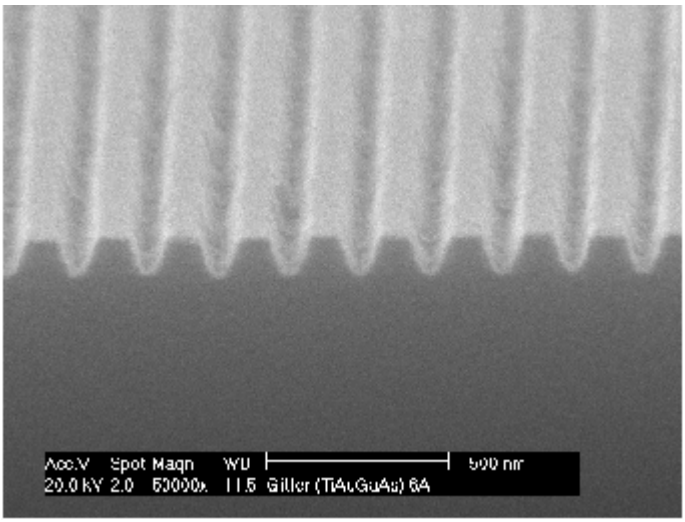

Fig. 4: SEM picture of 190 nm period grating etched into GaAs (photoresist removed)

The use of diluted photoresist (thickness 50 nm) allows us to produce grating periods as small as 180 nm holographically with a HeCd laser (lower limit for grating period:

325 nm/2 = 162.5 nm) in standard resist material. The used InGaAs QW laser material for the twin waveguide laser is designed for emission at about 980 nm, thus needing a grating period of about 190 nm, which is accessible with our setup as shown in Fig. 4.

2.2 Laser interferometer

The realization of a laser interferometer, consisting of a VCSEL and a detector integrated on one chip is the final goal of this project. At the beginning, Bragg mirrors consisting of GaAs and AlAs layers were grown and characterized by reflection measurement and layer thickness measured by scanning tunneling microscope (Fig. 5).

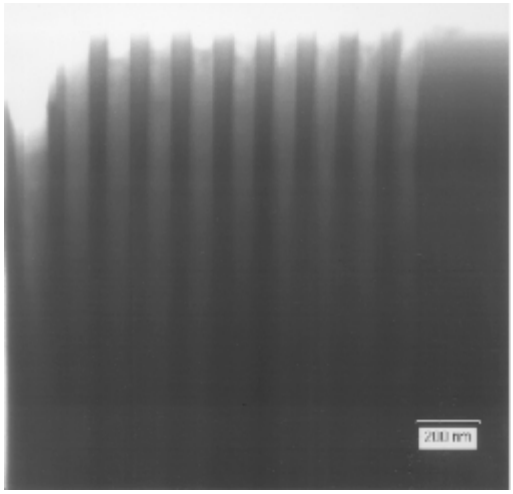

Fig. 5: STEM picture of AlAs/GaAs Bragg mirror.

The first VCSEL structures we realized consist of an upper dielectric Bragg mirror – made of SiO/SiN in a PECVD (plasma enhanced chemical vapor deposition) system – deposited on an MBE grown active region and a lower AlGaAs/AlAs Bragg mirror. These lasers showed single mode emission at room temperature but relatively broad linewidth [7]. Improvements are achieved by using a selective oxidation technique to reduce problems with current spreading and QWs as active region.

3. Conclusion

We started the growth of AlGaAs/GaAs bandgap lasers and were able to realize DH structure laser, strained InGaAs QW lasers and VCSELs which are state of the art, and in the near future we are going to realize new single mode lasers and an integrated laser interferometer.

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Far-Infrared Electroluminescence in Parabolic Quantum Wells

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We have measured the far-infrared emission from parabolically graded quantum wells driven by an in-plane electric field in the temperature range from 20 K to 240 K. The peak emission corresponds to the intersubband plasmon in the parabolic potential. Its photon energy (6.6 meV / 9.8 meV) remains rather unaffected by temperature variations, the full width at half maximum ranges from 1 meV (T = 20 K) to 2 meV (T = 240 K). The reduction of emission efficiency with increasing temperature is attributed to the change in the non-radiative lifetime.

1. Introduction

The need for solid state far-infrared sources operating without a magnetic field has stimulated the research on intersubband electroluminescence in semiconductor heterostructures. Experiments have been performed on parabolic quantum wells [1], on superlattices [2], and more recently on quantum cascade structures [3], [4].

Parabolically graded quantum wells are promising candidates for far-infrared sources operating above liquid nitrogen temperature. The large temperature-induced variation of the electron distribution is expected to have little impact on the emission performance. In accordance with the generalized Kohn´s theorem [5] the emission frequency is independent of the electron distribution and concentration in the well. In absorption and emission spectroscopy coupling between the radiation and the electron system has been observed at only one frequency [6], [1]. This is the harmonic oscillator frequency, solely determined by the width and the energetic depth of the quantum well. Here, we demonstrate the stability of the intersubband emission in a parabolic quantum well up to a temperature of 240 K [7].

2. Experimental

Two samples were examined: one with 140 nm, the other one with 200 nm well width, both with 167 meV energetic well depth. Figure 1 shows the layer structure and the device geometry of the 140 nm well sample schematically. The samples were grown by molecular beam epitaxy, depositing alternate layers of $Al_{0.3}Ga_{0.7}As$ and GaAs on a semi-insulating GaAs substrate. By adjusting the ratio of the layer thicknesses, the average Al-content in the well region is parabolically graded from x = 0 to x = 0.2. The well is sandwiched between $Al_{0.3}Ga_{0.7}As$ spacer layers and remotely doped. The sample was contacted with two parallel AuGe Ohmic contact stripes. In order to couple out the in-

tersubband radiation that is polarized with its electrical field perpendicular to the layers a metallic CrAu grating was evaporated between the contacts. A more detailed description of the 200 nm well sample had been given elsewhere [1].

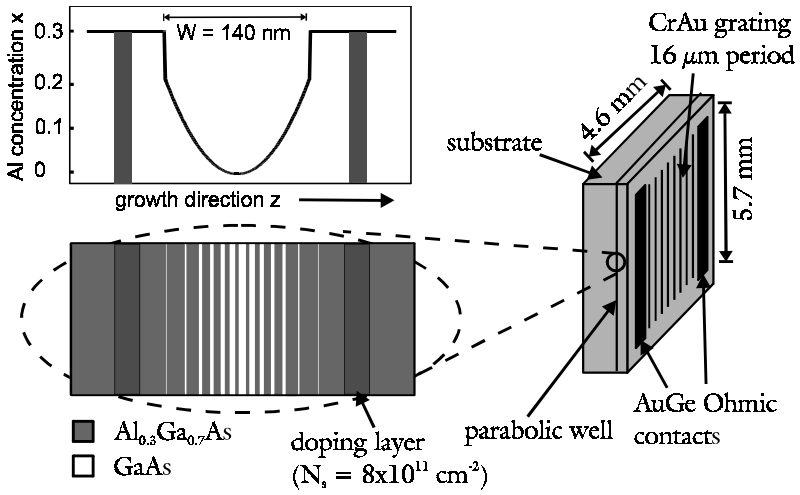

Fig. 1: Layer structure and sample geometry of the 140 nm well sample.

We measured the electroluminescence using a Fourier-transform infrared spectrometer in step scan /lock-in mode with a spectral resolution of 0.5 meV. The sample was mounted on the cold finger of a helium-flow cryostat. The emitted radiation was collected by an off-axis parabolic mirror, transmitted through the spectrometer, and then focussed on a helium cooled Si bolometer. The whole beam path was purged with dry nitrogen gas to minimize the far-infrared absorption of water vapor. In order to excite the electron gas a pulsed electric field at a frequency of 411 Hz and 50 % duty cycle was applied between the Ohmic contacts.

3. Results

In Fig. 2 a, spectra of the 200 nm well at various temperatures are displayed. The peak emission is observed at a photon energy of 6.6 meV for all temperatures. This value corresponds to the harmonic oscillator energy calculated from the well dimensions as 6.0 meV. In agreement with the generalized Kohn´s theorem, the emission energy is unaltered by the temperature-induced variation of the electron distribution in the well. The spectra of the 140 nm well in Fig. 2 b show a 20 K emission peak at 9.8 meV (calculated as 8.4 meV) that is slightly shifted to lower energies (9.1 meV) as the temperature is raised to 240 K. The full width at half maximum of the emission line of both samples ranges from 1 meV at low temperatures to 2 meV in the high temperature regime ($T > 100$ K). The temperature dependence of the optical power collected by the bolometer P_{co} of both samples is depicted in the inset of Fig. 2. It was determined as the integrated area of the emission spectra divided by an amplification factor and the bolometer responsivity.

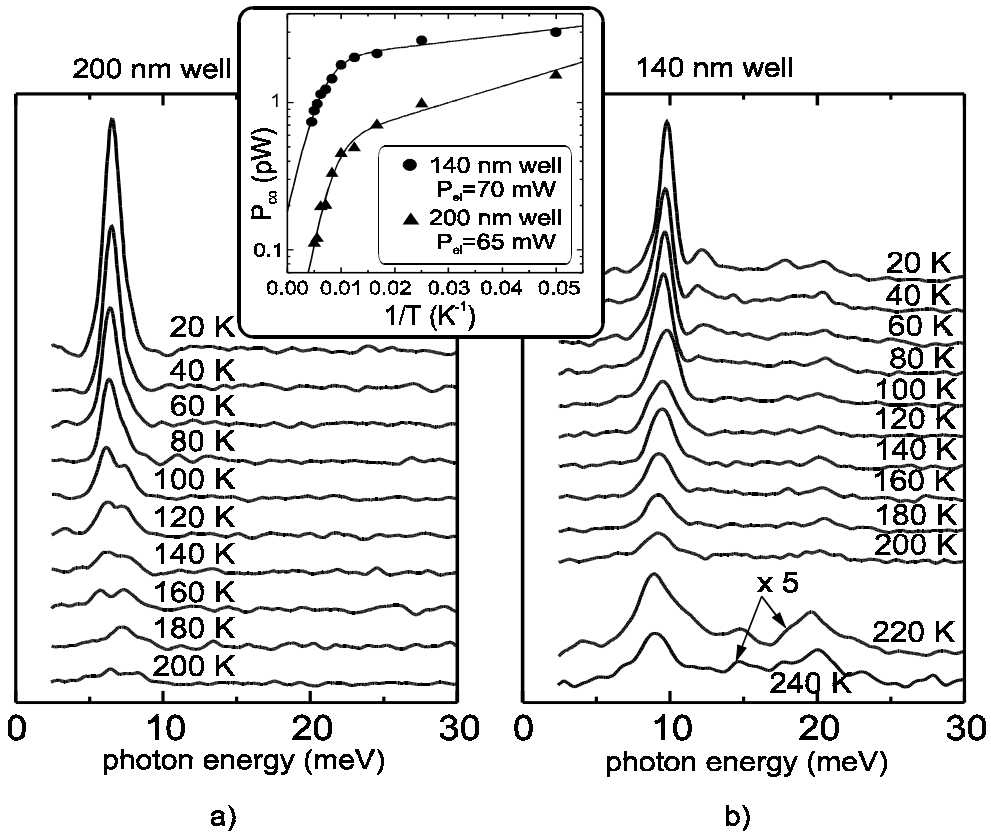

Fig. 2: Emission spectra of the two samples for various temperatures as indicated. The inset shows the dependence of the collected optical power P_{co} on the inverse temperature 1/T.

The collected optical power Pco is assumed to depend on the electrical input power P_{el} and on the ratio of non-radiative lifetime τ_{nr} and radiative lifetime τ_r (in case of $\tau_r >> \tau_{nr}$) like

$$P_{co} \propto P_{el} \frac{\tau_{nr}}{\tau_r} .$$

The proportionality between the collected optical power P_{co} and the electrical input power P_{el} has been confirmed up to ~70 mW, above which saturation occurs. The difference in the optical power P_{co} between the two samples can be qualitatively understood by looking at the radiative lifetime τ_r. It was calculated in the model of a classical electron oscillator as 59 µs for the 140 nm well and 130 µs for the 200 nm well. With the simplifying assumption of similar non-radiative lifetimes, grating-coupler efficiencies and excitation efficiencies, one would expect the optical power P_{co} of the 140 nm well sample to be approximately twice the one of the 200 nm well sample at comparable electrical input powers P_{el}.

The decrease of (collected) optical power is induced by a thermally activated process. The solid lines in the inset of Fig. 2 are fits of the inverse sum of two exponential functions in 1/T yielding activation energies of E_1 = 34 meV, E_2 = 0.8 meV for the 140 nm well sample and E_1 = 41 meV, E_2 = 2.2 meV for the 200 nm well sample. The higher energy E_1 is probably the activation barrier for the emission of optical phonons. The intersubband transition rate $1/\tau_{nr}$ shows a similar behavior of thermal activation, as de-

scribed by Heyman et al. [8]. We may deduce that the temperature dependence of the optical power is governed by the non-radiative lifetime τ_{nr}. At temperatures above ~100 K, the emission of optical phonons limits the optical power.

4. Conclusion

We have demonstrated electrically driven far-infrared emission of parabolic quantum wells up to a temperature of 240 K. At high temperatures, the thermal energy k_BT exceeds the photon energy by a factor greater than two. Despite of the large temperature related shift of the electron distribution, we observe single frequency emission, and the impact of high temperatures on the frequency and the line shape is small. The emission efficiency is limited by the temperature dependent decrease of intersubband lifetime.

Acknowledgements

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High Frequency Devices

Development of a SiGe BiCMOS Process for ASIC Applications

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1. Introduction

As one of the leading ASIC producers in Europe Austria Microsystems Int. AG has entered the area of high frequency capable processes with introducing a BiCMOS platform in 1993. Today BiCMOS technology comprises 1.2µm, 0.8µm, and 0.6µm processes with a wide range of design features. Based on this platform, Austria Microsystems Int. AG has developed in cooperation with SiGe Microsystems Technology Inc. a SiGe based HBT BiCMOS platform. The HBT process is now in its final stage with qualification, and multi project wafer access is available in mid-1999.

2. Key Design Features of the BiCMOS Process

- N and P buried layer with epi-silicon layer;
- Deep sinker;
- Fast poly-silicon Emitter NPN bipolar transistors (F_T 8 / 12 / 16 GHz);
- Lateral PNP transistors;
- Various resistor types poly resistors: 20 Ohm / 70 Ohm / 1.2 kOhm;
- Poly 1 to sinker capacitors;
- High capacitance poly-poly capacitors (up to 1.75 fF/µm²);
- F_T 16 – 18 GHz (0.6µm process);
- CMOS design compatibility;
- well characterized metal inductors.

In order to go beyond 18 GHz reached in conventional Si-technology AMS started to develop in cooperation with SiGe Microsystems a silicon-germanium process (heterojunction bipolar transistor) targeting at F_T, F_{max} > 30 GHz [1].

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[1] F_{max}: frequency at which unilateral power gain drops to unity;
F_T: frequency at which beta drops to unity when no load is connected to collector

$$F_{max} = \left[\frac{f_t}{8 * \pi * R_B * C_{BC}} \right]^{1/2}$$

R_B … Base resistance ; C_{BC} … collector/base junction

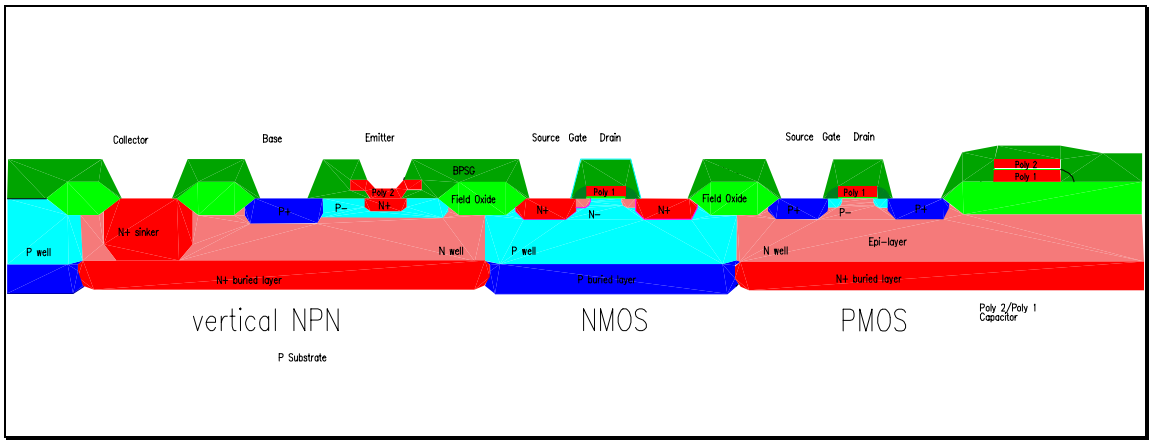

Fig 1: Schematic cross-section of BiCMOS process

Inherent to the operation of bipolar junction transistors (BJT) is the requirement of a low doped base to achieve high current-gain values. A low doped base on the other hand is in conflict with a good HF performance of the device. This contradiction can be resolved by the heterojunction bipolar transistors (HBT). In HBTs the effective doping concentration in a high doped base is kept low by means of the increased intrinsic carrier concentration caused by the bandgap difference between Si and SiGe. This yields an increased collector current (→ increased beta) compared to BJTs.

$$J_C = \frac{\mu q k T}{\int_x^W \frac{N_A(x)}{n_i^2(x)}\,dx} * \exp\left(\frac{qV_{BE}}{kT}\right) \qquad \text{(Moll–Ross relation)}$$

n_i^2 ... intrinsic carrier concentration

N_A ... base doping

The integration chosen follows a drift transistor approach where the germanium concentration increases linearly (graded Ge profile) from the emitter/base to the base/collector junction (Fig. 2). This concept results in a reduced base transit time which is the major component in the in the transistor delay terms. The graded Ge profile shows an improved Early voltage compared to HBTs with constant Ge profile through out the base (true HBT) whereas the true HBT concept is superior in current gain.

Since the Austria Microsystems Int. AG BiCMOS technology has been well acknowledged by various customers it was imperative to keep the changes in process flow to a minimum when integrating the HBT module in order to guarantee constant process parameters. The integration of SiGe stack could be accomplished with two additional masks compared to the standard BiCMOS platform.

To give an example of the optimization work in the development process I will focus on the collector/base junction. The base collector depletion-zone transit time (τ_{BC}) is for high speed transistors a decisive delay factor. To keep its value small a high collector doping (N_D) is needed. This is contrasted by the necessity of a low N_D to reduce the base/collector capacitance. A high breakdown voltage of the base/collector junction asks for a low doped collector. Optimizing this problem under the given constraints is best done by a pedestal collector implant (SIC) giving F_{max} values around 30 GHz.

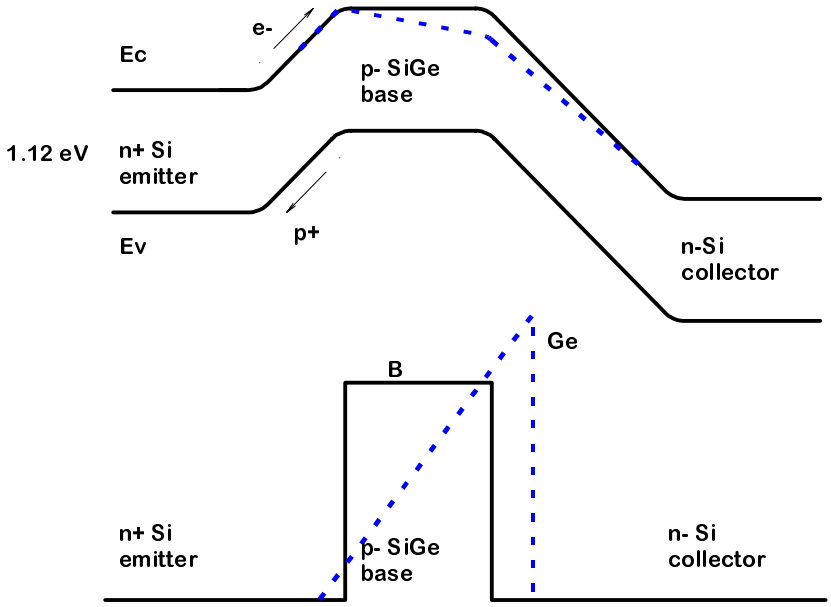

Fig. 2: Band structure diagrams of a conventional Si-NPN bipolar transistor and a modified bandgap of a SiGe NPN-HBTs. The implementation of a graded SiGe-layer reduces the bandgap and leads to a drift acceleration of the electrons.

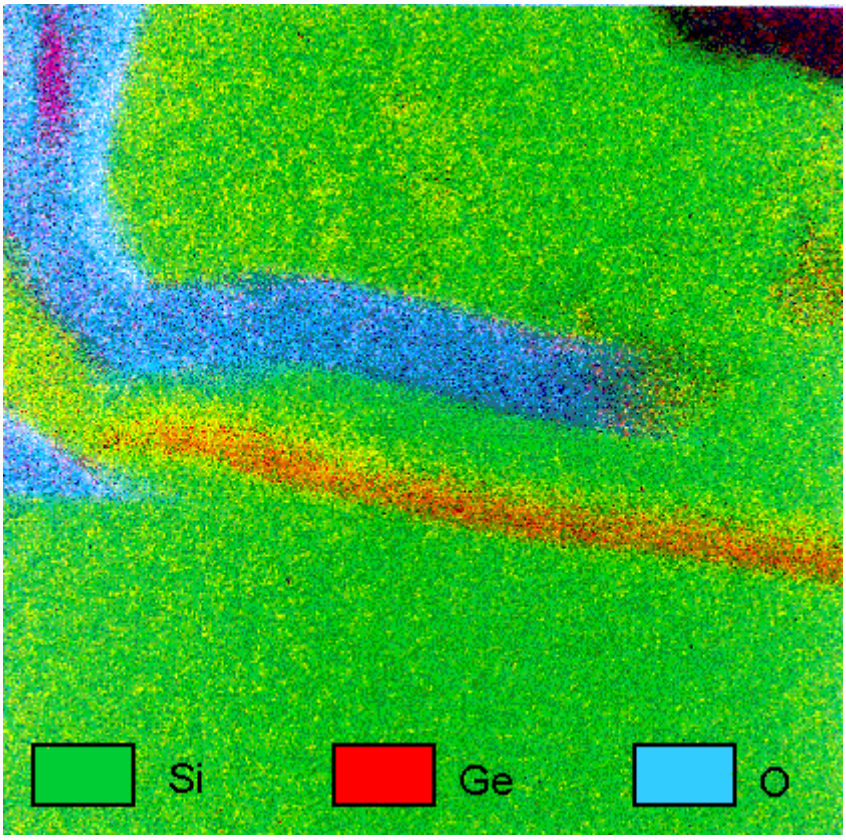

Fig. 3: Transmission electron microscope (TEM) picture with electron energy loss (EELS) analyzer. The picture shows the germanium enriched area in the base.

Trade-offs at collector/base junction:

⇑ ... high ⇓ ... low

⇓	τ_{BC}	→	N_D	⇑		
⇓	C_{BC}	→	yields high F_{max}	→	N_D	⇓
⇑	BV_{CBO}	→	N_D	⇓	Ionization in Si (”wide gap material”)	
⇒	optimized	**Selective Implanted Collector (SIC)**				

Tab. 1: Trade-offs at collector/base junction.

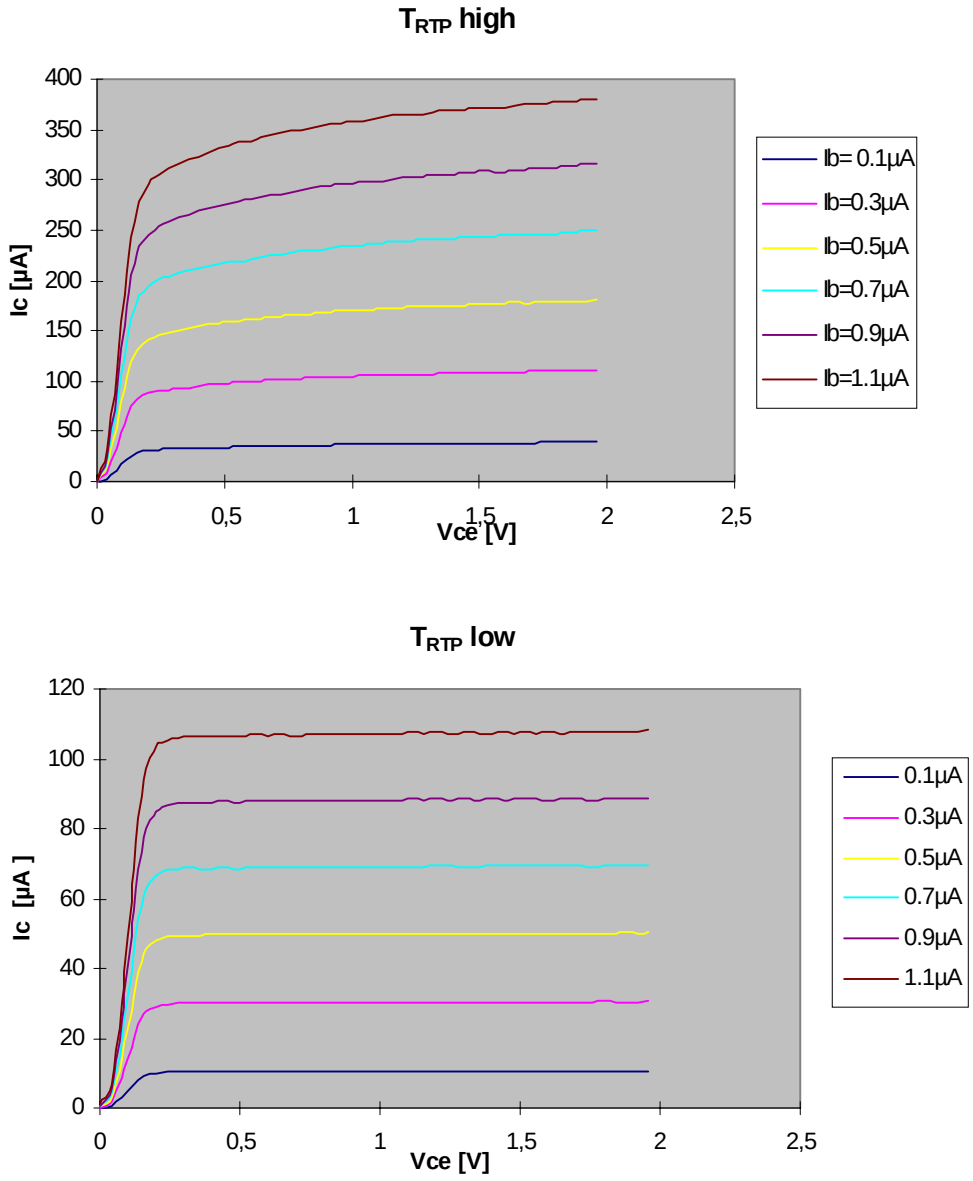

Fig 4 : Shows the dependence of output characteristics Ic vs. Vce on thermal stress (T_{RTP}) due to processing. Note the change in Early voltage.

An other crucial design issue is the alignment of the boron and the germanium profile in the base. Misalignment leads to degradation in device performance seen in a ruined Early voltage and current gain variations. These problems are cured by stringent control over the thermal budget seen by the wafer during processing (Fig. 4).

As a result of this integration a HBT BiCMOS process has been developed and brought to production maturity. This process features all standard BiCMOS process elements like full CMOS design compatibility, various poly resistors, high capacitance poly/poly capacitors, a.s.o. together with SiGe based drift HBTs with F_T's of 30 – 40 GHz, F_{max} of 25 – 35 GHz, low base resistance, and high Early voltage.

State and Applications of Si/SiGe High Frequency and Optoelectronic Devices

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The turnover of microelectronic devices and circuits has been rapidly growing from $ 45 billion in 1990 to $ 77 billion in 1993 to about $ 350 billion in the year 2000. Since silicon (Si) is the overwhelmingly dominating material in this market with an over 97% share there has been a great incentive to develop the silicon/germanium (SiGe) heterodevices due to their superior performance compared to conventional Si devices and due to their full compatibility with the widespread and mature Si technology. Accessible market shares will depend on cost/performance advantages, therefore SiGe heterobipolar transistors (HBT's), SiGe hetero-field effect transistors (HFET's), and SiGe hetero CMOS (HCMOS) circuits are very competitive devices which fit best into the respective Si markets. We report here about performance of SiGe HBT's, MODFET's and IR detectors, about relevant circuit applications, and in the last section we give some forecasts for SiGe in the RF market.

1. Introduction

The strong research activities worldwide in the recent past in growing and processing reproducibly and commercially silicon/silicon-germanium (Si/SiGe) heterostructures (even on an atomic scale) has turned out Si based devices which can be grown by MBE, LPCVD, or UHVCVD. The performance of these devices, such as the SiGe base heterobipolar transistor (HBT) and the SiGe modulation doped field effect transistor (MODFET) or HEMT (high electron mobility transistor), is superior compared to their Si based counterparts, which substantially broadens the performance and functionality spectrum of Si microelectronics.

The potential of SiGe heterostructure devices has already been demonstrated by many University groups and companies, such as DaimlerChrysler, GEC, Hitachi, Intel, NEC, Siemens, TEMIC, SGS Thompson. Today the chip manufacturers come into play and also system partners are included. The focus of activities has now shifted from single devices to circuits. In this paper we describe briefly the basic principles of opto- and microelectronic SiGe heterostructure devices and circuit applications, finally we give a short overview on the expectations for SiGe microelectronic devices in the RF market.

2. SiGe Microelectronic Devices

Silicon based HBT's are npn bipolar transistors with a thin (<50 nm) pseudomorphically grown $Si_{1-x}Ge_x$ alloy layer as the base. High Ge contents up to 50% can be incorporated, and compared to standard Si BJT's (bipolar junction transistors), the base may be as thin as 5 to 10 nm, which helps to decrease the base transit time and raises the cut-off frequency of the transistor. In addition, the doping in the base may be extremely

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high, above 10^{20} cm^{-3}, which reduces the base sheet resistance. The highest maximum oscillation frequency f_{max} from an HBT has been achieved with a base sheet resistance below 1 kΩ/ .

The DC performance of a SiGe HBT is basically governed by the high current gain due to suppressed hole re-injection because of emitter-base valence band offset [1]. This is elucidated by the Gummel plot in Fig. 1 showing the current gain as a function of emitter-base voltage from a passivated SiGe HBT coming out from a production line.

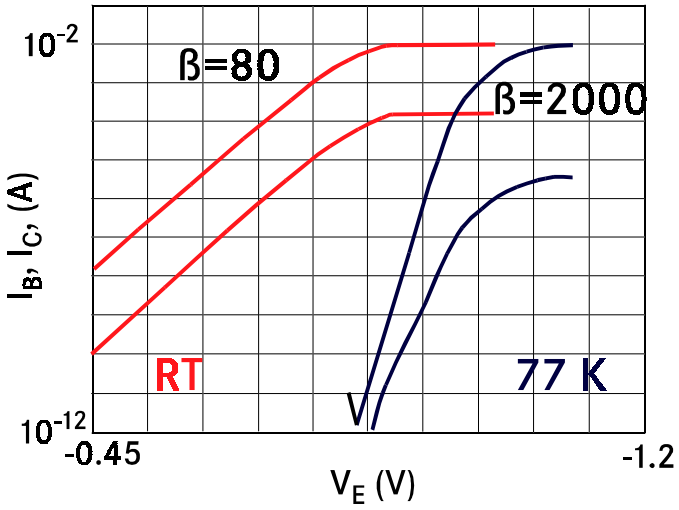
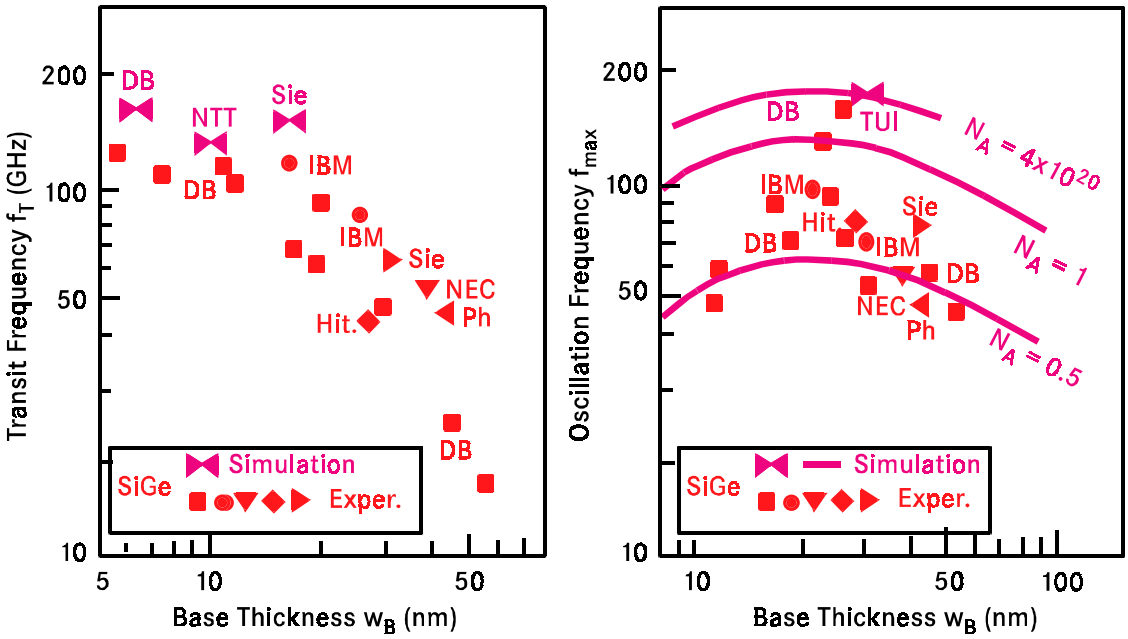


Fig. 1: Gummel plots of SiGe HBT's at room temperature and 77 K from a passivated SiGe HBT from a Si production line (TEMIC).



(a) (b)

Fig. 2: Transit frequencies (a) and maximum oscillation frequencies (b) of SiGe HBT's, measured by various labs (N_A = 0.5x10^{20} cm^{-3} resp. 4x10^{20} cm^{-3}).

Nearly constant current gains over 9 decades are observed with a high gain value β of 2000 at 77 K (80 at RT). The application potential for "high β" HBT's for low noise amplifiers in the lower GHz range which can further raise the dynamic input resistance is presently not exploited. The high frequency properties of various SiGe HBT's are summarized in the transit and maximum oscillation frequency (f_t and f_{max}) plot versus base thickness for various companies (DaimlerBenz, Hitachi, NEC, Siemens, Philips, TEMIC) shown in Fig. 2 [2] – [4]. Record values of f_t of 116 GHz and f_{max} of 160 GHz have been achieved by the DaimlerChrysler Research group with base thicknesses of 7 and 37 nm. The maximum transit frequencies at lower base width result also in lower f_{max} values due to the distinctly higher base resistance. The f_t/f_{max} ratio depends strongly on the collector design. A thin, heavily doped collector favors higher f_t values. Today HBT's with equal f_t and f_{max} of about 70 – 80 GHz can be fabricated. The frequencies increase with collector current up to a rapid fall off attributed to the Kirk effect which can be also seen for passivated devices [5], [6]. By increasing the collector/emitter voltage V_{CE} f_{max} can be furthermore increased due to reduction of the collector/base capacitance [5].

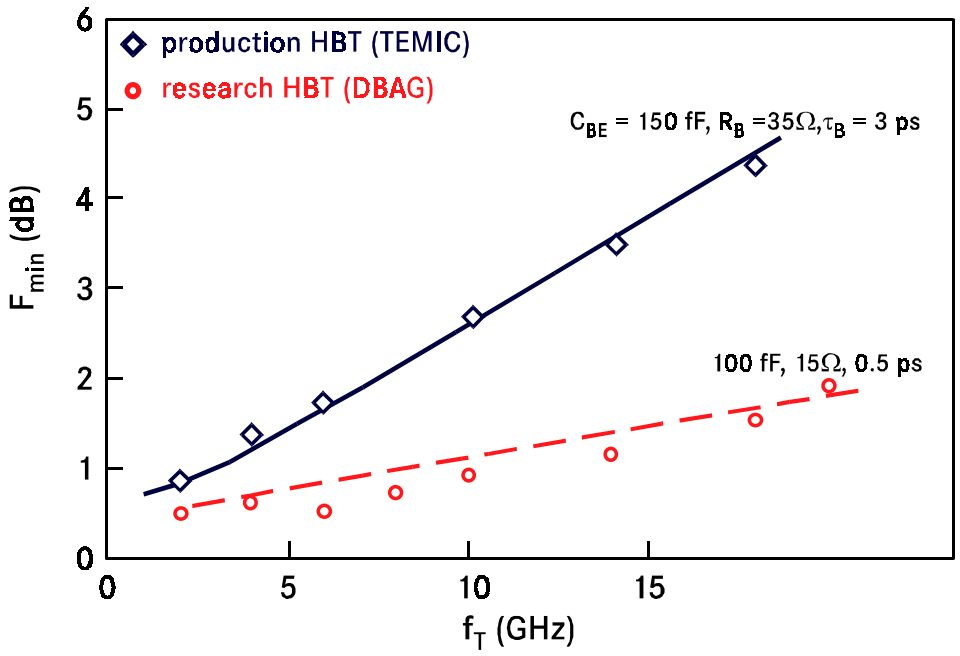


Fig. 3: High frequency noise of mesa chip HBT's and packaged HBT's. Simulated influence of base-emitter capacitance, base resistance and base transit time.

Another figure of merit is the high and low frequency noise. Fig. 3 compares the noise figure F_{min} for frequencies above 2 GHz for research HBT's and for marketable packaged HBT's (in SOT 343 or 143) [7], [8]. The noise figure from a production line HBT is still below 1 dB at 10 GHz which can be seen in Fig. 3 which compares the noise figures of a research mesa HBT with a planar passivated production HBT. The corner frequency f_C, which marks the transition point from 1/f noise to the shot noise is below 300 Hz, even for packaged HBT's [8], [9]. The Gummel plot gives an idea of the size of f_C as shown in Fig. 4. Parallel collector and base currents guarantee low corner frequencies below 1 kHz.

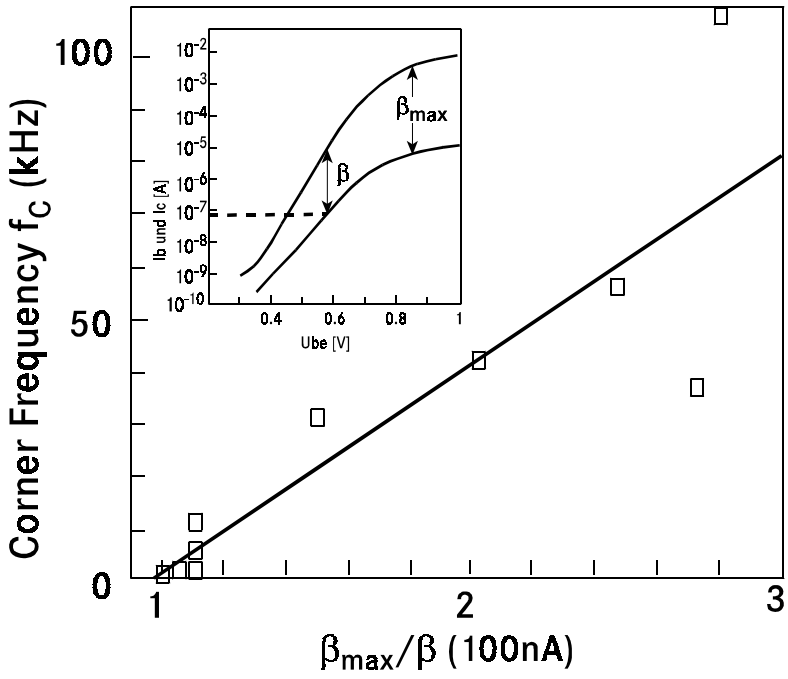


Fig. 4: Corner frequency related to the non-ideality of the Gummel plot (ratio of gain at high and low currents).

Si/SiGe power HBT's intended for 1.9 GHz applications either using 60 emitter fingers exhibited a collector/emitter breakdown voltage of 4.5 V with f_T and f_{max} values of 16 and 11 GHz, respectively, at a collector current of 400 mA. Class A power added efficiencies (PAE) of 44% at 1 W output power and PAE's of 72% at 900 MHz for class A/B operation have been measured. These data are achieved without any thermal shunt precautions in the contacts and without substrate thinning, which reflects the benefits of a Si substrate.

3. Si/SiGe HFET's

The band alignment of the Si/SiGe heterostructure favors the creation of carrier channels by modulation doping (carriers separated from dopant atoms). In a SiGe MODFET high carrier mobilities of 2900 cm^2/Vs and 1800 cm^2/Vs result for the two-dimensional electron or hole gas respectively [10], [11] and sheet carrier concentrations up to $2.5x10^{12}$ cm^{-2}. This also holds true in the case of a hetero MOSFET when the channel is buried under the gate and the interface scattering is strongly reduced due to the more perfect Si/SiGe interface. In addition, an increased velocity overshoot has been predicted due to the strain in the channels [12].

Figure 5 compares the DC performance of good n-HFET's, all of them with Schottky gates. The operation mode – depletion or enhancement – can be chosen by adjusting the doping in the supply layers above or below or even within the channel and by the layer thickness, e.g. cap layers above the channel. A gate recess, for example, can switch enhancement mode to depletion mode. Record values for extrinsic transconductances in depletion HFET's from 290 to 310 mS/mm at RT have been measured for depletion n-HFET's and 480 to 510 mS/mm for enhancement FET's at RT and up to 780 mS/mm at 77 K. Transconductances of p-HFET's are usually smaller (e.g. around 250 mS/mm for 0.2 – 0.25 µm gate length). However, theory predicts values similar to n-HFET's when

using a Ge channel in the p-HFET [12]. High currents of 320 and 200 mA/mm have been obtained for depletion or enhancement mode n-HFET's and currents up to 600 mA/mm have been obtained for MOS gated p-HFET's (3,7 nm SiO_2).

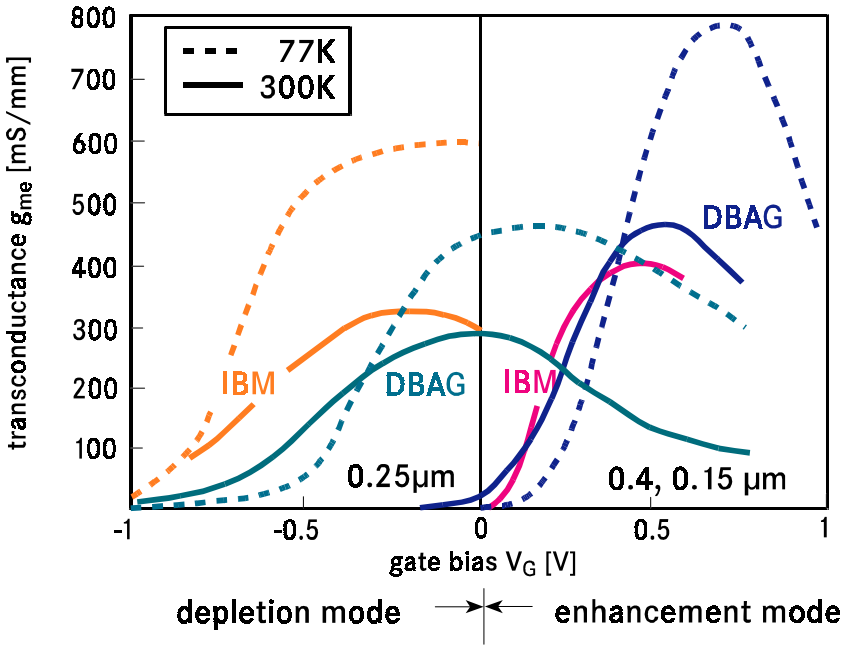


Fig. 5: Transconductances at room temperature and 77K of depletion and enhancement mode SiGe HFET's.

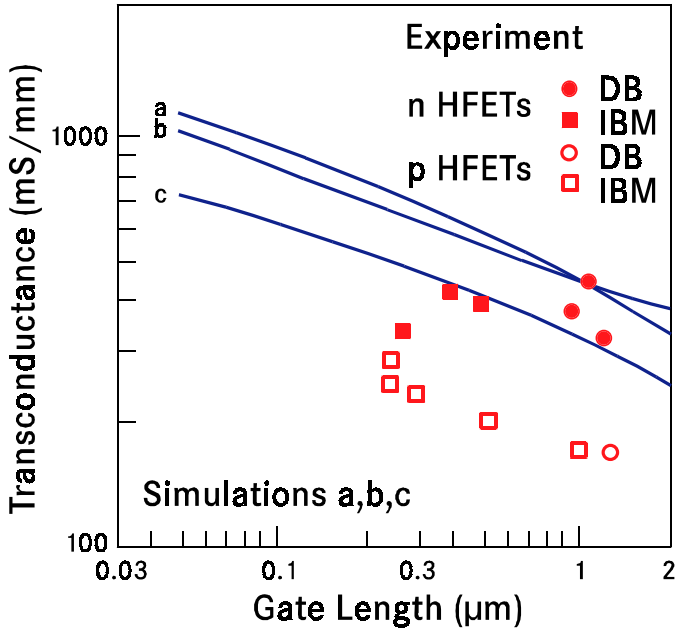
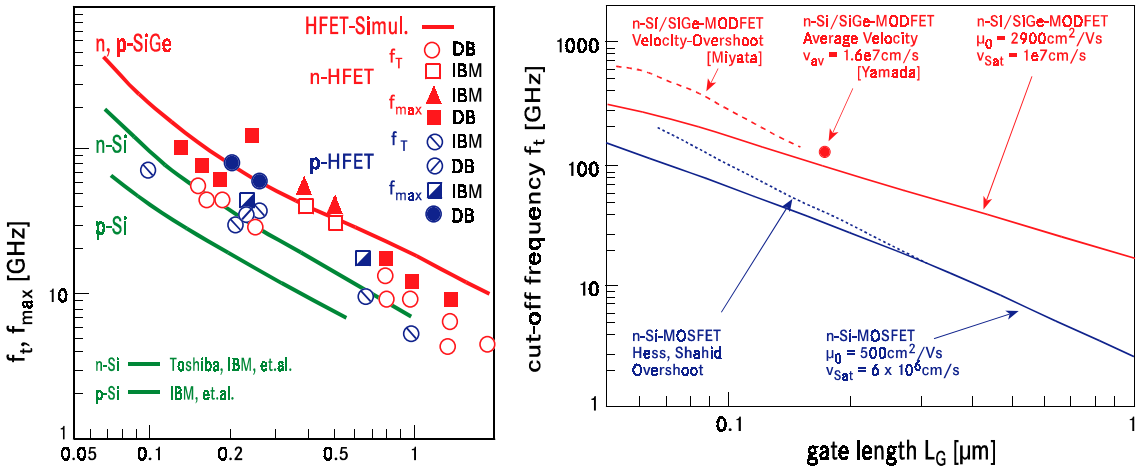


Fig. 6: Gate length dependence of the transconductance of n-HFET's. Experimental data reported compared to simulations.

Figure 6 makes a comparison of the transconductance status with expectations. Experiments have not established the significant gate length dependence (a, b, c) expected from theory [12]. Cut off frequencies f_{max} of 78 to 92 GHz and f_T of 43 to 46 GHz had been extrapolated from the gain curves. The lower drain source voltage V_{DS} of the order of 1V for voltage independent operation underlines the low power potential in digital circuits of SiGe HFET's.



(a) (b)

Fig. 7: Gate length dependence, (a) measurements of n- and p-type HFET's and (b) simulations for n-SiGe HFET's with and without velocity overshoot [15].

In Fig. 7, most of the frequencies f_T and f_{max} achieved so far for n- and p-HFET's are plotted versus gate length [13], [14] from IBM and our group. The gate length dependence of the cutoff frequencies are clearly visible, simulation predicts maximum cutoff frequencies of up to 200 GHz for gate length below 0.1 µm or even higher (>400 GHz) if velocity overshoot really exists [12], [15]. On the other hand, HFET devices with a relaxed gate layout of 0.35 to 0.8 µm have a better performance than Si MOSFET's and benefit from the manufacturability in a standard Si MOS production line.

4. Circuit Applications Using SiGe HBT's and HFET's

Presently the HBT is the best developed SiGe device, and it is an ambitious and time consuming goal to implement such a new technology into the well established Si production line of a chip manufacturer. By now those circuits are commercially available (*PA U7004B* from TEMIC) but so far mainly for special system customers with whom the chip manufacturer cooperates.

Various HBT circuits have been reported so far with promising performances. Figure 8 shows a chip with circuits for 5 to 40 GHz operation realized on semi-insulating substrate. A 12 bit digital to analog converter operating at 1 GHz has been demonstrated by IBM together with ADI [16]. NEC has reported an D-type flip-flop for 20 Gbit/s, a selector for 30 Gbit/s and 33ps, a 2:1 multiplexer for 20 Gbit/s and preamplifier with 19 GHz and 36 dbΩ [17]. Furthermore a multiplexer and a demultiplexer with 28 Gbit/sec have been realized by the Ruhr University Bochum using our samples. A wideband amplifier capable of 9.5 dB gain with 18 GHz bandwidth and a power consumption of 50 mW from a 3 V supply which operates at 1.6 V has been realized [18]. Varactor

controlled oscillators with Si/SiGe HBT's for different frequency ranges from 1.8 up to 40 GHz were presented by Nortel together with IBM, by TEMIC, and by IBM [19], [20]. Power amplifiers for 0.9 up to 2 GHz have been realized by TEMIC together with our group (DCAG) [21] and by Philips; LNA's with an F_{min} of 1.7 to 1.9 dB have been presented by TEMIC (with DCAG and University of Ulm) and by IBM. A frequency divider of 42 Gbit/sec and a 60 Gbit/sec demultiplexer were recently realized by Siemens [22], [23]. The large scale integration (LSI) potential has been demonstrated by the fabrication of arrays with small SiGe HBT's with more than 1000 and up to 30000 devices. SiGe HBT's are nowadays also used for hybrid integration. An active antenna for a 5 – 8 GHz receiver with the excellent noise figure of 1.4 dB was reported by the University of Ulm with a SiGe HBT from us [24]. Excellent low phase noise in a 4.7 GHz oscillator has been demonstrated with –135 dBc at 10 kHz offset from carrier, another HBT had –115 dBc at 10 kHz off. Finally dielectric resonator oscillators (DRO) for 4.7 and 10 GHz and an 8 – 12 GHz VCO have been reported by DCAG together with Dornier and CNET [25], [26].

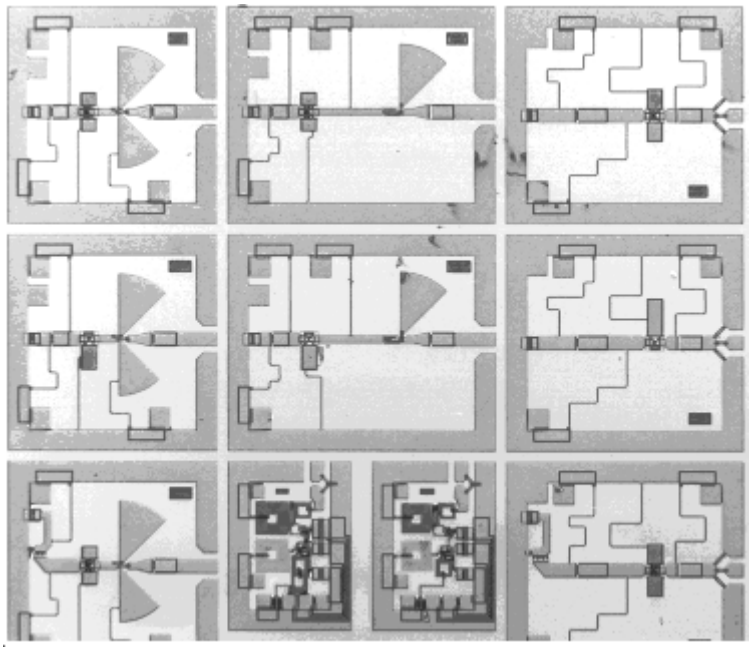
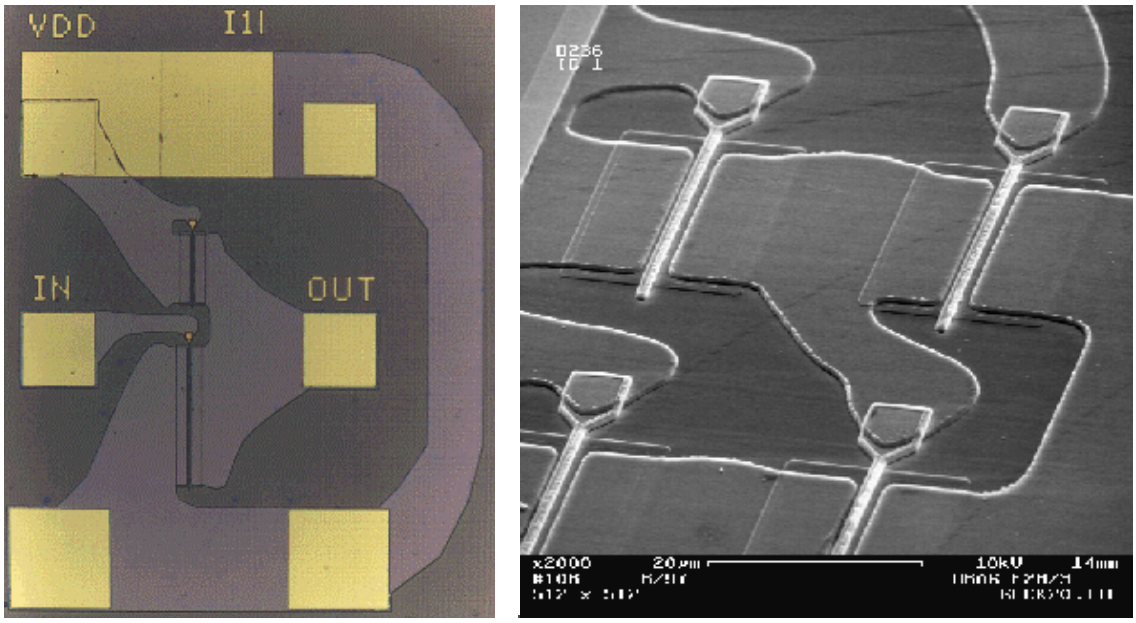


Fig. 8: SiGe HBT chip with circuits for 5 – 40 GHz

HFET circuits are far less developed. Digital and analog demonstrators are under investigation. A digital chip contains ring oscillators, inverters (shown in Fig. 9a) and level shifters (Fig. 9b). The chip technology is based on e-beam gate writing from 0.8 µm down to 0.15 µm and on two interconnect levels [27]. Very recently we have realized an transimpedance amplifier of 56 dBΩ with a –3 dBΩ frequency of 1.8 GHz. Circuits with sputter oxide passivation yield a higher transimpedance of up to 72 dBΩ with 1 GHz bandwidth. The great potential, however, lies in the integration of n-HFET's with p-HFET's to a new generation of hetero-CMOS circuits. SiGe hetero-CMOS enables the same mobility and velocity for both types of HFET's with equal geometry. Modular circuit concepts allow the integration of HFET circuits with standard VLSI-CMOS. The technology starts with conventional CMOS process including the poly gate, leaving blank areas for the heterodevices. Then the HFET processing (low temperature Si/SiGe epitaxy and oxide deposition, patterning) follows. The HCMOS circuit is then

reintroduced into the CMOS lines and receives the final metallization and passivation steps. The flexibility of such a concept has experimentally already been checked [28].



(a) (b)

Fig. 9: (a) Inverter circuit with a resistor as load and an n-type depletion MODFET as driver [27]; (b) level shifter with n-HFET's.

The chances for a SiGe HFET circuit fabrication are high. When the SiGe technology is implemented in Si IC factories, this infrastructure may be used for HFET circuits too. The strongest technological challenge for the future remains the realization of the ideal SiGe hetero CMOS concept. The current problems with the p-HFET technology has to be overcome with low thermal budget oxides and with defect densities related to the buffer layers. However, the outstanding performance perspectives justify the effort.

5. SiGe Optoelectronic Devices

The vision of an integrated optical circuit on a Si wafer for fiber optical communication requires Si based emitter and receiver device functions as key devices which can be monolithically integrated on a Si IC chip with e.g. a CMOS electronic driver circuit. A possible realization of interchip and intrachip coupling on a Si substrate via Si/SiGe light emitting and receiving devices can be seen in Fig 10. Figure 10 (a) depicts the distribution of an optical clock signal from an external laser via (patterned or diffused) Si waveguides to different detectors on the same chip, Fig.10 (b) shows schematically a Si based LED distributing signal via different Si waveguides, transmitting it in free space and collecting it in different waveguides on the next chip. A great impact to this field has been given by the realization of the first short-period strained layer Si_mGe_n superlattice light emitting diode which exhibited room temperature electroluminescence in the near infrared (1.3 µm) [29]. Later on room temperature electro- and photoluminescence has been measured from strained Si/SiGe quantum well layers [30]. About the same time good SiGe photodetectors with external efficiencies of $\eta \approx 12\%$ and response times of 400 nsec became available [31]. In addition, other passive optical device func-

tions such as modulators and interferometers with SiGe waveguides have been realized on Si substrates [32] which are necessary for an integrated optical and electronic circuit on Si.

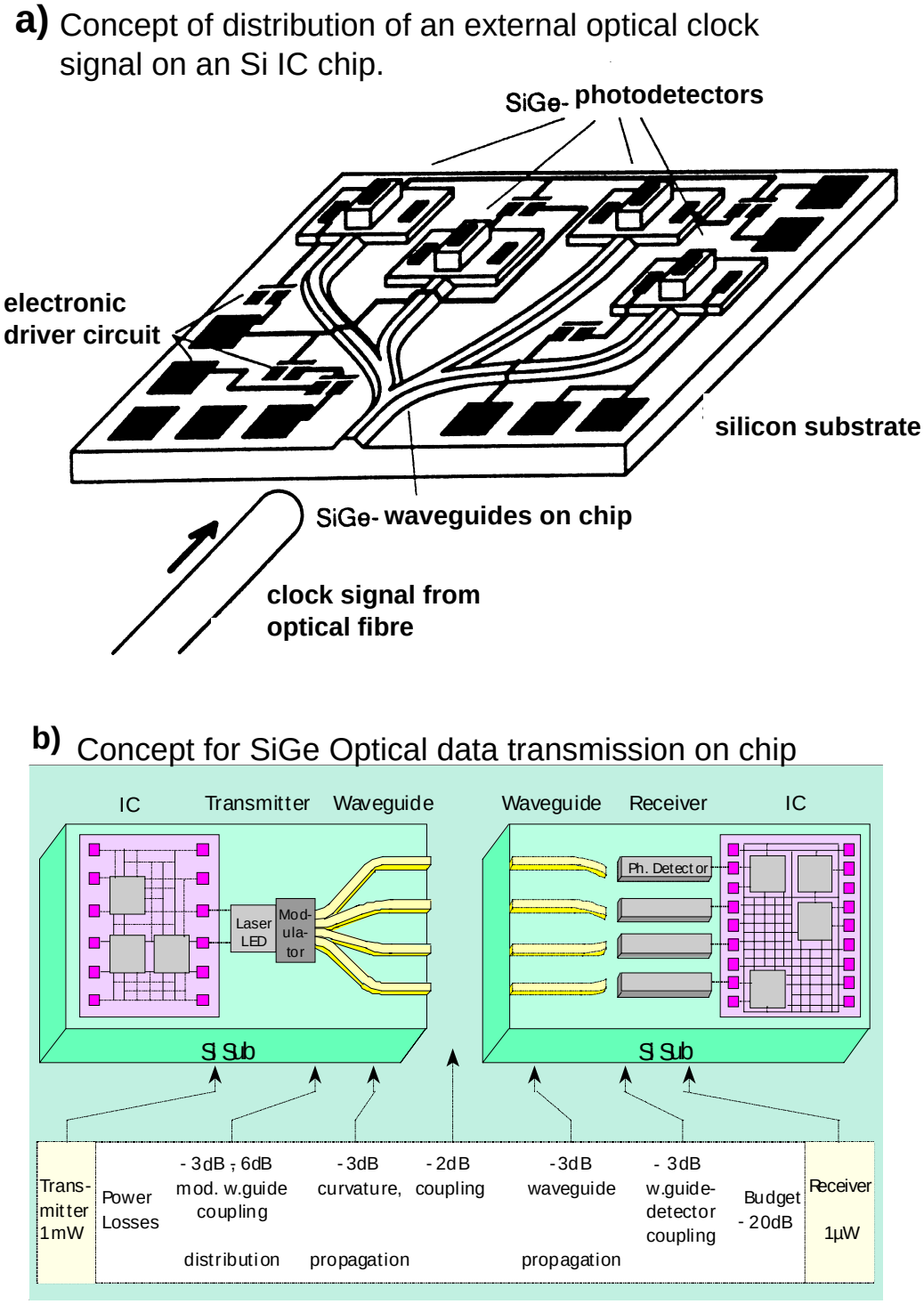


Fig. 10: (a) Concept of optical clock distribution on a Si IC chip using SiGe waveguides and photodetectors , (b) concept of optical interlink between two Si IC chips vial optical LED and detector devices.

Very recently interest has been raised on mid IR SiGe detectors – fabricated as large area focal plane arrays for thermal imaging applications in the 3 – 5 µm and 8 – 12 µm regime – to replace the conventional, commercially available silicide Schottky barrier detectors such as Pt:Si and Ir:Si. Even though these detectors – operating on the principle of hetero-internal photoemission (HIP) from photoexcited holes of a highly doped $Si_{1-x}Ge_x$ quantum well – have lower quantum efficiencies than comparable III-V detectors based on fundamental direct bandgap absorption such as HgCdTe and InSb, the advantage that these detectors can be fabricated on large scale Si substrates with good homogeneity, fill factor, and perfect thermal match to a hybrid mounted Si readout circuit overcompensates this drawback. Moreover, the use of SiGe bears the advantage of a wavelength tunable multi-color detector where the cutoff wavelength can be easily adjusted by the choice of the Ge content and/or doping level. Si/SiGe focal plane arrays have already been demonstrated with 256x256 [33] and 400x400 pixels [34] with excellent homogeneity, good dark current and external efficiencies around 0.75 %.

6. Markets for SiGe RF Devices

The turnover of microelectronic and optoelectronic devices and circuits is worldwide rapidly growing from US $45 billion in 1990, to 77$ billion in 1993 over 154 billion $ in 1995 and is estimated about 350 $ billion by the year 2000. Among all semiconductor materials Si is dominating this market with more than 97% share. 72% to 80% of this market share is covered by CMOS mainly for microcontrollers and memories.

Though the percentage share of bipolars will decrease from today to the year 2000 it means nevertheless an increase in turnover. This market trend is the biggest motivation to develop Si based hetero circuits. SiGe HBT's and SiGe HFET's or HCMOS fit best into the respective Si markets. SiGe HBT circuits will be introduced by the year 2000 while we hope to have a SiGe HFET ready to the market by then. Another important aspect is an economical one. SiGe needs no new fab because Si fabrication lines can be used, a fact that saves tremendously investment and processing costs. SiGe can use large Si-wafers which lowers material and area related processing costs. The area related processing costs are 0.09 $/mm^2 and 0.12 $/mm^2 for Si and SiGe [35] bipolar circuits while GaAs and InP costs go up to 0.5 $/mm^2 and 1.2 $/mm^2, respectively. SiGe hetero devices and circuits will be produced by large chip manufacturers. Companies like IBM, Siemens, NEC Philips, Hitachi, and TEMIC together with DaimlerChrysler are and will certainly stay active in this field.

Low cost, high performance Si/SiGe IC's are ideally suited for the high volume markets. There are various communication services as shown in Fig. 11. The mobile communication (MOBICOM) transmits audio and voice via handy phones at 0.9 to 2 GHz. The wireless local area networks (WLAN) at 2.4 and 5.8 GHz connects PC's. The satellite communication (SATCOM) at different bands (10 – 14 GHz, 25 GHz) or even higher supply low infrastructure areas and mobile users. The wideband communication via cables presently by coax and in future by fiber optic cables (FIBRECOM) transmit from 3 to 40 Gbit/s mainly in hubs of conurbation and in intercontinental networks. Each of these services will have 50 to 100 million users or terminals by the year 2005. With module system costs between $100 and $700 one expects market shares of 20 to 60 billion $ each [35]. Further markets are seen in navigation of mobile objects, e.g. global positioning (GPS ~1.5 GHz), satellite navigation (>10 GHz), defense and landing radar (20 – 40GHz), collision avoidance of cars (~70 GHz), robotic and industry sensors

(20 – 50GHz) which is sketched in Fig. 11. Market analysis also expects 100 Mio. modules for both fields. Computer and consumer electronics which increasingly demand faster signal processing might be a market for a SiGe chip. The share of microelectronic components in these systems is 20% to 40%, which makes this market attractive for chip manufacturers. According to collecting studies of different companies and market research groups the total turnover of SiGe chips in the next century is above 10 bill. US $.

Fig. 11: Scenario for applications of Si/SiGe hetero devices in the high volume communication market

Acknowledgment

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Silicon Germanium IC´s on the RF Market

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1. Introduction

Since 1974 the research on SiGe layers was heavily stimulated by the works of Erich Kasper, Ulf König, and Horst Kibbel [1], [2]. The principles of the growth of SiGe and a lot of technology details were invented by researchers of the DaimlerChrysler research center in Ulm, Germany. The break-through for SiGe into production was the first well functioning HBT at the end of the eighties [3]. The 1994 measured 113 GHz transit frequency of a double mesa SiGe-HBT [4] was one of the fastest silicon based devices until 1998 [5]. The 1995 achieved world record of maximum frequency of oscillation with 160 GHz is still valid [6].

In early 1993, U. König and A. Gruhle from Daimler Benz and H. Dietrich at TEMIC started a feasibility study and a predevelopment of SiGe-HBTs [7]. However, the real transfer into production started within the SIGMA project in the beginning of 1996 and was finished two years later in early 1998 [8]. Now SiGe1 is on the market, and a couple of well-known electronics companies are customers of TEMIC's SiGe1 technology.

Silicon Germanium heterobipolar transistors (SiGe HBTs) offer the opportunity to fabricate high performance ICs for RF systems in the 1 – 10 GHz range. The greatest benefit of SiGe one can earn in analog and mixed signal circuits as e.g. low noise amplifiers (LNAs), power amplifiers (PA), mixers, voltage controlled oscillators (VCOs), and phase locked loops (PLLs). In addition, high frequency analog to digital and digital to analog converters (ADCs and DACs) are reasonable circuits.

The advantages of SiGe over pure silicon for these applications are mainly the extremely high cutoff frequencies with record values from research HBTs of f_T = 130 GHz [5] and f_{max} = 160 GHz [6], and a ECL gate delay down to 9.3 ps [9]. The good high frequency noise performance with rf noise figures of 0.9 dB at 10 GHz [10] emphasizes the potential of SiGe HBTs in mobile communication systems. Furthermore, an important argument for using HBTs for wireless applications is the high power added efficiency at low DC voltages. SiGe HBTs challenge not only silicon, but also GaAs MESFETs by the higher linearity and gain for operation voltages below 3.6 V [11]. The main advantage of SiGe HBTs over III-V HBTs is that a standard Si production line and most of the standard bipolar process modules can be used for device fabrication. This allows low cost production with high yield and excellent reliability.

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2. Technology and DC-Performance

TEMIC offers a production technology, called SiGe1, including npn HBTs with and without selectively implanted collector on the same wafer [12]. The main important issue of the technology is the differential growth of the SiGe layer after a standard recessed LOCOS process. The SiGe poly is used for the base contact and for two of the three resistor types. The emitter has an inside and an outside spacer and an additional alpha-Silicon layer in order to perform the emitter and the collector contact. A SEM cross section of the emitter portion of a HBT is depicted in Fig. 1.

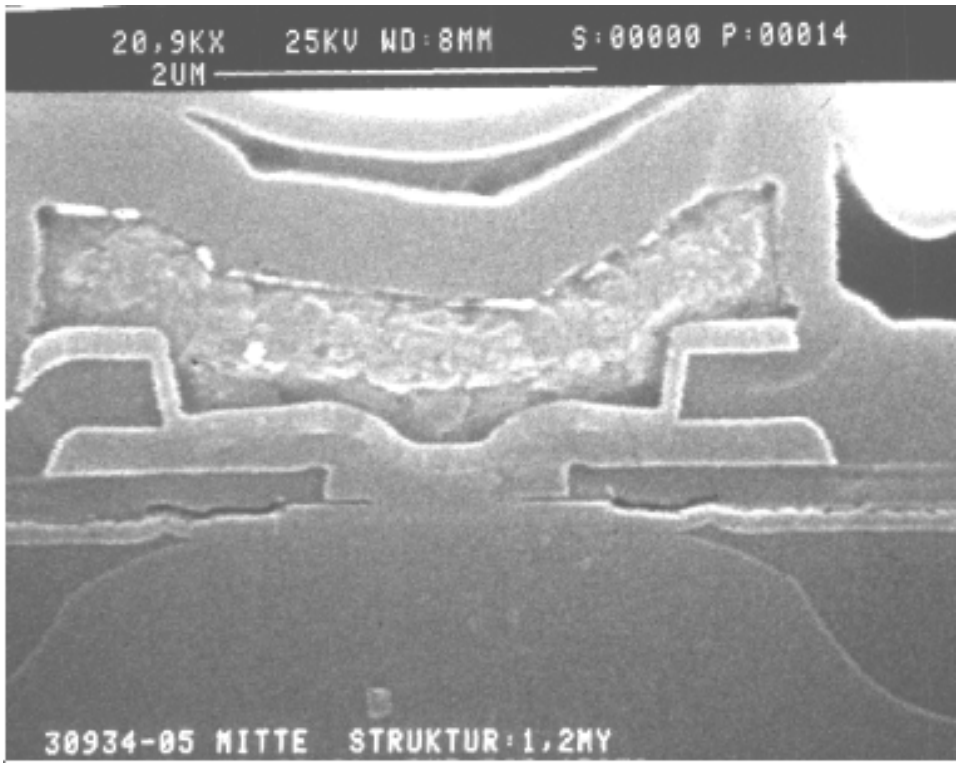

Fig. 1: Cross Section of the emitter part of a SiGe HBT.

In addition, spiral inductors, nitride capacitors, three types of poly resistors, a LPNP, rf- and dc-ESD protection, and varactor diodes are incorporated in the present technology. The parameters of the technology are summarized in Table 1.

In contrast to other companies, as e.g. IBM [13] and Siemens [14], which prefer a triangular Ge profile with only up to 15% Ge in their medium doped base, TEMIC´s SiGe1 technology has a nearly box shaped Ge profile with above 20% Ge in the base. The epitaxy itself is controlled by monitor wafers as depicted in Fig. 4 over three months. The highly boron doped SiGe base, $4x10^{19}$ cm^{-3}, which is grown by a single wafer CVD machine, has a real advantage over the drift HBTs due to the approximately 10 times smaller base sheet resistance, revealing values of 1.5 kΩ/ . Hence, it is possible to use wide emitter stripes, up to 2 µm, for power HBTs.

The main important parameters of the SiGe1 Technology are collected in Table 1.

Parameter	[unit]	non–SIC	SIC
NPN transistor			
Transit frequency	f_T [GHz]	30	50
Max. frequency of oscillation	f_{max} [GHz]	50	50
Current gain	h_{FE} []	180	180
Early voltage	V_A [V]	50	50
Collector emitter breakdown voltage	BV_{CE0} [V]	6.0	3.0
Collector base breakdown voltage	BV_{CB0} [V]	15	12
Noise figure at 2 GHz	F_{min} [dB]	1.0	1.0
LPNP			
Collector emitter breakdown voltage	BV_{CE0} [V]	7	
Current gain	h_{FE} []	7	
Typical collector current	I_{CP} [µA]	40	
Passive devices			
High ohmic poly resistor (poly1)	R_H [Ω/sq]	400	
Medium ohmic poly resistor (poly2)	R_M [Ω/sq]	110	
Low ohmic poly resistor (poly1–$TiSi_2$)	R_L [Ω/sq]	4.5	
Precision MIM capacitor	c_{SPEC} [fF/µm²]	1.1	
Spiral inductor 4 nH, Q–value at 2 GHz	Q []	7	
ESD Zener diode, Zener voltage	V_Z [V]	6.2	
Zener diode, parasitic capacitance	[pF]	5.5	
RF–ESD diode, parasitic capacitance	[pF]	0.3	

Table 1: Summary of the essential parameters of the SiGe1 technology.

3. Reliability

In order to demonstrate the reliability of the process a couple of important PCM parameters were collected over several lots.

Figure 2 corresponds to the expected probe yield for a chip having about 2000 minimum size transistors integrated. The SiGe1 technology is comparable in terms of masks and costs to a standard double poly Si BJT process. Therefore this technology is well suited for large scale integration (LSI), as nicely demonstrated in Fig. 3, which shows a wafer mapping of the 10k transistor arrays over a typical 6 inch wafer. In addition, a couple of lifetime tests on single HBTs and complete packaged circuits were all positive and were summarized in a special qualification report. The process was recently qualified.

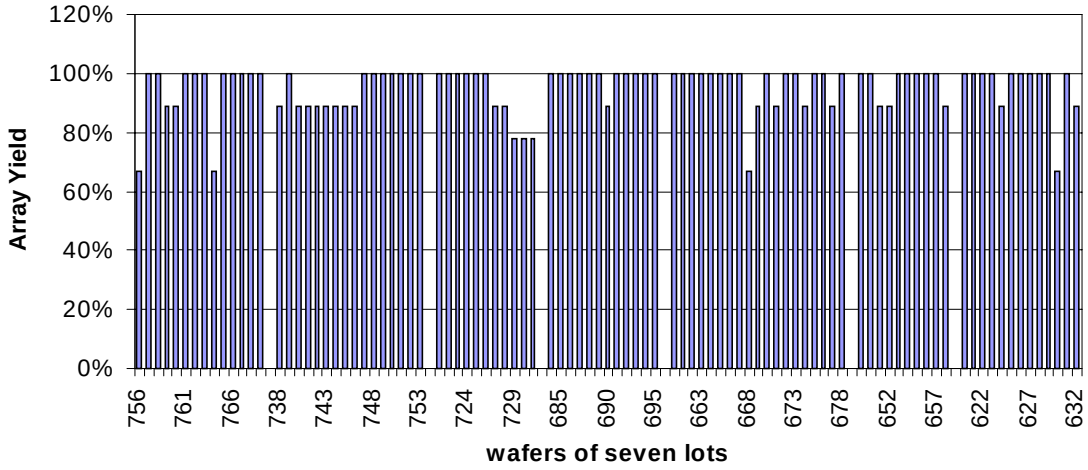

Fig. 2: Yield of PCM transistor arrays, corresponding to 2000 minimum size transistors.

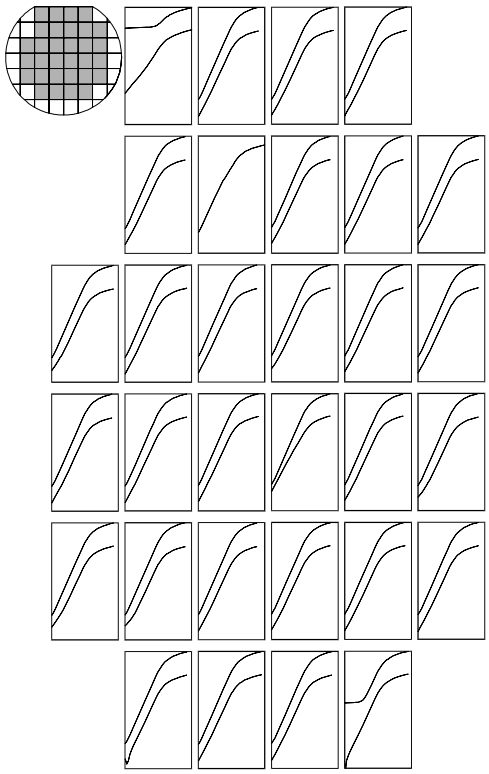

Fig. 3: Wafer mapping of a 10000 HBT array; HBT: 0.8x1.6 μm^2; array size: 3.5 mm^2.

4. RF and Noise Measurements

The SiGe HBTs reveal transit frequencies f_T of 30 GHz (Fig. 4) with a collector emitter breakdown voltage of BV_{CEO} = 6 V and 50 GHz with BV_{CEO} = 3 V, respectively.

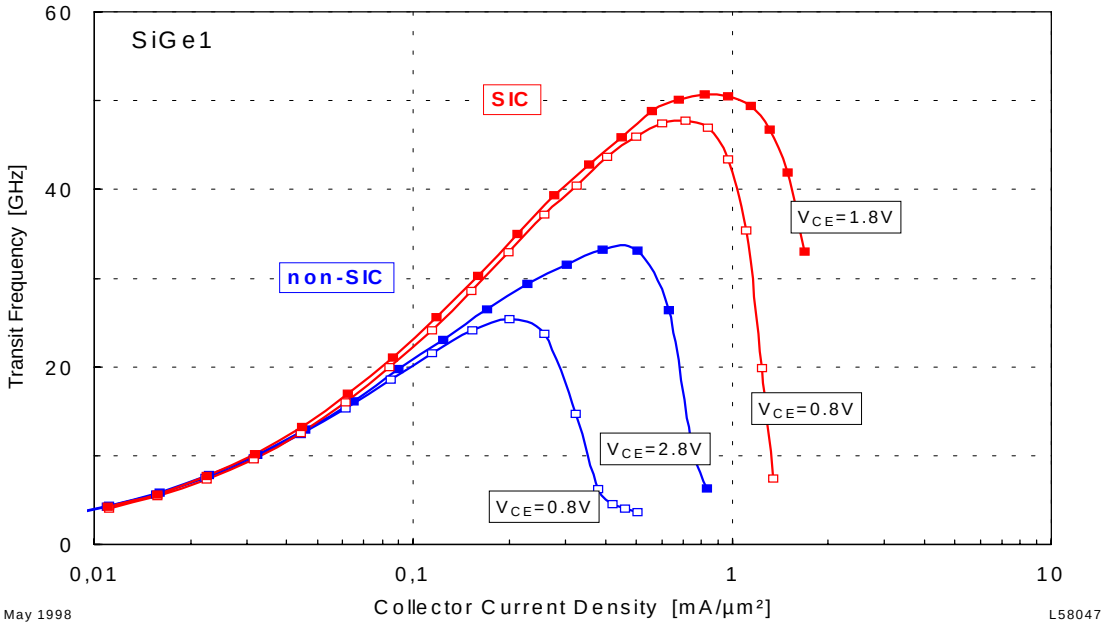

Fig. 4: f_T values of single emitter devices with and without SIC.

The maximum f_T and f_{max} values were achieved at current densities of 0.3 mA/µm² and 0.65 mA/µm² for the non-SIC and the SIC devices, respectively (Fig. 4).

For large signal applications, as e.g. power amplifiers, the linearity of the gain over a voltage swing is of great interest. The voltage dependence of the maximum frequency of oscillation and of the transit frequency for the non-SIC HBT revealed a constant value for V_{CE} voltages above 1.5 V. Hence for PAs high PAE values and a good linearity can be expected.

For low noise amplifiers the low high frequency noise of SiGe HBTs in the 1 to 5 GHz range is a real advantage over homo bipolar transistors. The typical minimum noise figure of SiGe1 HBTs at 2 GHz is about 0.8 dB, owing from the low base sheet resistance and the high current gain of 180. The associated gain is in the range of 17 dB.

5. Power SiGe HBTs

In order to demonstrate the performance of multi finger power devices, HBTs with different numbers of emitter fingers were investigated. The effective size of each finger is 1.6 x 30 µm^2.

On each side of the emitter is a base contact in order to achieve a low base resistance, and a collector finger contact is placed between a group of base and emitter contacts. To achieve homogenous current distribution for all emitters, a 4 Ohm ballast resistance is inserted in series to each emitter. The Gummel plot and the output characteristics of the multi emitter finger HBTs show good dc performance. The ideality factor of the base and the collector currents are close to 1 and the current gain h_{fe} is nearly constant over a wide current range. Due to the very high base doping the early voltage is above 50 V. The current gain is in the range of 150 and the breakdown voltage BV_{CE0} is 6 V, which is well suited for systems with 3.6 V battery power supply. The output characteristics of SiGe HBTs show no offset voltage, which is a big advantage over III-V single heter-

ostructure HBTs, because the offset voltage reduces the efficiency of the HBT in large signal operation.

A 10 emitter device with output matching for the fundamental frequency 1.9 GHz and 3rd harmonic achieved a value of 62% PAE. The results of the 10, 20 and 40 emitter devices show that the power scales with the number of emitters. With these devices 21 dBm, 24 dBm, and 27 dBm have been achieved in class AB operation at a collector-emitter voltage of 3.6 V. The PAE slightly decreases with the number of emitters from 62% at 21 dBm, to 50% at 32 dBm because the gain also decreases with the number of emitters. Gain reduction in multi emitter devices is a consequence of long internal connection lines of the devices. The electromagnetic coupling between these lines is responsible for gain and cut-off frequency reduction. In order to demonstrate the power capability of these HBTs also a 80 emitter stripe HBT was measured at 0.9 GHz showing 32 dBm output power and a corresponding PAE of 50%. Measurements on different geometries, finger lengths, and contact arrangements indicate that a further lateral layout optimization is still possible.

However, the newest results showed that it is possible to achieve PAE values as high as GaAs HBTs achieved at 900 MHz and 1.9 GHz. One of TEMIC's customers measured power added efficiencies as high as 72% at 900 MHz and 64% at 1.9 GHz as depicted in Figs. 5 and 6 [15] – [17].

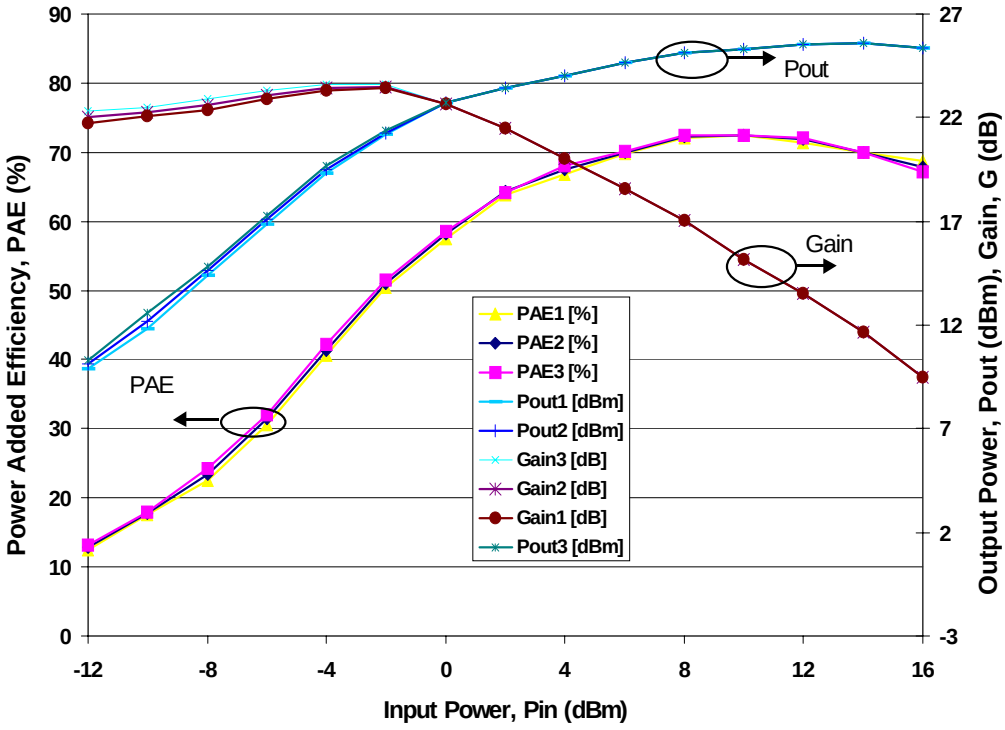

Fig. 5: Large signal results of 20 emitter HBT at 900 MHz revealing 72% PAE.

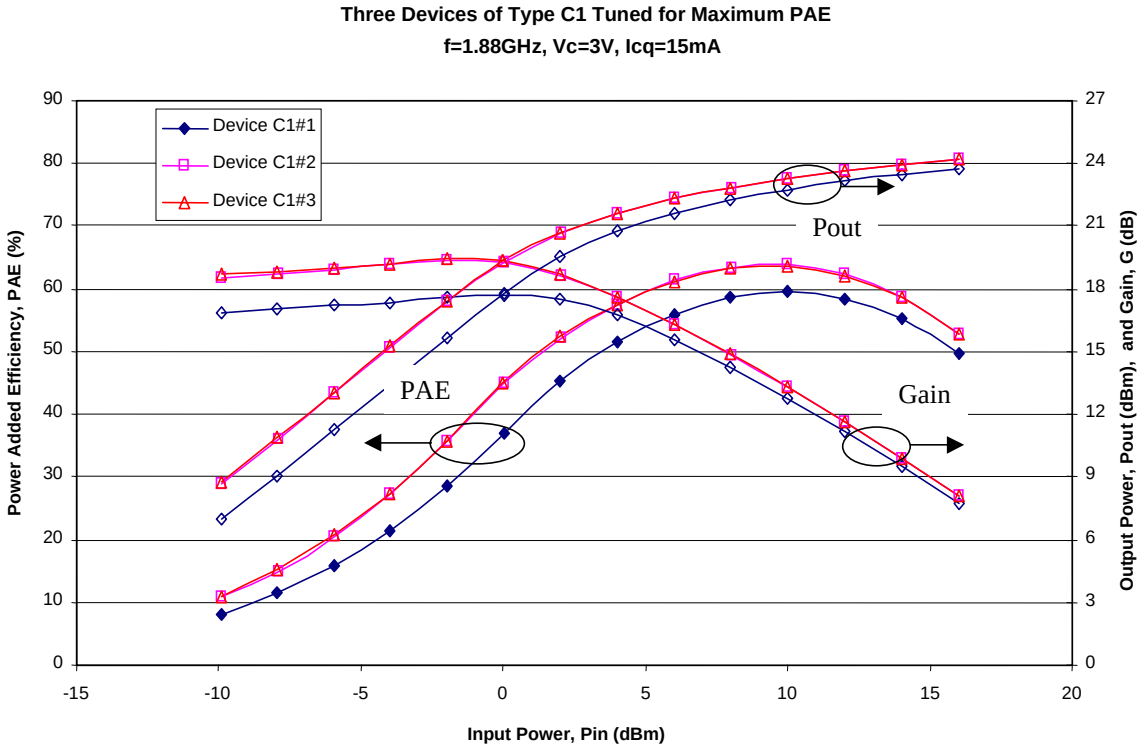

Fig. 6: Load pull measurements of 20 emitter HBT at 1.88 GHz (two different geometries).

6. Circuits

On research level a couple of SiGe based circuits were investigated in the last few years, e.g. a digital to analog converter (DAC) from IBM in 1993 [18], optical transmitter circuit from NEC in 1994 [19], [20], VCOs at 26 GHz and 40 GHz from Daimler-Benz in 1995 [21].

The application of the SiGe technology will be in wireless communication systems in the 1 – 6 GHz range. Hence, mixers, GSM power modules, dual band front-ends for GSM and DCS 1800 and DECT front-ends are in the focus. Additionally, LNA circuits were designed by the subcontractor University of Ulm and achieved a noise figure of 1.6 dB and an associated gain of up to 26 dB at 5.8 GHz. The relatively small bandwidth of the 5.8 GHz LNA is an advantage for mobile communication systems, reducing the expense for the input filter [22] – [24].

The first commercial product is a DECT front-end including a LNA with 1.6 dB noise figure and 20 dB gain combined with a 27 dBm power amplifier with 41% PAE over the whole packaged device, Fig. 7. This DECT front-end is now in production as one IC of a complete chipset [25].

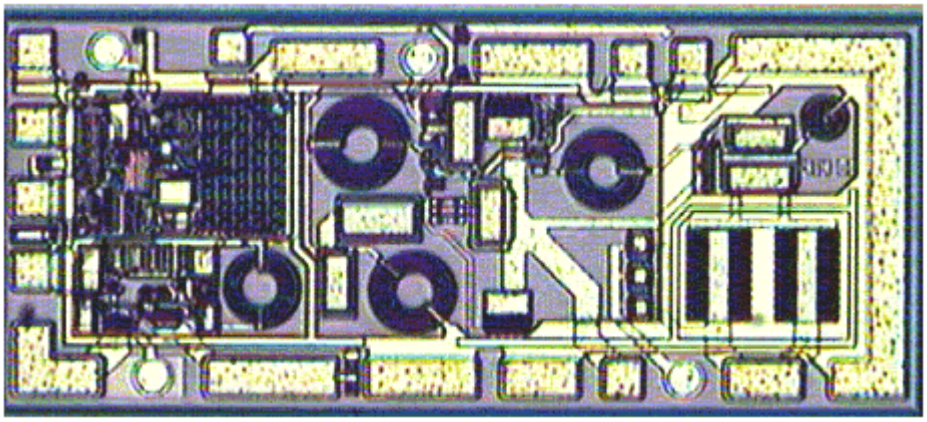

Fig. 7: DECT power amplifier with LNA.

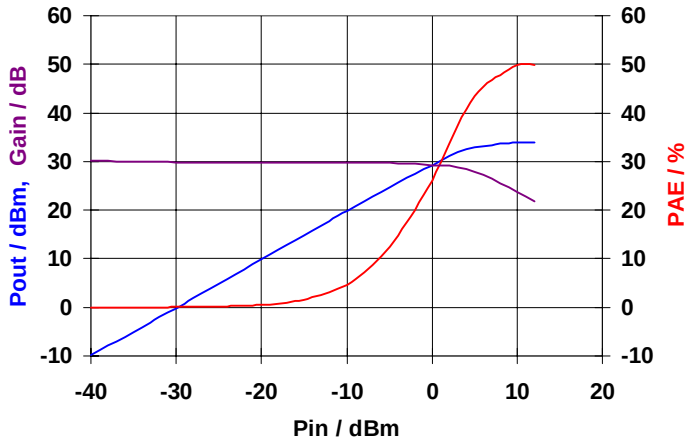

Fig. 8: Output power, power added efficiency and gain vs. input power of a flip-chip GSM-PA.

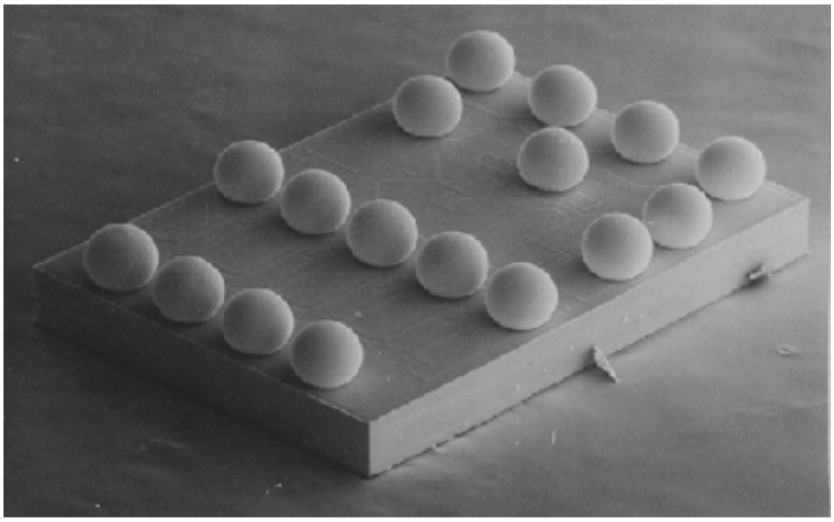

Fig. 9: REM photograph of a flip-chip GSM-SiGe-HBT 3 stage power amplifier.

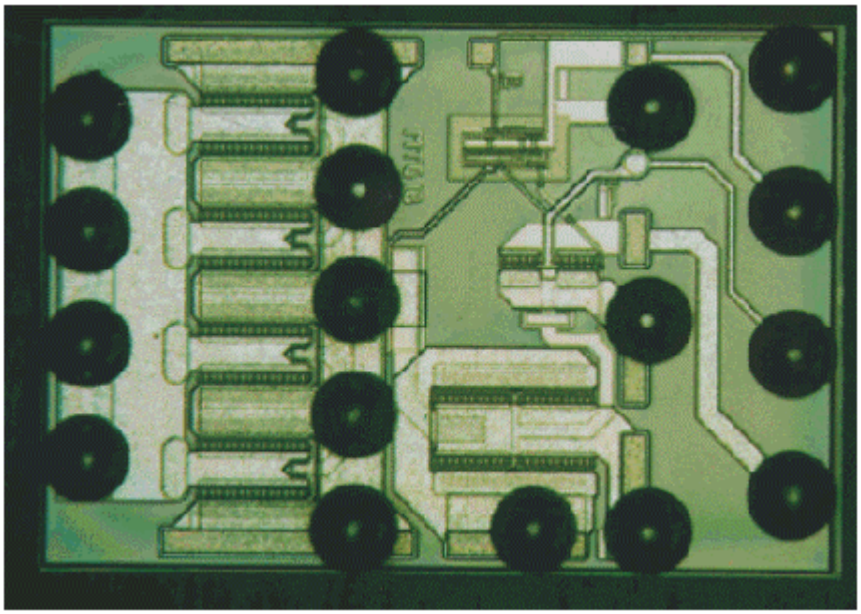

Fig. 10: Top view of GSM PA.

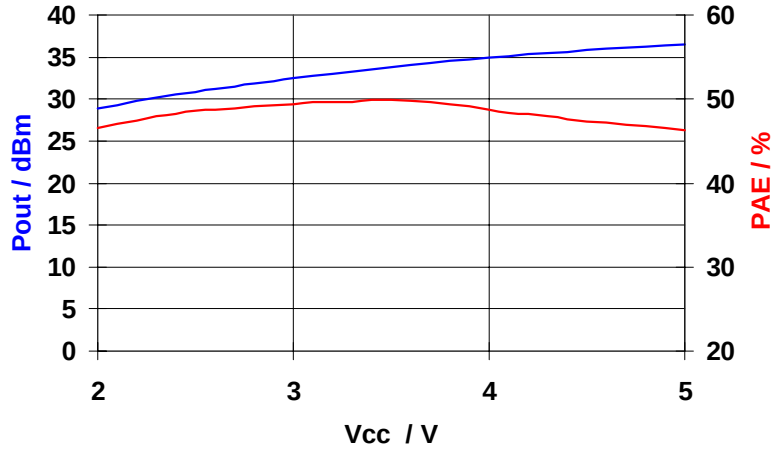

Fig. 11: GSM-flip-chip amplifier; PAE = 50%, Gain = 30 dB, Pout = 32 – 36.5 dBm, Vop = 2 – 5.5 V.

The second SiGe1 product group will be the TST0911, TST0912, and TST0913. These are power amplifiers for dual-band (GSM and DCS 1800) and for GSM and DCS 1800, respectively. Some important pictures and measurements are shown in Figs. 9 – 11. The overall PAE of the whole GSM chip achieves 50% and an output rf power up to 4.5 W. The power of these three stage amplifiers is voltage controlled, in order to set the power level to the needed value. The photographs shows a chip of the GSM amplifier, having approximately 300 emitters, whereas the dual-band IC has about 500 emitter stripes with 1.6 x 30 μm^2, corresponding to an emitter area of 18750 minimum size transistors.

7. Conclusions

Thanks to the differential epitaxy and the SiGe box profile the SiGe1 technology is well suited for analog and mixed signal applications. The real HBT concept distinguished by a high doped base and a lower doped emitter originates from the Daimler Chrysler research center in Ulm and was successfully improved to a production technology in the last three years at TEMIC in Heilbronn. TEMIC´s SiGe1 production technology is a 30/50 GHz f_T and 50 GHz f_{max} technology. It includes besides the two types of npn HBTs three types of poly resistors, nitride capacitors, spiral inductors, DC and RF ESD diodes and lateral pnp transistors.

SiGe1 is used for RF low noise amplifier and power amplifiers in mobile phones, e.g. DECT, GSM, DCS1800, CDMA, TDMA. In addition, gain blocks, dual-band transceivers and mixer circuits for base stations are in the product portfolio.

The quality and the reproducibility of the technology were demonstrated by highlights as functioning 10k arrays over whole wafers and lots, by 0.5 W power HBTs revealing 72% PAE at 900 MHz and 64% at 1.8 GHz, a LNA at 5.8 GHz with a record noise figure of 1.6 dB and 26 dB associated gain, and a 2:1 multiplexer showing a clear eye diagram at 40 Gbit/s.

However the main important message of this paper is:

The first TEMIC SiGe-IC´s are on the market.

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GaAs-MMIC Design Aspects for High Volume Production

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1. Introduction

1.1 History – Volume Production-Processes

Starting 1980 with GaAs-MESFETS and 1982 with the world's first GaAs-MMIC, production of GaAs devices at Siemens HL ramped up to more than 80 million pieces in 1998.

Three kinds of active device families are in production today, a MESFET, a HEMT and a HBT process. They all are produced in one single GaAs fab using the same equipment. Unified passive components make the MMICs complete.

Also the backend activities (thinning, via etching, sawing and packaging) are common for the three families.

For the MESFET family a patented self-aligned ion implantation process DIOM (**D**ouble **I**mplantation **O**ne **M**etalization) is used, which results in robust, reliable, and uniform devices compared to conventional recessed gate processes.

The process parameters are optimized to the application requirements:

Gate lengths of 0.8 and 0.5 µm are used depending on the frequency of operation. The active channel is optimized to either low noise or high power applications, and especially for mobile communication high power devices with low supply voltage allow to reduce the number of battery cells and therefore the weight and size of handheld mobile phones.

HEMT processes are based on epitaxial grown materials. For frequencies up to ~40 GHz a gate length of 0.18 µm is used (f_t > 60 GHz), and process parameters are optimized for either low noise or high power applications. For even higher frequencies 0.13 µm gates are used which results in f_t of 110 GHz.

The most advanced process uses **h**etero **b**ipolar **t**ransistors (HBT). Several MMIC designs are in the evaluation phase with very promising results regarding output power and efficiency at minimized chip area.

The passive components for all of the processes above follow unified design rules and are processed using the same standards and equipment. They cover lumped elements like resistors, inductors, and capacitors as well as distributed elements like microstrip and coplanar lines and their discontinuities. Interconnections between different compo-

nents are preferably realized by air bridges of plated Au which offer low parasitic capacitance and avoid edge problems due to non-planar surface.

Low inductive substrate via holes are essential for the behavior of microstrip based unbalanced circuits.

2. Essentials for Volume Production

2.1 Competitive Products in Cost and Performance, Customer Acceptance

Most impulses for volume production in the last few years have been due to the boom in the mobile communication market. Two contrary GaAs MMIC trends can be observed for the RF power stage in mobile stations:

- Devices as cheap and small as possible; DC circuits and matching on chip waste expensive chip area and should be added externally.
  Microwave skill by the mobile phone designer is essential.
- PA should be a black box, in- and output internally matched, bias circuit on chip. The customer doesn't want to care about microwave behavior.

As a manufacturer who provides components for all the different mobile communication systems all over the world Siemens offers both types to its customers. Figure 1 shows in identical scale MMIC examples for the minimized and the "all functions included" type.

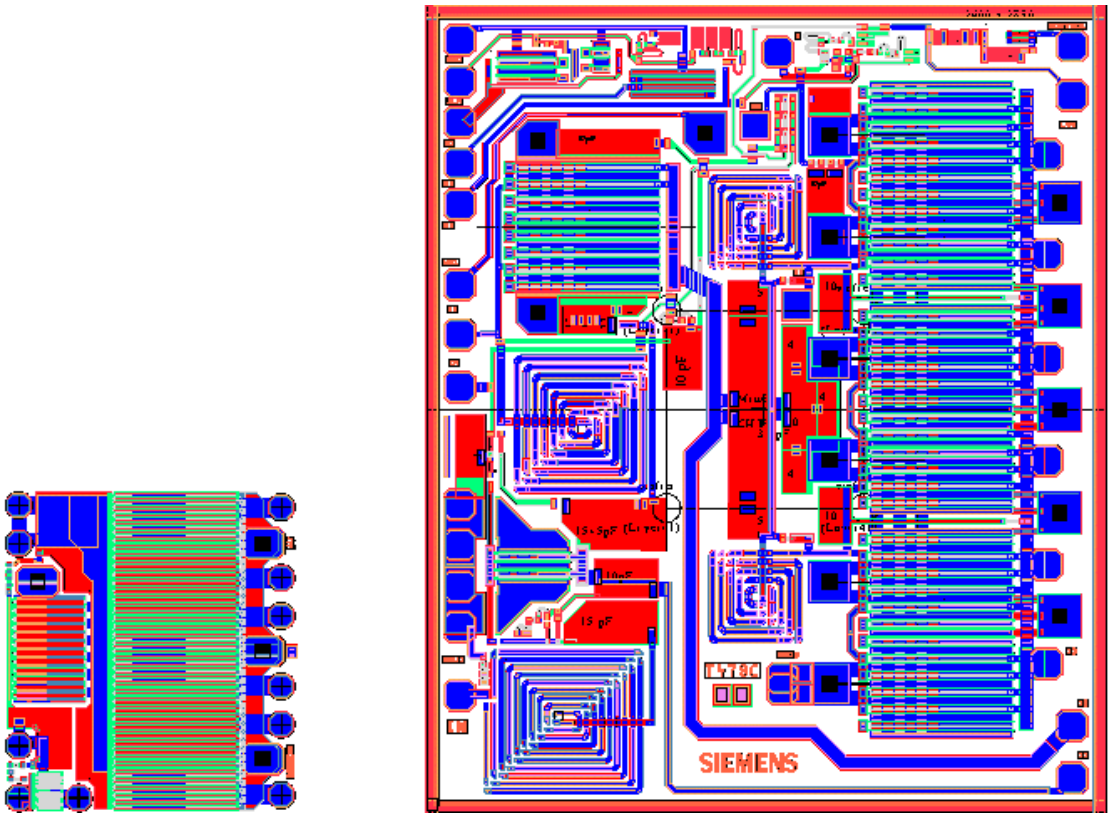

Fig. 1: 3 stage GSM PA MMIC minimized and "all included" type (identical scale)

2.2 Avoid Production Bottlenecks

Sometimes it is important to find workarounds for possible bottlenecks in production.

One example is the substrate via etching process. A wet etching process takes a few minutes per wafer while a dry etching process takes roughly ten times longer. Despite some advantages of the dry etching process (smaller structures and distances possible) the wet etching process is preferred because of its higher throughput.

A further example is the sub-0.3 µm gate process for HEMTs. It is not possible to realize these gate lengths with conventional lithography on an I-line stepper (365 nm). Alternatively, E-beam, deep UV, or X-ray lithography could be used, but they do not fulfil our requirements for throughput and/or cost reduction.

We use chromeless phaseshift masks on I-line steppers to define a well controlled homogeneous photoresist structure well below 0.5 µm, but for physical reasons still larger than the target gate length. Two or more subsequent spacer processes stepwise narrow the gate length precisely to its final value.

3. Cost Reduction

3.1 Component Shrink – High Packing Density – Plastic Packages

A key factor for cost reduction is chip shrinking. The design rules for active and passive components consider that the components are producible with sufficient yield. Progresses in process or equipment are opportunities to update the rules, which is performed permanently. Of course the maximum ratings for current density and breakthrough voltage must be taken into account. Usually there is little effect of shrinking on passive component models. Active devices should be remodeled, while special care has to be taken on thermal modeling, when shrinking the gate pitch (gate to gate distance).

Increasing the packing density may have effects on the circuit simulation that are difficult to handle. Exact models for electrical or magnetic coupling between components that are placed close to each other are not available in commercial simulation tools. To overcome this problem it is convenient to perform field simulation for some local coupling problems. Field simulation of complete MMICs still overcharges EM-simulators. It is still not possible to include active devices into EM-simulation.

SMD plastic packages are cheap and easy to handle for the application but not optimal in their RF-behavior and difficult to simulate. The model depends on bond wire length, chip size and even the location of chip via holes. The chip “ground” (backside metal) is connected to the external ground through an inductive lead. Ground current causes a voltage drop along this lead with the effect that the backside metal of the chip carries a certain RF-potential. This causes feedback across stages, which without any prevention may lead to a total degradation of the electrical behavior of the packaged MMIC.

Principally, a non perfect chip ground calls in question the models for microstrip-like components, because they generally are developed under the assumption of a perfect ground.

3.2 Design Consequences

Parasitics due to high packing density in principle are low loss capacitive and inductive effects, and experience shows that they mainly cause frequency shifts and gain slope

which usually can be compensated. The designer and layouter should be aware of these effects. Microwave skill in the layout phase helps to minimize their influence by clever chip architecture. Nevertheless these effects are difficult to be quantified. Knowing this simulation can be used to look for components which principally can compensate frequency shifts and gain slopes. If these components are designed with tuning options a method has been found to tune prototypes of the circuits experimentally.

The final component values have to be transferred to a production mask. The redesign procedure will be accelerated if the tuning options are defined late in the wafer process.

4. Future Trends

Distance radar in car traffic promises for the future similar production volumes like mobile communication today. A point of interest for this mm-wave application is flip-chip mounting and bumps for low inductive interconnections and for thermal reasons.

Carbon Co-Doping of $Si_{1-x}Ge_x$:B Layers: Suppression of Transient Enhanced Diffusion

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$Si/Si_{1-x}Ge_x$ heterobipolar transistors (HBTs) are now commercially available and expected to open the mobile communication market for Si-based electronics. A technological problem is caused by transient enhanced diffusion (TED) of boron in the extremely thin base layer of such transistors. It is mainly caused by injection of interstitials from a subsequent implantation processes. Co-doping of the $Si_{1-x}Ge_x$ base with carbon is shown to significantly reduce TED.

1. Introduction

$Si_{1-x}Ge_x$ is the obvious choice for extending the physical properties of Si through the exploitation of heterostructures without sacrificing standard Si technologies. Most of the worldwide activities in that area are dedicated to the $Si/Si_{1-x}Ge_x$ heterobipolar transistor (HBT), which is now available commercially in integrated analog circuits that will open fast growing high-frequency markets for Si-based electronics. In contrast to even more potent devices based on III-V materials, $Si_{1-x}Ge_x$ is readily integrated with standard Si MOS devices, which allows cost effective monolithically integrated circuits with mixed analog and digital functions. The feasibility of such hetero-BiCMOS circuits with a high degree of complexity in both their bipolar and CMOS components have been demonstrated by several companies [1], [2]. Their introduction is expected to be of major impact on the development of high-frequency electronics up to 20 GHz and beyond.

2. Transient Enhanced Diffusion

Depending on the concept of the HBT, its speed advantage is either caused by an additional drift field in a graded $Si_{1-x}Ge_x$ base (drift transistor; [3]) or by the reduction of the base width and simultaneous increase of the base doping (true HBT; [4]). In either case it is important that the heterointerfaces coincide with the p/n junctions to prevent detrimental parasitic potential barriers. Precise doping control during all fabrication and annealing steps is therefore a stringent condition for successful high frequency operation. It is especially the p-type (boron) doping of the base layer which can cause problems in later process steps, because boron is well-known for its transient enhanced diffusion in the presence of interstitials [5]. Those can be created by an oxidation process (known as oxygen enhanced diffusion; OED), or by implantation of high doses of dopants, which are routinely employed for the n-doping of the poly-emitter above the epitaxially fabricated base layer. Thermal activation of these dopants causes boron in the base to diffuse transiently much faster than would be expected from the well established bulk diffusion constant at that temperature. This can cause severe degradation of the high frequency behavior and other essential characteristics of these devices.

To suppress TED, co-doping with substitutional carbon has been proposed in the literature [6]. At sufficiently high concentrations, carbon is believed to form complexes with the injected Si interstitials [7]. This limits the density of interstitials available to transient boron diffusion, which should therefore be strongly reduced.

3. Experiments

Most experiments dealing with TED and C co-doping are based on Si layers implanted with B and C. But, since the base of a $Si_{1-x}Ge_x$ HBT is grown and doped epitaxially, it appears straightforward to deposit a B-doped $Si_{1-x-y}Ge_xC_y$ layer with a C concentration of 0.5 to 1 at. %. We have shown that such layers can be grown with a high degree of perfection under low-temperature growth conditions that allow substitutional C concentrations of a few at.%, i.e. far below the solid solubility [8].

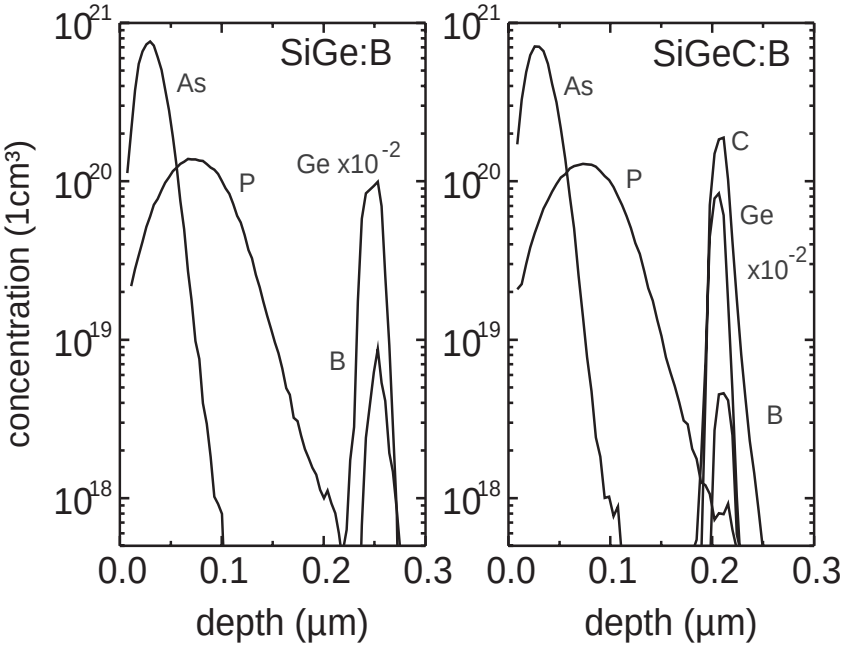

Fig. 1: SIMS profiles of $Si_{1-x}Ge_x$:B and $Si_{1-x-y}Ge_xC_y$:B epilayers with *ex-situ* implanted Si cap layers.

To study TED in a realistic, HBT-like situation we grew by molecular beam epitaxy (MBE) highly boron-doped $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ layers, which were capped by an initially undoped Si layer. Figure 1 shows SIMS profiles of a $Si_{0.79}Ge_{0.2}C_{0.01}$:B layer in comparison with a reference layer that was lacking the C co-doping. Ge concentrations are of the order of 20 at.%, and scaled down in Fig. 1 by a factor of 100 to fit the logarithmic concentration scale of the dopants. The Si cap layers were subsequently implanted ex-situ both with As and P to create the interstitials required for TED.

Figure 2 shows the development of the B profile as a function of oven anneals in the temperature range between 550 and 900°C. Since the Ge profile is not affected in this temperature range it is just indicated by a shaded area for reasons of clarity. As expected, the reference sample shows strong TED, which leads to a basically useless doping profile after the 900°C anneal. In contrast, the presence of about 1 at.% of carbon suppresses boron TED almost completely. The B profile remains within the

$Si_{1-x-y}Ge_xC_y$ layer, and only a minor reduction of the peak concentration is observed, which lies within the accuracy of SIMS. Obviously, C co-doping is a very efficient means to stabilize the doping profile of a $Si_{1-x}Ge_x$ n-p-n HBT during integrated circuit processing.

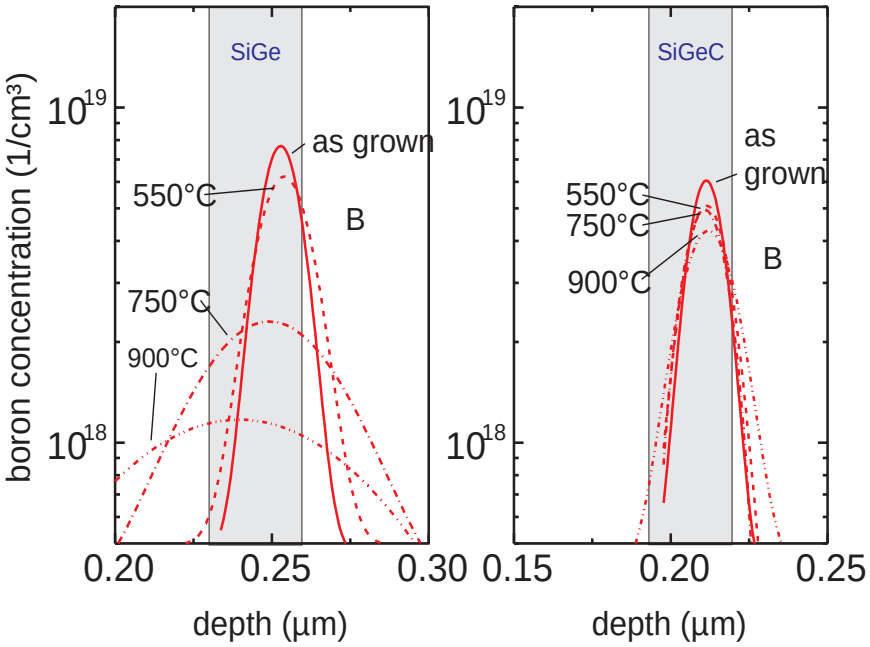

Fig. 2: Transient enhanced (TED) boron diffusion after annealing cycles in the temperature range 500° – 900°C. Left: $Si_{1-x}Ge_x$:B epilayers shows strongly enhanced diffusion at all temperatures studied. Right: $Si_{1-x-y}Ge_xC_y$:B epilayer suppresses TED of B almost completely.

4. Conclusions

We demonstrated that the use of a ternary $Si_{1-x-y}Ge_xC_y$ base layer with a C concentration ≤ 1% for the usually employed pure $Si_{1-x}Ge_x$ layer can drastically improve the notorious transient enhancement of boron diffusion, and thus conserve the basic speed advantages associated with an HBT. Further work will concentrate on possible side effects associated with the presence of substitutional and non-substitutional carbon, and on an process-compatible optimization of the carbon concentrations necessary (and tolerable) for device operation.

Acknowledgments

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Fabrication of Semiconductor Nanostructures by Scanning Force Microscopy

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A process for fabrication of semiconductor nanostructures using scanning force microscopy (AFM) in combination with conventional optical lithography is described. It is based on the mechanical modification of ultra-thin photoresist layers with super-sharp AFM tips and subsequent pattern transfer by reactive ion etching. Minimal feature sizes of 45 nm and periods of 88 nm were achieved by this technique.

1. Introduction

The fabrication of semiconductor nanostructures for the development of quantum electronic devices has attracted tremendous interest in the last few years. In such devices, the electron wavelengths of typically 20 – 50 nm are comparable to the device dimensions. Therefore, the electronic properties are dominated by quantum phenomena. The realization of nanostructures remains a big technological challenge. Although with scanning probe microscopy controlled surface modifications have become possible down to the level of single adatoms [1], for practical applications one would like to combine the high lateral resolution of scanning probe techniques with existing semiconductor process technologies [2]. In the present work, we have developed a process sequence that combines conventional optical lithography with mechanical modifications of ultra-thin photoresist layers with super-sharp atomic force microscopy (AFM) tips [3]. This allows an efficient definition of very large, as well as nanoscale resist patterns with subsequent pattern transfer to the substrate in one single reactive ion etching step.

2. Process Description

The AFM patterning is realized by indentation of an AFM tip into a soft photoresist layer. This produces well defined structures where the resist is locally removed. The minimal feature size is mainly determined by three parameters, namely, 1) the resist thickness, 2) the size and shape of the AFM tips, and 3) the directionality of the final pattern transfer process. For optimum results the use of ultra-thin photoresist layers is of particular importance because the size of bulge of the displaced photoresist around the holes is the main limitation for the minimal feature separation.

2.1 Lithography with Ultra-Thin Photoresists

To produce an ultra-thin photoresist layer, the positive resist ‘Shipley S1805’ is diluted with a thinner (’Shipley EC Solvent’) in the proportion 1:12 to 1:15. The highly thinned photoresist is spin-coated on the sample with 5500 rpm, forming a homogeneous layer

with a thickness of about 15 nm. Conventional optical photolithography with a 'Süss Mask Aligner' was used for definition of a test pattern in the resist with various device structures with typical feature sizes of several µm (see Fig.1a).

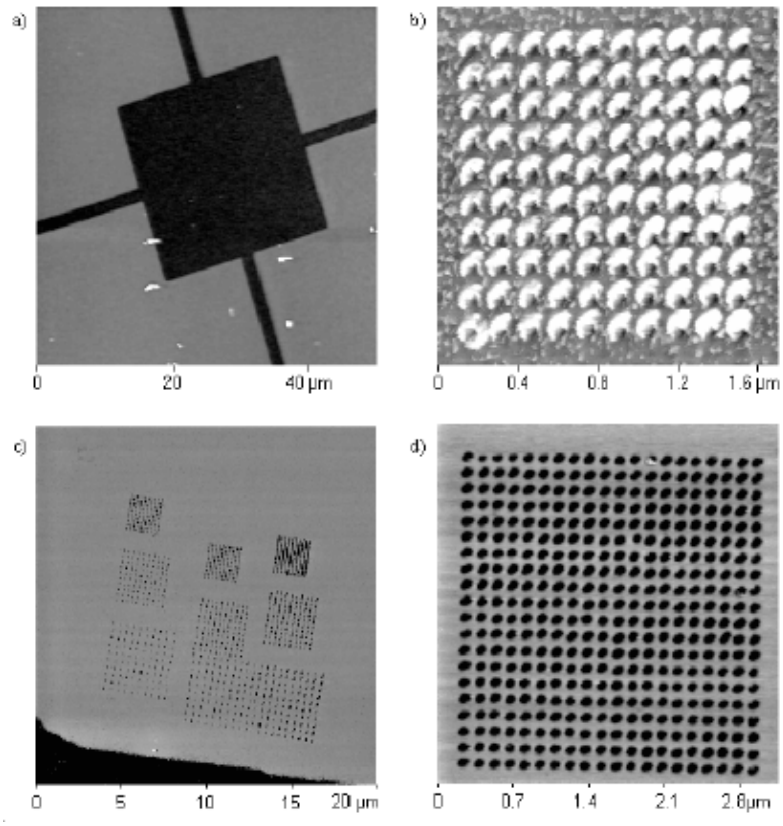

Fig. 1: AFM images illustrating the different stages of the lithography process: a) large scale resist pattern produced by optical lithography, b) hole array indented into the 10 nm photoresist the AFM, c) large scale and d) zoomed-in images after RIE pattern transfer to the Si wafer and oxygen plasma resist removal.

Ultra-thin photoresists require a careful choice of the developer since a very low solubility of the unexposed resist is required. We have tested two different developers. The developer 'Shipley MF319' shows a significant solubility of the unexposed resist as it is increasingly diluted. While the solubility of the unthinned resist is about 0.4 nm/s, it is 1.1 nm/s for a resist thinned to 1:15. Therefore, the final resist thickness of 15 nm is very difficult to control. For the 'Microposit Developer' no solubility of the unexposed resist was found. For 15 nm resists, 15 sec developing time was found to be sufficient.

The mechanical properties of the photoresist are significant for the following AFM nanofabrication process. If the resist is too soft, a reflow of the features occurs, and if it is too hard, unnecessary large indentation forces are required. This leads to increased chances of tip damage during the resist modification. The mechanical properties of the photoresist can be adjusted by a hardbake step after the developing. Here we have used a 30 min hardbake at 130° C. This hardbake also causes a shrinking of the photoresist, which becomes more pronounced with increasing resist dilution. At a 1:15 dilution, this shrinking amounts up to 30%, i.e., the resist thickness is reduced from 15 to 10 nm.

2.2 Mechanical Patterning Using Scanning Force Microscopy

Nanoscale patterns were generated by indentation of the AFM tip into the photoresist. This produces holes with the displaced photoresist left as a bulge around the holes, as is shown in Fig. 1b). The crucial parameters of this mechanical modification process are: 1) the shape and material of the AFM tip, 2) the thickness and hardness of the resist, 3) the applied indentation force, and 4) the nonlinearity corrections of the AFM piezo scanner. In order to minimize the mechanical stress on the AFM tips during indentation, the AFM was operated throughout in the 'tapping' mode, where the cantilever is vibrated near its resonance frequency with an amplitude of about 100 nm.

At first we have used focused ion beam sharpened silicon tips of 'Park Scientific Instruments'. Although these ultra-sharp tips with tip radius of around 10 nm produce very narrow holes in the resist, the monocrystalline Si tips easily break during the mechanical contact with the sample. A much better reproducibility was achieved when using carbon EBD tips that are produced by electron beam induced deposition of very hard amorphous carbon on standard silicon tips and the subsequent sharpening with an oxygen plasma [3]. This yields tip diameters in the 10 nm range. With the EBD tips many thousands of holes can be produced without significant tip degradation. Failure usually occurs only by breaking off of the carbon tip from the cantilever. The optimal tip force applied during the indentation process is reached when the tip just penetrates the layer of photoresist down to the sample surface. If the force is too strong, apart from possible tip damages, the size of the indented holes increases. At too low indentation forces the photoresist is not penetrated entirely and no reproducible pattern transfer is possible. For the 10 nm resist, we use an exposure force of about 2 µN. This corresponds to a scanner extension of 100 nm for cantilevers with a spring constant of 20 N/m.

The resist thickness is a crucial parameter for the ultimate resolution to be reached. Thicker resist layer lead to larger bulges, which limits the minimal distance between adjacent holes. On the other hand, since the resist is also attacked in the final pattern transfer by the reactive ion plasma, a reasonable thick resist is needed to allow a sufficiently deep etching of the samples. Therefore, a compromise between resolution and pattern transfer has to be found. For a resist thickness of 10 nm, a sufficient pattern transfer is possible (depth after etching about 30 nm), while the resolution is still good (minimal period about 85 nm, see Fig. 2). An important aspect for the fabrication of well defined complex structures is the compensation of the large nonlinearities of the AFM piezo scanners. This generic problem of AFM was solved using the external position control provided by the AFM of 'Park Scientific Instruments'. Test structures written without the scan correction exhibit pattern distortions as large as 10%.

2.3 Pattern Transfer by Reactive Ion Etching

For pattern transfer of the resist patterns to the Si wafers that were used as test samples, we have used an 'Oxford Instruments' reactive ion etcher with SF_6 as reactive gas. As the ultra-thin etch mask of the photoresist is attacked by sputtering, a high etch selectivity between the resist and Si is of crucial importance. We have increased the selectivity by using low RF powers (reduced sputtering rate of the resist). In addition, higher gas pressures and flow rates were found to increase the Si etch rate. A drastic reduction of the resist sputtering rate can be achieved by adding CH_4, which generates a protecting polymer layer, but unfortunately this decreases also the Si etch rate. The optimal etch conditions were found to be a RF power of 30 W, SF_6 flow rate of 50 sccm, pressure of

40 mtorr and a CH_4 flow of 25 sccm. This results in an etch rate for Si of 49 nm/min and of 6 nm/min for the resist. Finally, the photoresist is stripped from the sample in the same RIE reactor with an oxygen plasma (90W, 10 sccm, 60 mtorr). The resulting patterns after these processing steps are shown in Fig. 1 c) and d).

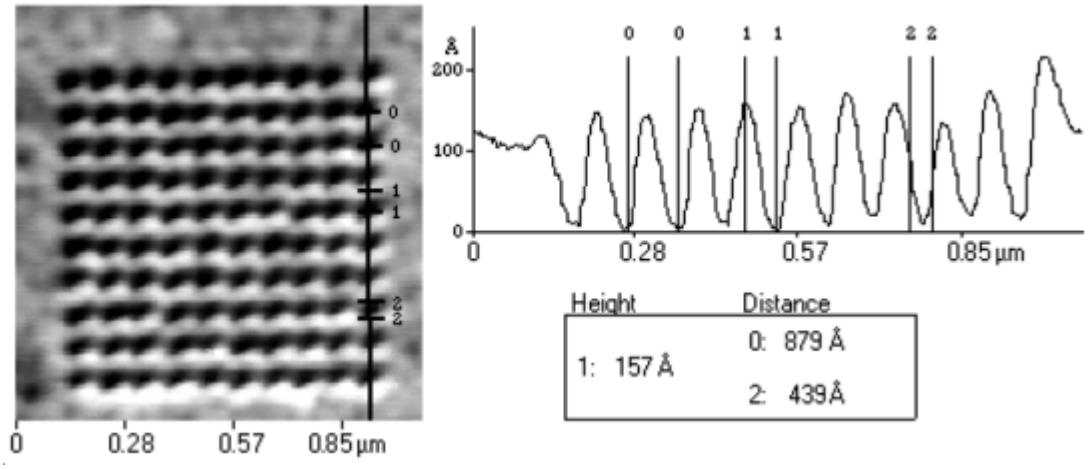

Fig. 2: Atomic force microscopy image and cross sectional profile of a periodic hole array in Si fabricated by AFM nanolithography. Array with 10 x 10 holes with a period of 88 nm, hole diameter of 44 nm and hole depth of 16 nm.

3. Summary of the Results

The minimal feature sizes that were made by the combined optical and AFM lithography process are shown in Fig. 2. The test pattern of a periodic hole array exhibits feature diameters of about 44 nm with an etch depth of about 30 nm. Minimal grating periods of 88 nm were achieved. Apart from such hole structures we have also fabricated lines with 45 nm line widths. The lines were drawn by putting a series of holes in very close proximity (less than 30 nm) to each other. In this way also more complicated structures can be made. The largest dot arrays we have produced so far consisted of several thousand individual dots and exhibited no apparent pattern distortions within fields of several micrometer in size. The big advantage of our approach is that is a mask-based lithography technique that is independent of the substrate and which allows the use of proven semiconductor processing steps. Therefore, we were able use our method for GaAs nanostructure fabrication just by modifying the final etching process.

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Focused Ion Beam Technology – A New Approach for the Sub 100 nm Microfabrication Regime

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Focused ion beam (FIB) technology is an attractive tool for various maskless processes with the capability of structure fabrication below 100 nm. The current state of the art and the potential application for device modification, failure analysis, and process development is reviewed. The utilization of the FIB as a substantial component for fabrication and testing of metrology and the relevant electrical properties in the sub 100 nm regime is described.

1. Introduction

The focused ion beam represents a versatile tool for metrology and highly resolved 3-dimensional imaging of complex multilayer structures. Furthermore, it allows the fabrication of ultrafine structures by direct deposition of metal or insulator schemes and spatially confined doping. A minimum feature size down to 25 nm and a nesting tolerance of 10 nm could be obtained. Composite materials were selectively etched in reactive gas atmospheres achieving aspect ratios up to 100.

These characteristics are very attractive for future VLSI device processing techniques, because FIB provides the flexibility and reliability necessary for explorative work on scaled or entirely new devices. The ability to view, modify and analyze devices in the submicron range has established this technique in three major semiconductor applications of industrial relevance: device modification, failure analysis, and process monitoring.

The initial results shown prove the flexibility of the FIB for nanostructuring of microcircuits and suggest the relevance of this technique for the development of entirely new devices.

2. Experimental

All the experiments reported were performed on a Micrion 2500 FIB system operating at 50 kV acceleration voltage with a Ga liquid metal ion source (LMIS). The system allows the use of an ion beam with currents ranging from 1 pA to 11 nA, with a beam diameter of 5 nm (FWHM), respectively 500 nm (FWHM) for the high current mode. The energy of the ion beam can be varied between 15 and 50 keV in steps of 5 keV. The system has an additional charge neutralization electron flood gun system which guarantees higher beam stability and ESD prevention.

The stage allows translation of the sample ± 38 mm perpendicular to the beam, 360° continuous rotation, and tilting of the sample up to 60°.

The vacuum in the recipient ($p < 10^{-7}$ Torr) is maintained by a turbo molecular pump backed by a remote mechanical pump to guarantee hydrocarbon free vacuum.

The precursor gas for the tungsten deposition was $W(CO)_6$ respectively trimethyl-cyclotetrasiloxane (TMCTS) and oxygen for SiO_2 formation. All depositions were performed at room temperature. For enhanced etching, XeF_2 and Cl_2 could be introduced through a nozzle. The process conditions for deposition and gas assisted etching are summarized in Table 1.

Table 1: Process parameters

FIB	Gaseous component	Accel. voltage	Beam current	Minimum spot size	Pixel dwelltime	Pixel spacing
		kV	pA	nm	µs	µm
GAE (Fig. 1)	XeF_2	50	1575	100	0.5	0.15
W-depo. (Fig. 1)	$W(CO)_6$	50	700	65	0.5	0.11
GAE (Fig. 2)	Cl2	50	1575	100	0.5	0.15
W-depo. (Fig.3)	$W(CO)_6$	50	5	8	0.5	0.11

3. Measurements and Results

3.1 Device modification

This tool provides as well the potential to fabricate novel circuit layouts directly without the necessity for a sophisticated mask layout and will foster the development and introduction of new IC designs.

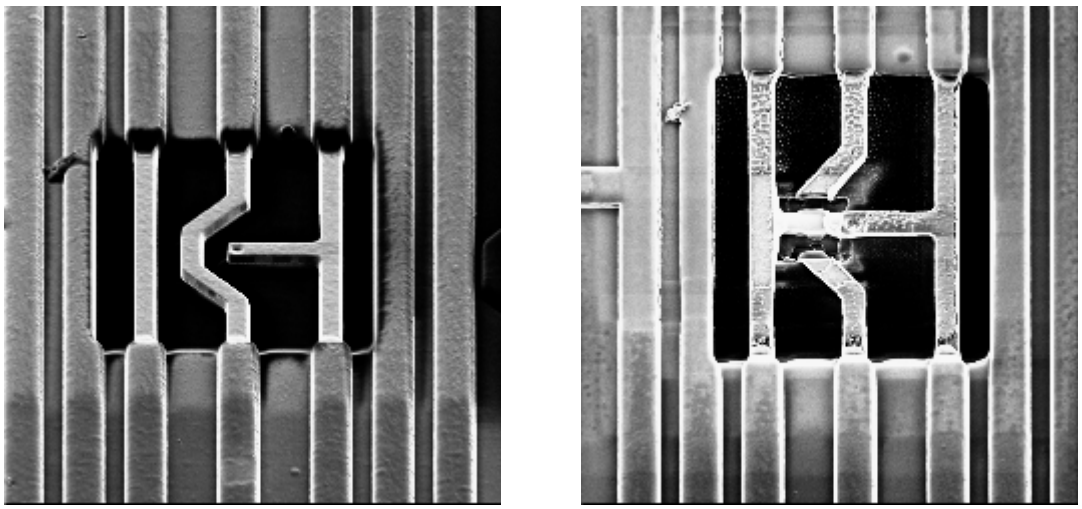


Fig. 1: Sample device modification by isolation cut and rewiring with tungsten deposition.

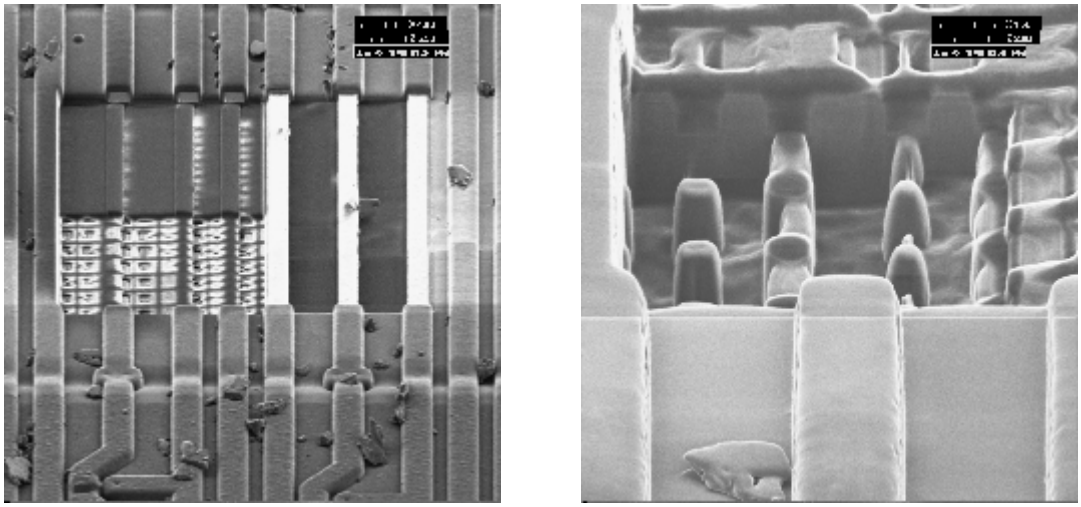
Beyond the analytical capabilities, a combination of deposition and etching steps for metals, semiconductors and insulators allows the direct construction of prototype microelectronic devices. In this operation mode the in-situ modification of circuits directly on the chip was demonstrated (Fig. 1). After the selectively removal of the passivation layer by gas assisted etching the wiring of an exemplary device was locally remodeled by first disconnecting the existing structure with subsequent redeposition of tungsten.

3.2 Failure Analysis

Failure analysis utilizes the capability of FIB technology to access and image structural details hidden beneath the surface. Knowledge of the wiring and type of the composition allows to identify the source of failure.

Using an exemplary microelectronic device the analytical feasibilities of the FIB were exploited revealing an imaging resolution down to 5 nm. By ion milling and gas assisted etching, multilayered structures could be made accessible for investigation within a few minutes and without further laborious preparation. In-situ cross-sectional imaging is highly beneficial in a multilayered fabrication sequence as it allows quick evaluation and interpretation of process steps.

Figure 2 shows a preparation sequence of an integrated circuit which was exposed to chlorine assisted sputtering. Conductive material and dielectrics could be very well distinguished by the differing contrast of the materials.



(a) (b)

Fig. 2: Sequential preparing steps of an integrated circuit: (a) Removal of passivation layer/metal lines/isolation layer, respectively; (b) cross-sectional preparation of a memory cell array.

3.3 Process development

The most attractive feature of the FIB apart from the high imaging resolution is the ability of metal and insulator deposition. Unfortunately, in all cases these deposits contain influential concentrations of carbon, and oxygen. This affects the resistivity of the deposited metal inasmuch the resistivity of FIB deposited conductors is usually higher compared to pure bulk material.

In situ annealing of the deposition by heating the substrate during the focused ion beam deposition enhances the conductivity nearly equal to the pure metal [1], [2], but could introduce thermal drifts during the deposition process leading to lower pattern accuracy. John Melngailis and coworkers [3] promote a method assigned as laser assisted focused ion beam induced deposition. Thereby a laser heats the area where the ion induced chemical vapor deposition takes place confined to the diameter of the laser beam.

Using a siloxane precursor the FIB offers the capability to deposit insulator materials by ion-beam induced chemical vapor deposition from tetramethylcyclotetrasiloxane (TMCTS) in the presence of oxygen. The variation of the partial pressure of TMCTS respectively oxygen and the variation of dwell- and refresh time allow the variation of the stoichiometric composition. Hence, insulating layers with adjustable optical and electronic properties can be evolved. Such insulating materials formed by ion beam induced CVD mainly consist of Si, O, but may contain trace impurities of Ga (from the LMIS) and C by fragmentation of the silicon precursor [4]. The optical transmittance and electrical properties of the layers are mainly controlled by the amount of enclosed Gallium.

The comprehensive understanding of the deposition process will allow to improve the electrical properties of FIB deposited insulators providing the required reliability for performing circuit modifications. Baker [4] suggested metal-insulator-metal capacitor structures with FIB insulators to test the influence of enclosed Ga with regard to resistivity and breakdown voltages.

Figure 3 displays a capacitance test structure (a) formed by SiO_2 deposition between two metal pads. This setup allows monitoring of leakage current, breakdown voltage, dielectric strength and resistivity for dielectric layers feasible.

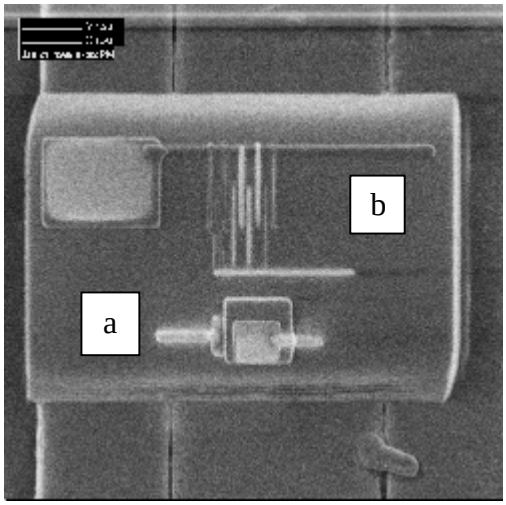


Fig. 3: Capacitor test structure (a) and interdigitated tungsten-fingers (b) with a 220 nm pitch placed on an in situ generated SiO_2 pad.

In general, new materials will be occasionally introduced and the deposition process needs to be adapted in respect to the available precursors, beam energy, refresh- and dwelltime etc. to achieve the desired resistance, dielectric strength, contact resistance and interconnect properties (ohmic or rectifying).

The installation of routine test vehicles is projected for systematic investigation of the morphological and electrical features obtained for specific deposition parameters. The deposition process was found to strongly affect the line width, nesting tolerance, contact hole sizes, etc., and yield of structures. Unified test vehicles provide a suitable mean for gaining a thorough understanding of the complex deposition mechanism.

First test structures (Fig. 3) fabricated by FIB deposition were interdigitated fingers with a 220 nm pitch (b) and metal-insulator-metal capacitor structure (a) to determine conductor to conductor shorts, surface and interfacial leakage currents respectively the dielectric strength of the SiO_2 layer. The highest performance in resolution and pattering achievable was 5 nm respectively 30 nm.

3.4 Shallow implantation

Recent applications of FIB for semiconductor devices focus on an optimized MOSFET (FIBMOS) using the localized beam to fabricate a unique, laterally tailored doping profile along the channel. The arrangement of Ga-LMIS in combination with the high resolution ion column and adjustable beam energy in the range from 50 keV to 15 keV allows generating a strategically placed ultrashallow doping profile with tolerable crystal distortion. Former investigations [5] confirmed that the output resistance improves, detrimental hot electron effects diminish and threshold voltage stabilizes as channel length is reduced, which in general leads to significantly better device performance.

4. Conclusion

Concluding the presented material illustrates the potential of FIB for metrology and highly resolved 3-dimensional imaging of complex multilayer structures. Spatially confined doping and deposition of metal as well as insulating layers was demonstrated in spatially confined areas in the nm range. Concluding, FIB is a prospective tool for the improvement of high-frequency devices as well as fabrication of entirely new circuits.

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Enhanced Energy Resolution in Ballistic Electron Emission Microscopy Through InAs Base Layers

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Ballistic Electron Emission Spectroscopy (BEES) and Ballistic Electron Emission Microscopy (BEEM) offer the unique possibility of probing subsurface quantum states. To improve the spectroscopic sensitivity, it is important to increase the amount of electrons which are able to penetrate into the sample. In this work we show that the transmission coefficient and the attenuation length of the base layer can be enhanced by more than one order of magnitude, if the commonly used thin metal film is replaced by a molecular beam epitaxy (MBE) grown InAs layer. At low temperatures (T = 100 K), a passivated InAs layer yields an attenuation length in the order of 70 nm – 90 nm instead of 5 nm obtained on Au films.

During the last years, scanning tunneling microscopy (STM) and related techniques have evolved as powerful tools in the investigation of surfaces [1], [2]. With the introduction of ballistic electron emission microscopy/spectroscopy by Kaiser and Bell [3], [4] the unique spatial resolution of the STM has been combined with the possibility of local probing the electronic structure of sub-surface interfaces.

In typical BEEM experiments, the ballistic electron current is in the low pA range and thus, the transmission coefficient though the metal base becomes a limiting factor for spectroscopic resolution. If buried structures, such as minibands in superlattices, shall be investigated [5], the ballistic electron current through the superlattice will be smaller by at least one order of magnitude than e.g. for an Au-GaAs Schottky diode. In this work, low temperature BEEM studies are carried out on MBE grown InAs-GaAs heterostructures, where a degenerately n-doped InAs layer replaces the commonly used metallic base. At appropriate growth temperatures (550 °C) a closed and suitable flat InAs layer was achieved. Due to the large lattice mismatch between InAs and GaAs (7.2 %), such layers are strained, but as shown by Ke and coworkers [8] the strain is fully relaxed by dislocations for film thickness above 33 monolayers. InAs carries the unique advantage of a surface accumulation layer. For this reason, insulating surface depletion barriers like on other semiconductors such as GaAs or silicon do not play a role.

InAs-GaAs heterostructures with InAs film thickness between 160 nm and 300 nm were investigated. Bar-shaped InAs mesas (0.3 mm x 2.5 mm) were defined by photolithography and using a wet chemical etchant. Then, a In-Sn back contact was alloyed in forming gas atmosphere. A second etch process was made to obtain different InAs film thickness, followed by a polishing and passivation process based on an aqueous $P_2S_5/(NH_4)_2S$ solution originally introduced for GaAs [6]. Finally, an In-coated Au-wire was attached to establish an ohmic contact to the InAs layer. More details on this passivation process will be published elsewhere [11]. At room temperature, the internal resistance of the InAs samples was too low for reliable BEEM current detection and thus

the STM head was put into a cryostat and slowly cooled to lower temperatures. For the present experiment, a temperature of T = 100 K was chosen, since this provides convenient STM operation conditions. All experiments were performed using Au tips and a tunnel current of I_T = 1 nA at a initial bias voltage V_{Bias} = 2 V. The electronic circuitry for measuring the BEEM current is described in [7].

In contrast to the data of Au-GaAs reference samples, two onset voltages are clearly visible in typical BEEM spectra. The lower onset voltage in Fig. 1(a), V_b = 0.65 V, is the threshold voltage for ballistic electrons overcoming the barrier at the InAs-GaAs interface in the Γ-valley. Using BEEM, Ke and coworkers [8], [9] have studied the properties of InAs-GaAs heterojunctions as a function of the InAs thickness, however, still with an Au-base layer on top. They found that the barrier height at the InAs-GaAs interface depends on the thickness of the InAs film and decreases non-linearly from 0.9 eV at a thickness of one monolayer to 0.63 eV at 33 monolayers. Above that thickness, a constant barrier height was obtained in their work indicating that the strain in the InAs film is fully relaxed. The onset voltage of V_b = 0.65 V in our work is in excellent agreement with their data. The second threshold at higher bias, V_L = 0.79 V, can be associated with the onset of ballistic electron transport through the L-valley of the InAs film. The L-valley of GaAs cannot be associated with the observed current onset at V_L, since it is much higher in energy in our samples. A third onset at somewhat higher bias voltages due to ballistic electron transfer into the L-valley of GaAs, however, could not be resolved in the present experiment.

To analyze the data in more detail, a modified Bell-Kaiser [4] model was applied. In addition to the original model, we also included electron transmission through Γ and L-valley of InAs, quantum mechanical reflection[10] at the GaAs-InAs barrier and a experimentally measured voltage dependent tip-sample separation [11]. For the InAs film, a bulk-like bandstructure was assumed. The effective masses in Γ and L valley were taken from [12]. Nonparabolicity effects were neglected since their influence on the calculation was found to be relatively small. Phonon assisted interface scattering is supposed to play a major role in our samples, and thus, the strict $k_{//}$ conservation rules were relaxed in our calculation. As we have included electron transmission through the Γ and L-valley of InAs in our model, the onset voltages V_b and V_L as well as the transmission factors through the Γ and L valley, t_Γ (= 0.7 %) and t_L (= 6 %), are obtained independently. Fig. 1(b) shows the transmission of an InAs film as a function of film thickness (T = 100 K). For reference purpose, the transmission of different Au-films (T = 300 K) is shown also. Note that the attenuation length of Au is almost independent of temperature and changes only in the order of 10 % between T = 300 K and T = 77 K (see Ventrice [13] e.g.). As one can see, the transmission of an Au-film is considerably smaller than the transmission of an InAs film. For the InAs film itself, the transmission through the L-valley is found to be 8.6 times larger than through the Γ-valley for all film thicknesses. From these data, the attenuation length of ballistic electrons, λ_a, can be determined. For this purpose, the ballistic electron current I_{BEEM} is expressed as

$$I_{BEEM} = I_T t e^{-d/\lambda_a} \tag{1}$$

where I_T is the tunneling current, t the transmission coefficient of the base layer obtained from the Bell-Kaiser model and d the film thickness. From this procedure, we obtain values of λ_a = 4.6 nm for gold, 46 nm for the InAs Γ-valley and 70 nm for the InAs L-valley, respectively.

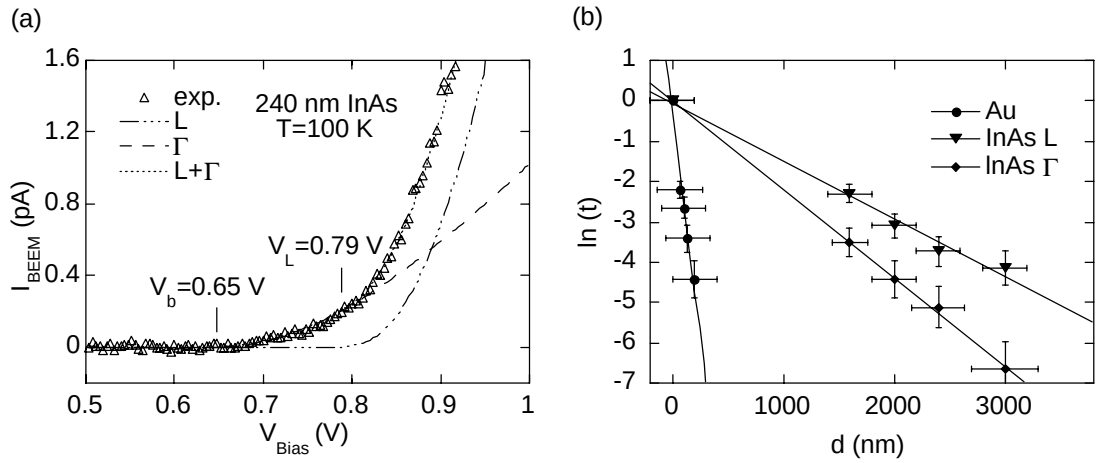

Fig. 1: (a) Representative BEEM spectrum for a 240 nm InAs layer. (b) Transmission coefficients for ballistic electrons through an Au-film (T = 300 K) and the Γ and L-valley of InAs (T = 100 K).

The attenuation lengths in InAs are approximately one order of magnitude larger than in Au and moreover, the attenuation length in the L-valley is approximately 30 % larger than for the Γ valley. For the Γ valley, the large attenuation length is qualitatively understood by low electron-electron scattering rates, due to the low carrier concentration in the InAs film compared to a metal film. The large transmission coefficient and the large attenuation length for electrons passing the L-valley of InAs, however, is somewhat surprising and needs a more detailed discussion. In our opinion, the process can be explained as follows: To be transmitted ballistically through the InAs L-valley, the electron has to undergo at least two scattering processes. First, the electron has to gain a large k-vector, necessary to enter the L-valley of InAs which is located at the boundary of the Brillouin zone in k-space. After the electron has reached the InAs-GaAs interface, a second scattering process is necessary to enable the transfer from the InAs L-valley into the Γ-valley of GaAs. Electron transfer into the L-valley of GaAs will only occur at higher energies and was not observed in the present experiment.

The second major advantage of InAs, or in general semiconductor base layers, results from the low effective mass. Due to the large electron mass difference in Au and GaAs, parallel momentum conservation leads to considerable electron refraction at the Au-GaAs interface. As a consequence, the energetic distribution of the ballistic electron current is inverted beyond the interface and the corresponding energetic resolution is considerably decreased. For InAs-GaAs heterostructures, however, this is not the case, since the effective mass in InAs is smaller than in GaAs. Consequently, the energetic distribution of the ballistic electron current is focussed beyond the InAs-GaAs interface and the energetic resolution of the measurement is enhanced.

In summary, we have performed BEEM studies on InAs-GaAs heterostructures, were the commonly used metal base was replaced by an degenerately doped InAs film. We have demonstrated that the BEEM current and the attenuation length of ballistic electrons is enhanced by approximately one order of magnitude on this samples. It is found that this enhancement is due to lower scattering rates in the Γ-valley of InAs and also to a large contribution of ballistic electrons passing the semiconductor base through the InAs L-valley. This enhancement of the BEEM current is beneficial for all applications,

where the BEEM signal is expected to be small such as for the investigation of buried superlattices or self assembled quantum dots.

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Onset of Scattering Induced Miniband Transport

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A systematic study of electron transport in undoped GaAs/GaAlAs superlattices is presented. Hot electron spectroscopy is used to measure the superlattice transmittance at different bias conditions. The transmittance of a five period superlattice is found to be independent of the direction of the electric field, while for a superlattice larger than ten periods, a dependence of the transmission on the electric field direction is observed. The onset of scattering induced miniband transport is clearly evident. From the experimental data a coherence length of 150 nm is derived. The limiting mechanism is found to be interface roughness scattering.

1. Introduction

Decreasing the barrier thickness of multiple quantum well structures leads to a stronger coupling between the degenerate eigenstates in the wells and thus to the formation of superlattice minibands. The application of an external electric field parallel to the growth axis quantizes the energy continuum associated with the miniband dispersion into a Stark ladder of discrete energy levels, and transforms the extended Bloch waves into strongly localized wave functions. Under strong localization coherence will be reduced to a few periods and in the limit, to a single quantum well.

Numerous studies of the formation of superlattice minibands have been reported including transport measurements of biased n-i-n superlattice structures. However, it turns out that the experimental study of electronic properties of a biased superlattice is hindered by the interdependence of the intensity of the current injected and the field present in the superlattice [1]. At high electric fields the large current densities make the field in the superlattice non-uniform and causes the formation of high field domains and leads to thermal saturation of miniband transport [2].

In this work we present a study of ballistic transport in nominally undoped GaAs/$Ga_{0.7}Al_{0.3}As$ superlattices, where the influence of electron-electron and electron-impurity scattering can be neglected. Under flat band conditions the eigenstates of the periodic structure are expected to be extended over the entire length of the superlattice. We apply the technique of hot electron spectroscopy to measure the positions of the minibands and to investigate the transmission of hot electrons in biased superlattices.

2. Experiment

A three terminal device is used to probe the transmittance of undoped GaAs/GaAlAs superlattices. An energy tunable electron beam is generated by a tunneling barrier and passes the superlattice after traversing a thin highly doped n-GaAs base layer and an undoped drift region. The measured collector current reflects the probability of an in-

jected electron to be transmitted through the superlattice. The transmittance of the superlattice can be measured directly at given superlattice bias conditions by varying the energy of the injected hot electrons independent from the superlattice bias.

Our samples, grown by molecular beam epitaxy, have the following common features: A highly doped n^+-GaAs collector contact layer ($n = 1x10^{18}$ cm^{-3}) is followed by a superlattice and the drift regions which are slightly n-doped ($5x10^{14}$ cm^{-3}). This is followed by a highly doped ($2x10^{18}$ cm^{-3}) n^+-GaAs layer (base) of 13 nm width. On top of the base layer a 13 nm undoped $Ga_{0.7}Al_{0.3}As$ barrier is grown followed by a spacer and a n^+-GaAs layer, nominally doped to $n = 3x10^{17}$ cm^{-3}, in order to achieve an estimated normal energy distribution of injected electrons of about 20 meV. Finally, a n^+-GaAs contact layer ($n = 1x10^{18}$ cm^{-3}) is grown on top of the heterostructure to form the emitter.

In Fig. 1 the calculated conduction band diagram is shown for typical bias conditions. The miniband positions (indicated by shaded areas) are calculated using a self consistent Schrödinger calculation. The static transfer ratio $\alpha=I_C/I_E$ of a five period superlattice with 2.5 nm AlGaAs barriers and 8.5 nm GaAs wells is plotted as a function of the injection energy. The position of the first peak coincides very well with the calculated position of the first miniband. The second observed peak is shifted 36 meV to higher injection energies and is ascribed to the first LO-phonon emission replica ($\hbar\omega_{LO}$ = 36 meV) of the injected electron distribution. The peak at 150 meV represents transport through the second superlattice miniband, and the sharp rise of the transfer ratio at 280 meV is due to the transition to continuum.

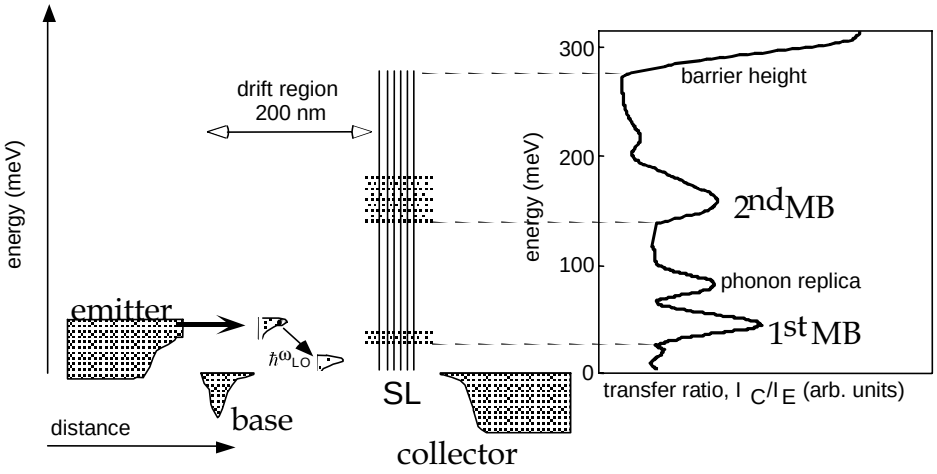

Fig. 1: Calculated conduction band diagram along the growth direction. The transfer ratio of a 5 period superlattice with 2.5 nm barriers and 8.5 nm wells is plotted vs. injection energy.

The measured static transfer ratio of a 5 period superlattice with 2.5 nm AlGaAs barriers and 6.5 nm GaAs wells versus injection energy is shown in Fig. 2 for different collector biases. The black solid line represents the transfer ratio at flat band condition ($U_{BC} = 0$). The sharp increase of the transfer ratio at about 45 meV coincides very well with the lower edge of the first miniband which is calculated to be 46 meV. A clear shift of the maximum (due to the voltage drop in the drift region) and a reduction of the amplitude of the transfer ratio is observed for increasing collector voltages.

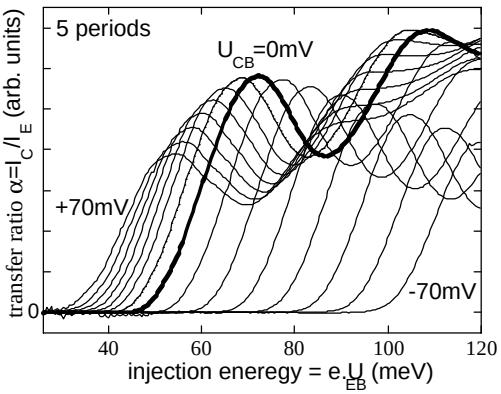

Fig. 2: Transfer ratio versus injection energy at different collector base voltages of a 5 period superlattice with 6.5 nm GaAs well and 2.5 nm AlGaAs barriers. The solid black line represents the transfer ratio under flat band condition ($U_{BC} = 0$).

In order to investigate the transmission of biased superlattices we have taken the total miniband transmission (T_α) which is defined as twice the area of the lower energy side of the first transfer ratio peak as a measure for the average current through the first miniband at given bias conditions. The analysis of T_α versus applied electric field for the five and 20 period superlattices is shown in Fig. 3. The total miniband transmission T_α (dots) of the 5 period sample is symmetric for both bias directions, while clear asymmetric behavior is observed for the 20 period sample (diamonds).

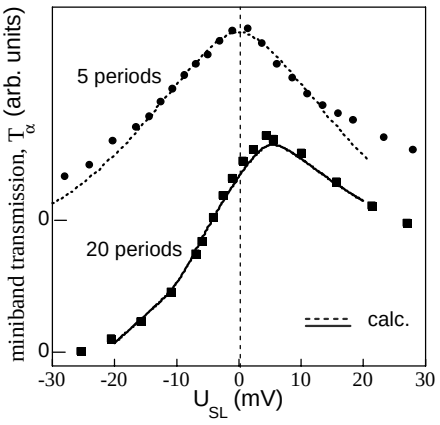

Fig. 3: Miniband transmission versus electric field of the 5 and 20 period superlattice compared to a one- and three-dimensional calculation respectively.

To understand our findings we have performed two different kinds of calculations for the transmission through the superlattice. In a first calculation, based on a transfer matrix method, we consider a 1-dimensional ideal structure with nominal sample parameters. The calculated coherent transmission T_α (dashed line) is in good agreement with the experiment for the 5 period sample as shown in Fig. 3, demonstrating that the transport is dominated by coherent transmission in this case.

However, the picture changes dramatically for the 20 period structure: For negative bias (decelerating field) the measured current decays much faster with field than the one

predicted by the 1-dimensional calculation. For positive bias the current first increases slightly until it decays rapidly but always stays higher than the calculated coherent model.

We assign the observed difference between the 20 and 5 period superlattice to the onset of diffusive transport. For a longer superlattice only a small fraction of the carriers can traverse the structure without scattering. Typically, the scattering process decreases the kinetic electron energy in the transport direction, either by transferring the energy difference to a motion perpendicular to the superlattice-direction (elastic scattering), or by exciting a phonon (inelastic). If a positive bias is applied to the collector, we observe an increase of the transfer ratio since the scattered electrons contribute additionally with the coherent electrons to the collector current. For the negative bias only coherent electrons traverse the superlattice, scattered electrons are flowing back to the base according to the applied electric field. Therefore the presence of scattering destroys the symmetry of the transmission with respect to the field direction. The transition from coherent to diffusive transport is clearly evident.

In order to check this reasoning the results were compared with a second calculation of the transmission through a full 3-dimensional structure where interface roughness is included [3]. As shown in Fig. 3, the calculated transmission (solid line) becomes asymmetric in excellent agreement with the experimental result (diamonds) indicating the limitation of the coherence length due to interface roughness scattering.

Following our reasoning given above, the transmission for negative fields is mainly due to the fraction of electrons traversing the structure without scattering. The average velocity in the miniband is of the order of $\Delta d/(2\hbar) = 1.5 \times 10^7$ cm/s where d is the superlattice period and Δ the miniband width. Using this value in a mean free path of $\ell_{coh} = v\tau_{scatt} = 150$ nm, which is one of the longest reported so far.

In summary, we have used hot electron spectroscopy to investigate the transmission of biased undoped superlattices. The onset of scattering induced miniband transport has been observed and the coherence length has been determined to be 150 nm. We have shown that the coherent transport at 4.2 K is limited by interface roughness scattering.

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Modulation Doped $Si/Si_{1-x}Ge_x$-Field-Effect Transistors

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Modulation doped $Si/Si_{1-x}Ge_x$ samples show high electron mobilities because of the motion of the carriers along a crystalline heterointerface and the absence of ionized impurities in the conduction channel. We present the methods and technologies that are applied at our institute to fabricate field-effect transistors on MBE-grown modulation doped $Si/Si_{1-x}Ge_x$ substrates. Ion implantation is used to form highly doped regions in the substrate; metal evaporation then realizes ohmic source and drain contacts on the implanted regions, and Schottky gates on unimplanted regions. In a following mesa process, reactive ion etching (RIE) is used to isolate the devices on the substrate laterally. The complete transistor process requires six lithographic steps. We employ optical contact lithography for structures down to 0.5 µm and electron-beam lithography for gate lengths <0.5µm. By incorporation of a variety of test structures in our process, we are able to derive the essential device and process parameters after each technology step. For these characterizations we use an HP 4155 semiconductor parameter analyzer and an HP 4284 LCR-meter in connection with an on-wafer prober.

1. Introduction

In a modulation doped $Si/Si_{1-x}Ge_x$ heterostructure, a 2-dimensional electron gas (2DEG) is formed which shows much higher mobilities than the 2DEG in a conventional SiO_2/Si heterostructure [1]. This is for one due to the fact that the charge carriers move along a crystalline heterointerface instead of an amorphous one. In addition, by modulation doping, the doping layer is spatially separated from the conduction channel, so free electrons are provided without having ionized impurities in the conduction path.

Our aim is to test the device applications of modulation doped $Si/Si_{1-x}Ge_x$ heterostructures grown by MBE at our institute. For this purpose we process several test structures up to a modulation doped field-effect transistor (MODFET). These fabrication processes consist of different technological steps [2] which have to be controlled and optimized with respect to the device and process parameters. In this outline we describe the technological steps that are necessary, as well as the different test structures which we employ to get information about our samples.

2. Technological Background

A field-effect transistor requires two kinds of contacts, nonrectifying ohmic contacts and well rectifying Schottky contacts. For an ohmic metal-semiconductor contact, the semiconductor has to be highly doped, so the charge carriers can tunnel through the Schottky barrier. This doping procedure is done by ion implantation, where the ionized dopants are accelerated toward the sample. The doping profile depth is then a function

of the initial kinetic energy of the ions. In a following rapid thermal annealing step, the spatially destroyed lattice is rebuilt and the dopants become electrically active. Metal evaporation then realizes ohmic source and drain contacts on implanted regions and Schottky gate contacts on unimplanted regions of the sample.

When processing several device structures on one sample, they need to be isolated laterally. For this we apply a mesa structuring that defines the shapes of the devices and prevents electrical contacts via the 2DEG between them. This mesa structuring is done by reactive ion etching (RIE), where the Si and SiGe layers are dry-etched in an SF_6 or CF_4 plasma process.

Every technological step requires a mask structuring of the sample, so that only certain regions of it are prepared while the other regions are shadowed. We employ optical contact lithography for the masking process. A photoresist is applied to the sample and illuminated through a photomask. The illuminated regions of the resist can then be removed in the developing process, the remaining resist saves the underlying sample from the technological processing. With these methods of optical lithography it is possible to process Gate lengths of down to 0.5 µm. For preparing smaller Gate lengths, e.g. for high-frequency applications, electron beam lithography is used.

3. Fabrication of Test Devices

To test the material properties of our MBE-grown modulation doped $Si/Si_{1-x}Ge_x$ heterostructures, we developed a simple fabrication process for a MODFET together with different test structures and devices. The complete process requires six lithographic steps, for which we designed a series of masks [3]. These masks are defining the regions on the sample that are implanted, evaporated or etched. They contain the MODFET Source, Drain and Gate contacts, different Hall bars with optional Gates and various test structures to control and optimize single aspects of the whole process (Fig. 1).

For Hall measurements of our samples, two Hall bars of different sizes and a square Van-der-Pauw geometry are prepared. The Hall bars can have optional gates to control the density of charge carriers in the conduction channel. With a transmission line it is possible to evaluate the ohmic contact resistances and the sheet resistance of the conduction channel. The Schottky diodes allow the measurement of the Schottky barrier height of the gate contacts and the leakage currents around the mesa etched structure. On a transistor flute with varying gate lengths the saturation drift velocity of the charge carriers ban be evaluated.

The transistor fields contain several MODFET structures with different gate lengths. A completely-processed transistor with a gate length of 1 µm is shown in Fig. 2. At these structures we derive the transistor parameters and so the direct device application of our samples as a MODFET. For all of the mentioned characterizations we use an HP 4155 semiconductor parameter analyzer and an HP 4284 LCR-meter in connection with an on-wafer prober. The I-V characteristics for a MODFET with a 1 µm Gate are shown in Fig. 3.

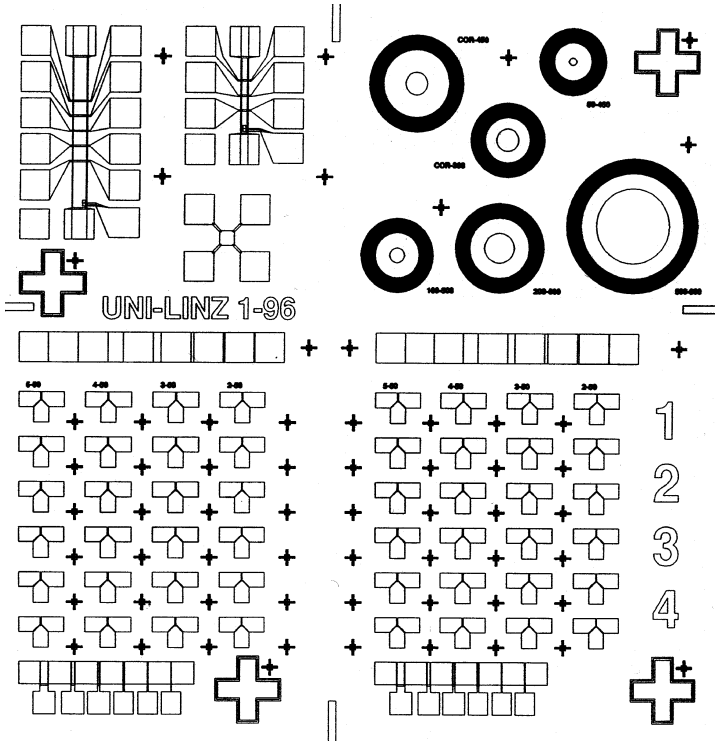

Fig. 1: Overlay of the masks for our MODFET process with six lithographic steps. In the upper left corner the Hall structures are placed, in the upper right corner the Schottky diodes. In the middle there are the transmission lines. The lower half shows the transistor fields and the transistor flutes.

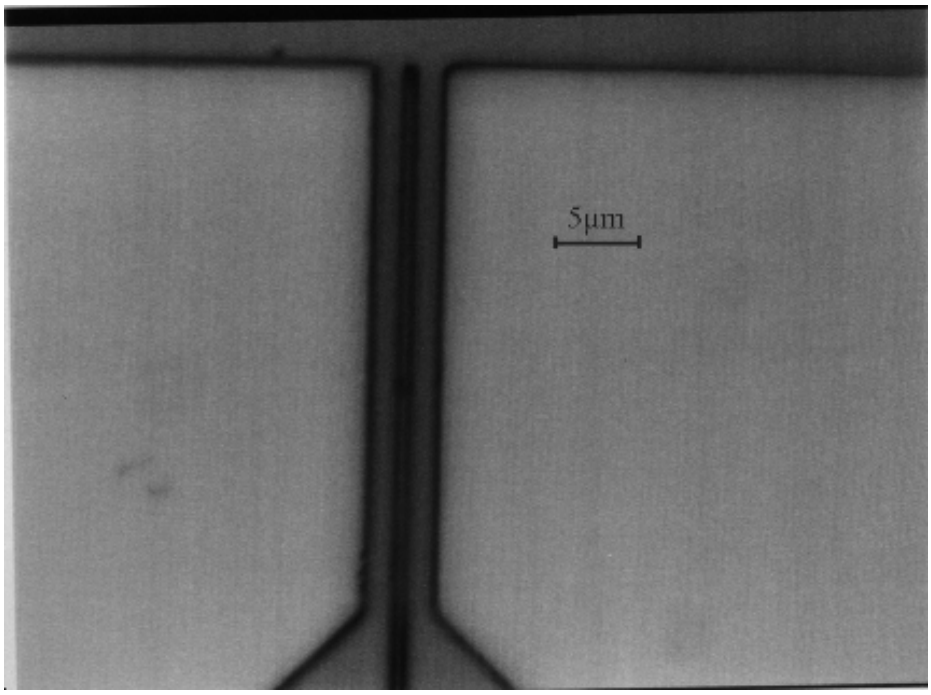

Fig. 2: MODFET with a gate length of 1µm. It is processed on a modulation doped Si/SiGe sample ZSG365 grown by MBE in Linz.

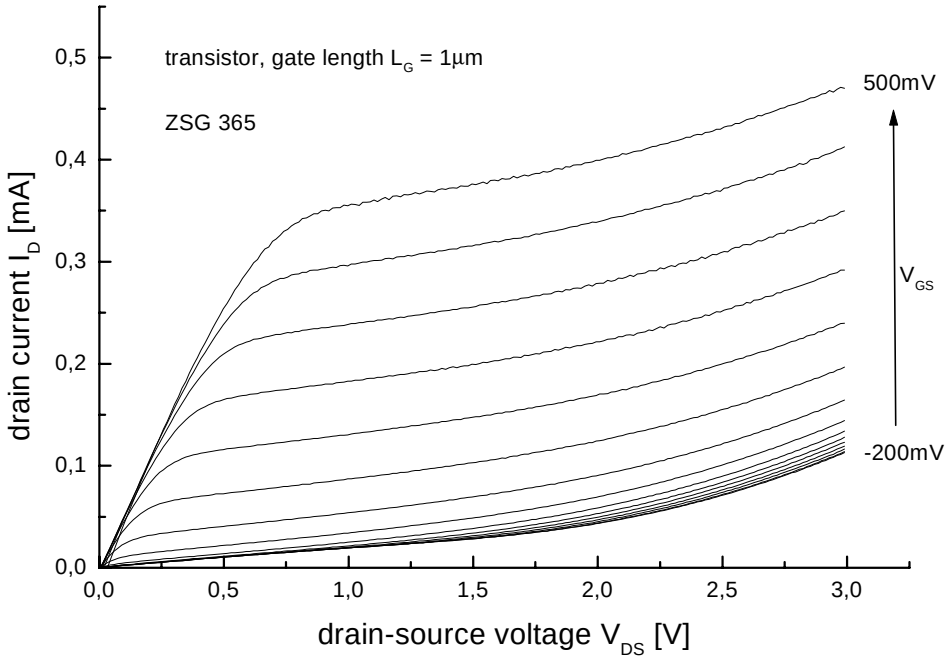

Fig. 3: I-V characteristics of a MODFET with a gate length of 1 µm. This transistor is working in an enhancement mode, so the gate voltage V_{GS} has to be increased.

4. Conclusions

We employ a technological process that allows us to derive the essential material and device parameters of our modulation doped Si/SiGe heterostructures. The test structures and devices can be fabricated in a short time and offer many possibilities for a complete characterization. The device processing can be advanced to Gate lengths <0.5 µm by electron beam lithography, e.g. for high-frequency applications.

Acknowledgements

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Growth Instabilities in Si Homoepitaxy

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We report on a new type of growth instability in Si homoepitaxy that arises from a slight sample miscut. This instability leads to a considerable surface roughness of up to 20 Å on a distance of 250 nm and occurs in a temperature regime frequently used for Si buffer growth. We also provide a recipe to avoid surface roughening.

1. Introduction

The technical relevance of Si (001) surfaces and interfaces caused strong interest and intensive research efforts in their growth properties. The Si surface shows a general tendency for roughening during strained layer heteroepitaxy. Recently, some groups investigate this phenomenon that is commonly known as step bunching and try to amplify it to obtain templates for lateral ordering in subsequent self-organized growth, such as e.g. Ge islands.

The electronic properties of layers resulting from overgrowth are strongly influenced by their interface morphology as carrier scattering from interfacial roughness plays a major role for transport in heterostructure devices. Therefore, ideally flat Si and SiGe interfaces are indispensable prerequisites for optimum performance in present and future Si-based heterostructure devices. It is the goal of our work here to investigate the involved roughening mechanisms on the Si [001] surface and understand their driving forces to allow for the fabrication of interfaces that are as flat as possible and thus ideal for heterostructure devices.

2. Experiment

2.1 Experimental

The samples used for this study were cut from standard Si (001) wafers into 17×17 mm pieces. The substrates have well-defined miscuts of some 1° and 2° along the [100] and 1,5° along the [110] direction, respectively. We used an HF-free standard RCA cleaning procedure before loading them into our Riber SIVA 45 MBE machine. An oxide desorption step at 1000 °C initiates subsequent overgrowth. Si and SiGe layers were deposited at growth rates of 0,2 and 0,8 Å/s and growth temperatures between 350 °C and 750 °C, the layer thickness usually being 1000 Å.

After growth the surface morphology was immediately mapped in ambient air with a Park Scientific atomic force microscope (AFM) in contact mode.

2.2 Results

In Fig. 1, a series of 5×5 µm² AFM micrographs is depicted. The morphology undergoes a quite dramatic metamorphosis within this narrow temperature range: At 450 °C, the surface shows a rather regular terrace structure perpendicular to the miscut direction with an average spacing of 0.25 µm and a height of just a few mono-atomic layers (ML; 1 ML = 1.36 Å). The period is more than an order of magnitude larger than the expected terrace width of 78 Å for equally spaced ML steps leading to a 1° miscut. The slightly undulating pattern is characteristic for the low temperature growth regime and persists at least down to temperatures of 350 °C. At 490 °C, the terrace structure is still present, but it is now covered with triangular features. Those line up almost perfectly along the [100] miscut direction, forming ridge structures perpendicular to the terrace edges. At 550 °C, remnants of the terraces and the ridges remain, but individual triangles can no longer be resolved. Upon further increase of the temperature the feature heights decrease until finally a flat surface results at 750 °C.

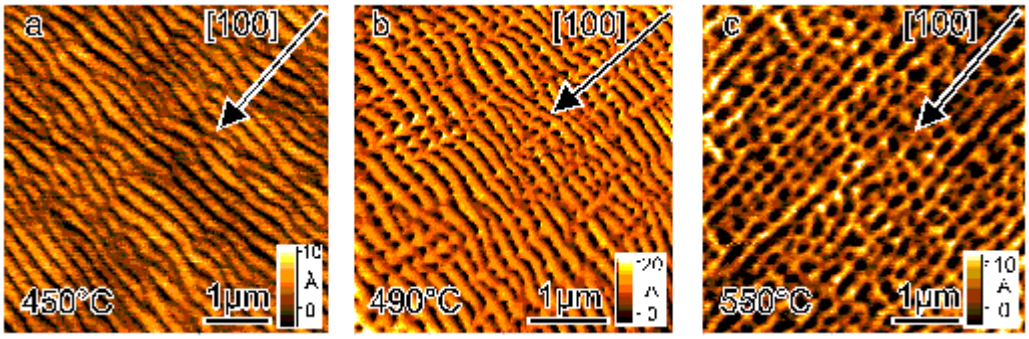

Fig. 1: 5×5µm AFM pictures of samples with 1° miscut along [100]. Films were deposited with 0.8 Å/s at growth temperatures of (a-c) 450, 490 and 550 °C, respectively.

The evolution of the surface morphology was found to depend surprisingly little on the growth rate in the range between 0.2 and 0.8 Å/s studied here. At 0.2 Å/s the features, especially the triangles, become more regular (Fig. 2a), but both the lateral periods and the feature heights remain constant within experimental error.

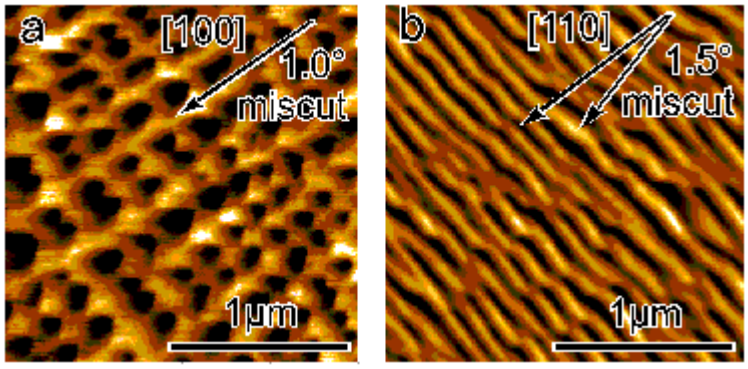

Fig. 2: The surface morphologies resulting from different miscut directions are quite variable. (a) shows a sample miscut 1° along [100], (b) 1.5° along 10° off [110]. Both layers were deposited at 490 °C and 0.2 Å/s to a thickness of 1000 Å.

The influence of the miscut direction was assessed by experiments on substrates having a 1.5° miscut along an in-plane direction 10° off [110]. An example is shown in Fig. 2b next to a [100] miscut reference sample. Obviously, the terraces run perpendicular to the respective miscut direction, but in both cases the terrace edges disintegrate into zigzag arrangements of <110> segments.

For a characterization of the surface morphologies, we extracted the average period widths of the terraces and the average peak-to-valley height variations as a function of the growth temperature, miscut angle and direction (Fig. 3).

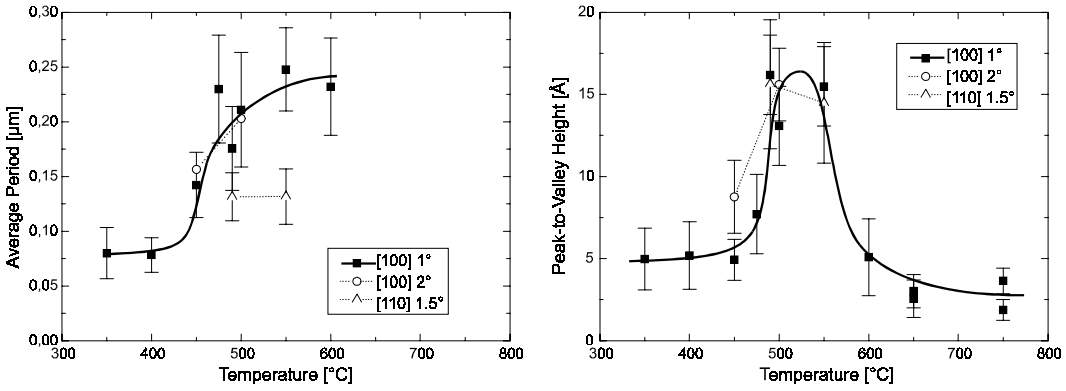

Fig. 3: The evolution of surface features is depicted as a function of growth temperature. (a) shows the development of the feature distance and (b) the height evolution.

The most prominent feature in Fig. 3 is the simultaneous tripling of both the period length and the amplitude over the temperature range. It should be noted that the roughest surfaces result at temperatures being quite commonly used for buffer growth, i.e. 500 –550 °C. Beyond 550 °C the feature height decreases rapidly leading to a surface showing a non-correlated roughness of merely a few Å at 750 °C.

Subsequent annealing for sufficiently long times results in flat surfaces with a rms roughness of about 2 Å and no long-range correlation. Hence, the observed instabilities are kinetically driven and thermodynamically unstable.

RHEED oscillation measurements revealed that the evolution of the surface structures takes place entirely in the step flow regime.

2.3 Discussion

The striking difference in surface morphology between the sample miscut in the [100] and [110] direction gives strong evidence for an influence of the microscopic properties, namely the dimerization of the (001) surface, on the roughness morphology. In the case of a [110] miscut two energetically different terrace edges exist : S_A steps are oriented parallel to the dimer rows on the upper terrace, and S_B steps perpendicular [1]. Initially, growth occurs mainly via S_B steps, since it is energetically more favorable to attach Si atoms to the end of a dimer row, but also because adatom diffusion is estimated to be 1000 times larger along the dimers [2], S_B step growth is mainly fed from the upper terrace as no step edge barrier (Schwoebel barrier) is present. Consequently, at low growth temperatures, S_B terraces are kinetically unstable and grow much faster. Faster

growth in return leads to a larger upper terraces, which again means a larger capture ratio, as compared to S_A type steps. In the end, this instability generally leads to step bunching and rough surfaces (see fig 2b). At somewhat higher temperatures, however, the diffusion perpendicular to the dimer rows becomes enhanced and finally the predominant diffusion asymmetry observed at lower temperatures is overcome, S_A steps advance as fast as S_B steps and the result is a flat surface.

The behavior of the [100] miscut samples is far more complex and not yet fully understood. The <110> segmentation can be understood as caused by "diffusion trenches" along the step edges, where diffusion barriers might be lower and adatoms are highly mobile. The almost perfect alignment of the triangles could be explained in terms of strain fields that are known to be connected with the surface dimer rows.

3. Conclusions

Considering the fact that every wafer is usually specified only within ±0,5° of an exact crystal plane the outcome of our experiments bears important implications for Si-based epitaxy. They clearly show that one has to be very concerned about Si buffer growth. Investigations on strain-induced step bunching should be carried out quite carefully. Bearing in mind that HF cleaned wafers cannot be overgrown at high temperatures because of the formation of SiC precipitates and as a consequence thereof the evolution of a considerable surface roughness. This leaves us in principal with two alternatives : Flat Si buffers on an HF cleaned wafer by either two successive buffer layers the first grown at a low temperature to avoid SiC precipitates to be formed and a second grown at higher temperatures above 600°C to smoothen the surface afterwards or annealing of the substrates after buffer growth. The second viable way to achieve a flat surface is to use RCA cleaned wafers. RCA cleaning leaves a nearly C-free oxidized wafer surface that thus can be overgrown with a Si buffer at temperatures above 650°C. This approach provides the surfaces best suited for heterostructure devices as well as future surface investigations.

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CH_4/H_2 Plasma Etching of IV-VI Semiconductors

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We demonstrate for the first time CH_4/H_2 plasma etching of IV-VI nanostructures. Similar as for II-VI compounds, we find a power law dependence between the etch rate and the energy band gap. However, if other than group IV elements are incorporated in the crystal, the etch rate deviates from this behavior. In particular, for $Pb_{1-x}Eu_xTe$ the etch rates drastically decrease with increasing Eu content, which can be used, e. g., for preferential etching.

1. Introduction

The narrow gap IV-VI semiconductor compounds have major importance for the fabrication of mid infrared optoelectronic devices like lasers and detectors operating in the spectral range between 3 µm and 30 µm [1]. In the fabrication of such devices lithographic patterning and etching are of crucial importance. Up to now only wet chemical etching has been used for the fabrication of buried IV-VI heterostructure lasers. For III-V and II-VI semiconductors, however, it has been shown that plasma etching is superior in several aspects as compared to wet chemical etching. In this work we demonstrate for the first time the feasibility of CH_4/H_2 plasma etching for the structurization of IV-VI semiconductors.

2. Experimental Procedures

Our etching experiments are performed in a Technics Plasma PP300/M barrel reactor operating at 2.45 GHz. The samples are placed in the center of the reactor, which consists of a glass chamber with a total length of 40 cm and a diameter of 24.5 cm. The gas flow through the reactor is controlled by mass flow controllers for CH_4, H_2, and Ar, and the pressure is adjusted at about 0.3 mbar by a control valve to the vacuum pump. The typical steady state temperature of the samples during plasma etching reaches 150 °C. Prior to the etching, photoresist patterns are produced by standard photo lithography. Etch masks are obtained by depositing 500 Å to 1500 Å Cr on the photoresist and subsequent lift-off. For our etch experiments we use several micrometer thick molecular beam epitaxial PbTe, PbSe, and $Pb_{1-x}Eu_xTe$ layers grown on [111] oriented BaF_2 substrates. The etch process was characterized by a profilometer and by examining the etched profiles by scanning electron microscopy.

3. Plasma Etching of Different IV-VI Compounds

In a first set of experiments we etched several different IV-VI semiconductor compounds simultaneously in the barrel reactor. Thus, the process parameters (gas flows of 5 sccm CH_4, and 50 sccm H_2, 300 W rf power, 0.2 mbar pressure in the chamber) were

identical for all samples. The achieved etch depths after 10 min etching time are shown in Fig. 1 as a function on the energy band gap for the binary compounds PbSe, PbTe, and PbS, revealing a systematic decrease of the etch rate with increasing band gap. The experimental data can be fitted by a power law:

$$\text{etch rate}_{\text{IV-VI}}\,[\text{nm/min}] = 50500\ E_{\text{gap}}[\text{eV}]^{-3.2} \quad (1),$$

as demonstrated by the dashed line in Fig. 1.

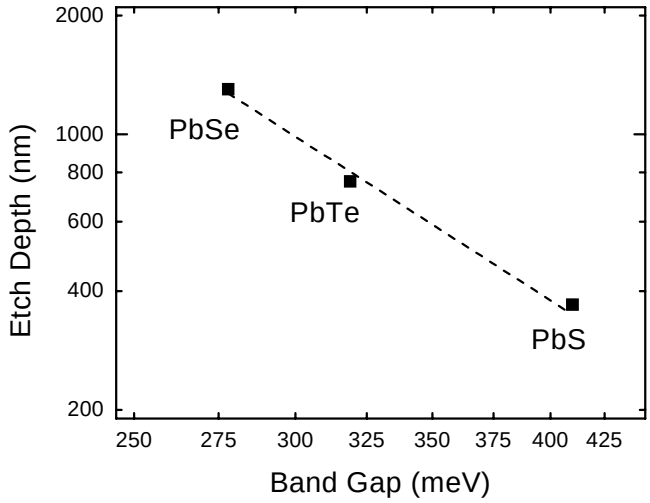

Fig. 1: Etch depth as function of band gap for binary IV-VI semiconductors achieved in a barrel reactor with 5/50 sccm CH_4/H_2 gas flow, 300 W rf power, 10 min etch time and p = 0.2 mbar. The dashed line represents a power law fit of the data.

A similar dependence is also valid for II-VI semiconductors. In our barrel reactor we achieved for CdTe, ZnTe, ZnSe, ZnS:

$$\text{etch rate}_{\text{II-VI}}\,[\text{nm/min}] = 7000\ E_{\text{gap}}[\text{eV}]^{-5.9} \quad (2)$$

This suggests an equivalent etch reaction for IV-VI and II-VI semiconductors. For $A_{II}B_{VI}$ semiconductors the etch process was suggested to be [2]:

$$A_{II}B_{VI} + 2H + 2CH_3 \longrightarrow A_{II}(CH_3)_2 + H_2B_{VI} \quad (3)$$

The H and CH_3 radicals are generated in the plasma [3]. However, the CH_3 radicals can also react to form a polymer deposit [4], so that deposition and etching are always competing processes. As a consequence, the etch rate depends strongly on the CH_3 content in the plasma. The assumption that the B_{VI} component is reacting with the hydrogen was supported by Auger spectroscopy on the etched surfaces [5]. The similar dependence of the etch rate on the band gap energy of II-VI and IV-VI compounds indicates that the reaction in equ. (3) describes also that of the IV-VI compounds just by exchanging A_{II} with A_{IV}. However, when Pb is substituted by other elements such as in ternary IV-VI alloys, the chemical reactions are altered. We find that the etch rate is strongly reduced and the power law dependence does not hold when Pb is partially replaced by Sn, Mn, or Eu.

4. Plasma Etching of $Pb_{1-x}Eu_xTe$

For more detailed investigations of the etching behavior of ternary IV-VI compounds we have focused on the PbTe/$Pb_{1-x}Eu_xTe$ system which is one of the important material combinations for IV-VI laser fabrication. In Fig. 2(a), the etch depth of PbTe and $Pb_{1-x}Eu_xTe$ (x = 1 %) is shown as a function of methane concentration.

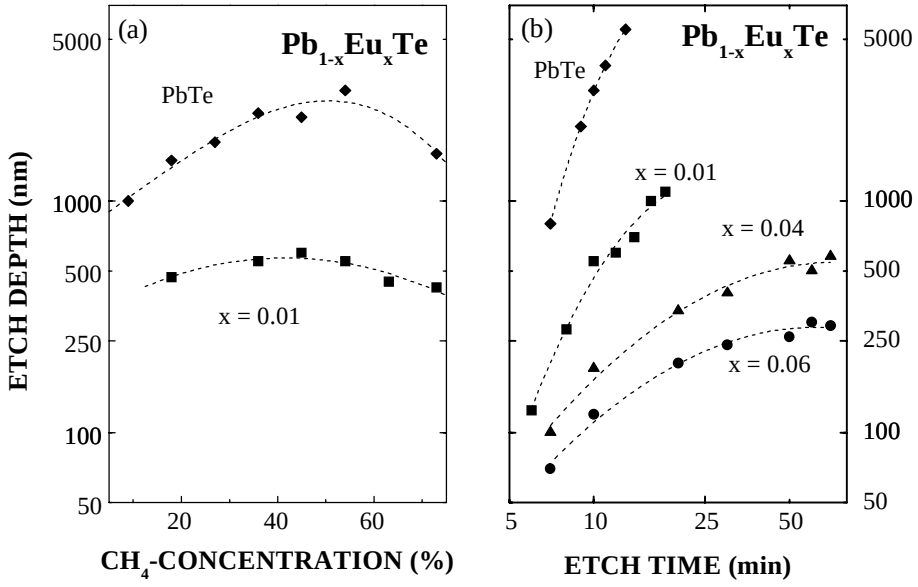

Fig. 2: (a) Etch depth of $Pb_{1-x}Eu_xTe$ after 10 min for a total gas flow of 55 sccm and an rf power of 300 W; (b) Time dependent etch depth for 30/25 sccm CH_4/H_2 gas flows. The dashed lines are guides for the eye.

These results are achieved with a total CH_4/H_2 gas flow of 55 sccm as optimized for this reactor and a rf power of 300 W. With increasing methane concentration the etch depth of PbTe after 10 min increases first from 1000 nm at 10 % CH_4 to 2600 nm at 54 %. Increasing the CH_4 content above 60 % leads to a decrease of the etch depth. This behavior indicates that the etch rate increases with the CH_3 content as long as no polymerization takes place. For PbEuTe (x = 1 %) a similar concentration dependence is observed. However, the etch rate is more than a factor of 3 lower than for pure PbTe and decreases drastically with increasing Eu content (see Fig. 2(b)). In addition the maximum etch rate shifts to lower CH_4 concentrations with increasing x_{Eu}. This could be caused either by polymer formation favored with increasing Eu content or by the formation of non-volatile Eu compounds.

This interpretation is further confirmed by our time dependent etching experiments as summarized in Fig. 2(b). In these experiments, a methane concentration of 54 % is chosen to give a maximum etching rate for PbTe, while the total gas flow and the rf power are the same as in Fig. 2(a). While for PbTe the etch rate is nearly constant in time, the etch rate of PbEuTe decreases more and more rapidly with time with increasing Eu concentration. In fact, for x_{Eu} = 6 % the etching stops completely after 60 minutes due to polymer or non-volatile Eu-compound formation. Fig. 2(b) also demonstrates the very strong dependence of the etching rate on the Eu concentration. For identical etch conditions, the etch depth decreases by a factor of 50 when x_{Eu} is increased from 0 % to 6 %.

Therefore, CH_4/H_2 plasma etching can be used as preferential etch to expose $Pb_{1-x}Eu_xTe$ heterojunctions.

Acknowledgements

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Electron Beam Lithography of Nanostructures

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After a short description of the hard- and software we have used for making the nanostructures, we report on three activities: i) For Si/SiGe modulation-doped field-effect transistors, we fabricate Schottky gates by a lift-off technique with gate lengths below 100 nm. ii) By exposing arrays of boxes with a side length of less than 70 nm and by transferring them via reactive ion etching into a pre-structured Hall bar we produced antidots for magnetotransport investigations. iii) Oxide-patterned silicon substrates are used as a template for selective molecular beam epitaxy. By combining the prepatterned substrates with Stranski-Krastanov growth of Ge or SiGe layers, self-organized quantum dots can be arranged in a regular pattern for selective excitation or contacting.

1. Introduction

For electron beam lithography of nanostructures on Si/SiGe heterostructures we use a JEOL JSM 6400 scanning electron microscope at an accelerating voltage of 40 keV and Polymethylmetacrylat (PMMA) resists with molecular weights between 50k and 950k a.u. The samples are cleaned in acetone and methanol in combination with ultrasonic. On samples with no oxide layer we have used additionally a HF dip to increase the adhesion between substrate and photoresist. Beside the HF dip we have used no other chemicals (like hexamethyldisilicane) to improve the adhesion between substrate and photoresist.

To create the masks and for exposure we have used “Elphy FE 1.233D” from Raith. After a short trial period we have realized some bugs in the “Elphy FE” software which made it necessary to program at least a part of the software by ourselves. The “Nanolithography” package, we have programmed as a supplement for the “Elphy FE” software includes a design part which allows to generate the masks and export them to “Elphy FE”. This solved the problem with instabilities in the mask design part of “Elphy FE”. To improve the exposure quality of periodic dot structures we have implemented a small utility which optimizes the exposure parameters.

As a part of this optimization “Nanolithography” finds the proper combination of working area, working distance and magnification based on databases which include all the technical parameters of the JSM 6400. This optimization takes also into account that the JEOL has only some discrete magnifications and working distances. Without these routines “Elphy FE” would expose either to small or to big structures.

The calibration of the scaling routines has been done with the help of a Park Scientific atomic force microscope. First we calibrated it with a gold grating of known period. After calibration we investigated a grating, which we had exposed with our electron microscope. By comparing the nominal grating period with the real period, we got a correction factor that we use now in the scaling part of the optimization.

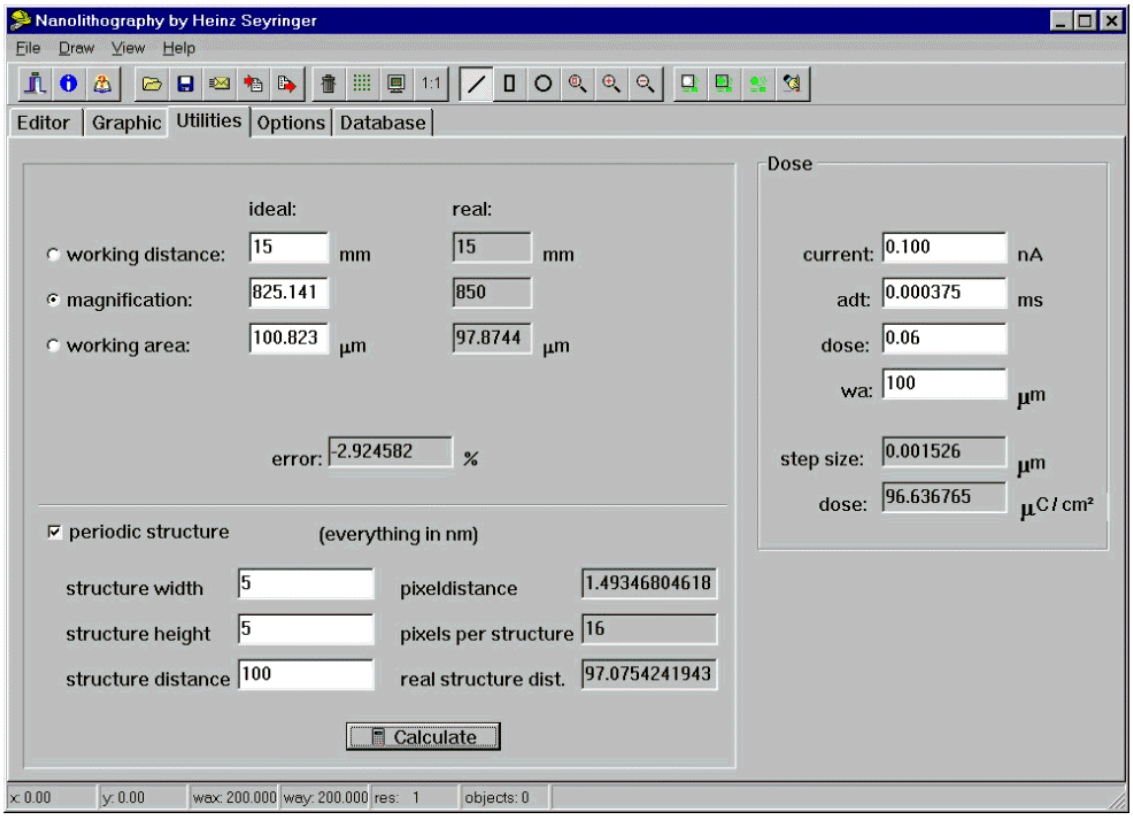

Fig. 1: Utility page of the “Nanolithography” software.

Using this setup we were able to produce holes with a diameter of less than 50 nm in an SiO_2 layer.

2. Modulation-Doped Field Effect Transistors

One of the most important applications of nanostructures is the fabrication of Schottky gates for Si/SiGe modulation-doped field-effect transistors with gate lengths below 100 nm. To align these gates properly we use the mark recognition and alignment system of “Elphy FE”. In the first step of the mark recognition we scan some big marks outside of the transistor structures to make a rough alignment of the mask coordinate system with the sample coordinate system. For the fine alignment we scan four masks in the immediate surrounding of the gate (see Fig.2). These four marks are used to correct the shift, rotation and scaling of the mask coordinate system.

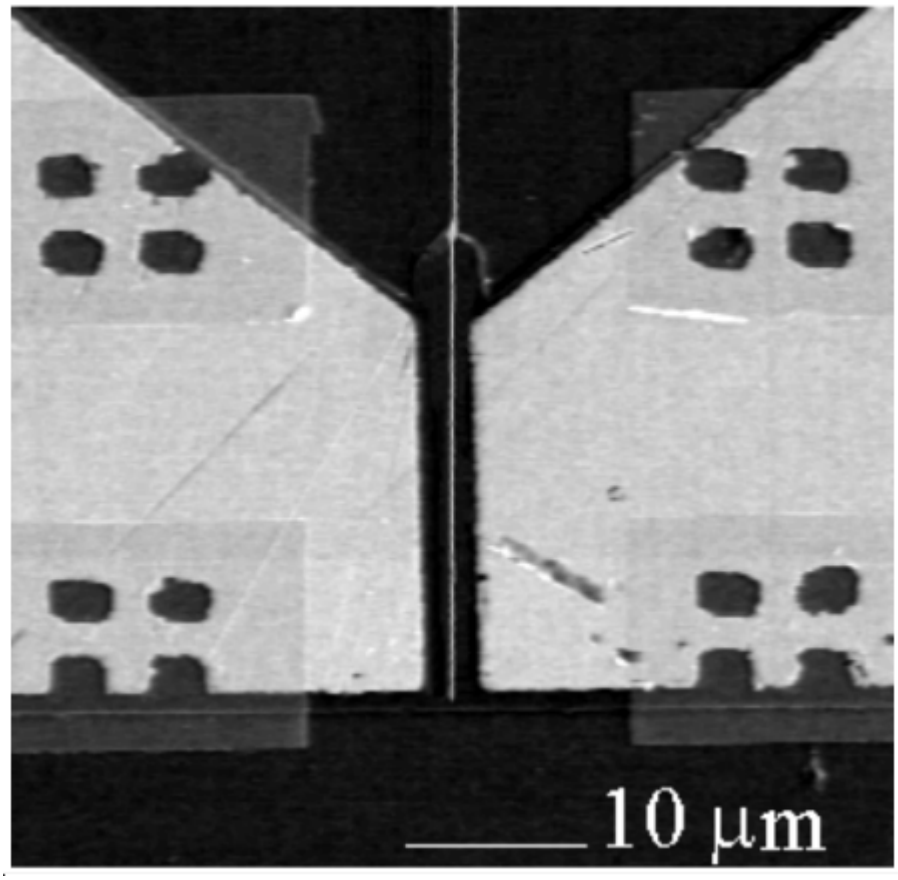

Fig. 2: Schottky gate for Si/SiGe modulation-doped field-effect transistor written by electron beam lithography.

For the lift-off technique it is very important to get negative resist flanks. The usual way to achieve this is by exposing the resist to chemicals like chlorbenzene before it is developed. This makes the top layer of the resist more resistant against developer, which causes the developer to produce slightly negative flanks. The disadvantage of this method is that the chemicals are toxic and that the chemical reaction depends on the surface morphology.

To avoid these problems we have developed a simple but efficient method to create negative flanks. We use the highest possible accelerating voltage - which is in the case of our electron microscope 40 kV - and optimize the exposure parameters for the exposure of structures with dimensions of a few nanometers. Then we expose nominally 5 nm wide gates with a dose that is much to high. A remarkable percentage of the electrons scatters from the substrate-resist interface back into the resist (because of the proximity effect) and causes a much broader exposure distribution at the interface. The result is that we get gates with gate length below 100 nm with negative flanks without any additional chemicals.

To optimize the high frequency behavior of the transistors we investigate multiple resist layers for the fabrication of gates with T- or Γ cross sections. Basically, we use PMMA 50k and PMMA 950k as the two layers. To increase the height of the gates we investigate three layer resist systems with two layers of PMMA 950k on top of a PMMA 50k layer.

3. Antidots for Magnetotransport Investigations

To produce the antidots we have used PMMA 50k and exposed arrays of boxes with side lengths of less than 70 nm. It is important for the magnetotransport investigations that all dots have the same size and shape which means that the astigmatism correction has to be done very precisely. In vacuum there are always some hydrocarbon compounds which can be used for electron beam induced chemical vapor deposition. This deposition occurs only in the region where the primary electrons hit the sample and therefore gives an image of the beam shape which allows a precise correction of the astigmatism.

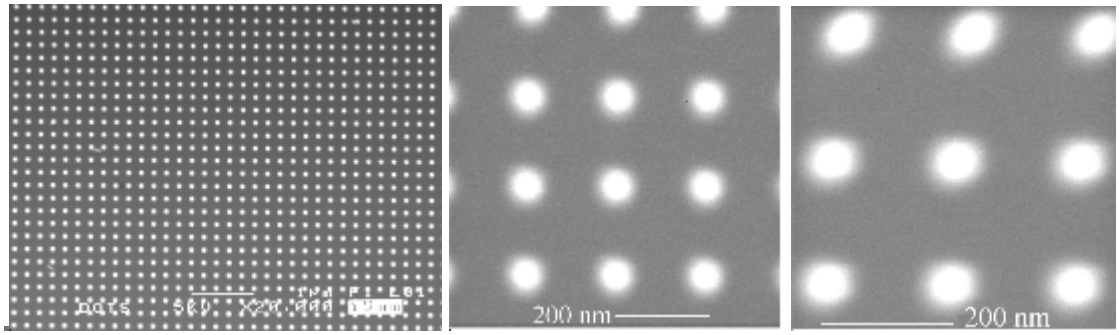

Fig. 3: Picture 3a shows a typical array of antidots. In picture 3b the astigmatism is properly corrected, while there can be seen a small astigmatism in the dots of picture 3c.

To transfer the dots from the PMMA into the silicon we use reactive ion etching (= RIE) with CF_4 gas at a power of 85 W and a pressure of 30 mtorr. The problem of the RIE is that we damage the sample and create depletion regions which have a big influence on carrier density and mobility.

By measuring the magnetoresistance we can calculate carrier density and mobility from the Shubnikov De Haas oscillations. Change in size and period of these antidots will provide information about the damaged area around the anti-dots. This information can be used to optimize the etching process and increase the electron mobility in devices by decreasing the surface scattering.

4. Oxide Windows for Ge-Dot Growth

Oxide-patterned silicon substrates are used as a template for selective molecular beam epitaxy [1]. By electron beam lithography we transferred arrays of windows less than 100 nm wide into a SiO_2 layer. These allow crystalline growth in areas where the substrate is exposed and polycrystalline deposition on the oxide covered areas. The latter can be removed selectively by etching the SiO_2 layer in diluted HF.

These oxide-windows allow the control of dot sizes and arrangements.

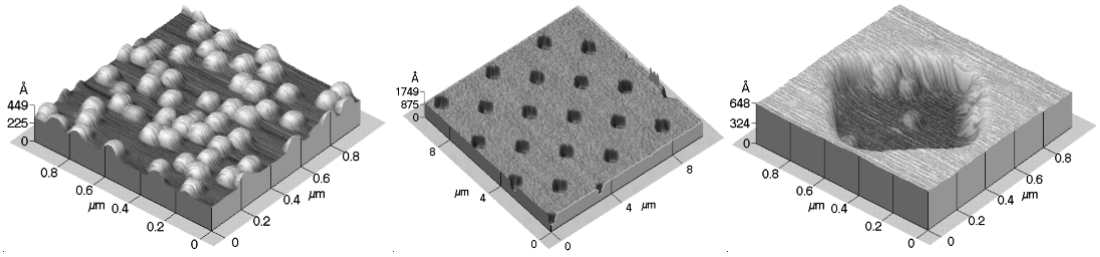

Fig. 4: Ge-dots grown on unpatterned silicon substates have a high density with a random distribution (Fig. 4.a). In contrast, oxide patterned silicon substrates (Fig. 4.b) allow us to control position and size of Ge-dots (Fig. 4.c).

5. Conclusion

With the combination of “Nanolithography 2.0” and “Elphy FE” we are able to produce nanostructures for a multitude of application. Especially the use of antidots in Hall bars for optimizing RIE damage might be of interest for industrial applications.

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Fast Growth Method for the Fabrication of Modulation Doped Si/SiGe Field Effect Transistors

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The fabrication of SiGe-based n- and p-type MODFET structures requires the growth of strained Si or SiGe quantum wells on top of relaxed SiGe buffer layers. In order to achieve a sufficiently low threading dislocation density in the active layers, the concept of SiGe buffers with gradually increasing Ge content was developed. A disadvantage of these buffers is the time required for their fabrication, mostly by MBE or UHV-CVD. We present a novel, fast technique based on DC-plasma enhanced CVD which offers growth rates 10 – 50 times bigger than those obtained with MBE or UHV-CVD. The investigations of graded SiGe buffers by x-ray diffraction, atomic force microscopy and secondary ion mass spectroscopy reveal structural properties comparable to MBE or UHV-CVD grown material.

1. Introduction

SiGe-based MODFET structures have demonstrated device performances superior to conventional Si-based MOSFETs in the field of high-frequency applications. In order to achieve the desired electronic structure, i.e. to tailor the band gaps and band alignment, Si and SiGe channels have to be grown pseudomorphically on top of relaxed SiGe layers. In a tensely strained Si channel on top of relaxed SiGe, the sixfold degeneracy of the Δ-minima of the conduction band is removed. Two of these (Δ_2-minima along growth direction) are lowered in energy and form the quantum well for electrons. As growth is usually performed on the (001) surface, the effective mass of the electrons relevant for the in-plane movement is then the small transverse mass ($m_t = 0.19\ m_0$ for unstrained Si), which is favorable for fast device applications. However, misfit dislocations, which are required for the plastic relaxation of SiGe, are accompanied by threading segments which intersect the active layers and decrease the device performance. It has become a main aim of growth optimization to reduce the threading dislocation densities [1]. The most widely used technique is the growth of SiGe buffers, where the Ge content is graded from zero up to the final concentration of typically 20 – 30 %, followed by a constant composition buffer and the active layers (see Fig.1) [5]. The whole buffer stack has a typical thickness of several µm, and hence the time required with conventionally applied techniques such as MBE or UHV-CVD is considerably large, since the growth rates are typically in the order of Angstrom per second.

A novel growth technique developed at the ETH Zurich in cooperation with Balzers is the so-called "Low Energy DC Plasma Enhanced CVD" (LEPECVD) [2]. With this

method growth rates higher than 50 Ås^{-1} have been demonstrated. We have investigated the structural quality of LEPECVD grown samples by means of x-ray diffraction (XRD), atomic force microscopy (AFM) and secondary ion mass spectroscopy (SIMS). It turned out that the sample quality is comparable to material grown by conventional techniques.

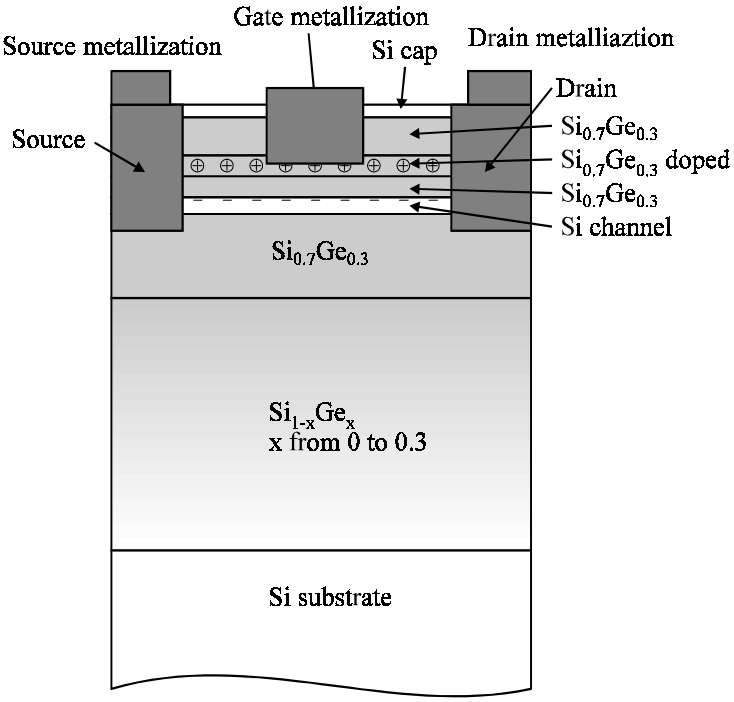

Fig. 1: Scheme of a n-type MODFET grown on a graded SiGe buffer. The layer thicknesses are not on scale, in reality the active layers are much thinner.

2. Experimental

The samples have been grown at the ETH Zurich on (001) oriented Si wafers. HF dipped wafers were loaded into the growth chamber via a load-lock. After outgasing and cleaning in an H-plasma, 100 nm Si buffers were grown at 600 °C, followed by the SiGe buffer layers grown at temperatures between 500 – 600 °C and at rates between 10 – 50 Ås^{-1}, typically. In contrast to conventional CVD techniques, in LEPECVD an intense low-energy plasma (arc discharge voltages of 20 – 30 V DC) is used to decompose the reactive gases SiH_4 and GeH_4 and to enhance the hydrogen desorption on the surface. The energy of the ions impinging on the substrate can be controlled by the substrate bias and usually lies in the region below 10 eV. Details on the method and sample growth can be found elsewhere [2], [3].

XRD reciprocal space maps have been recorded using a triple-axis setup with primary beam divergence and analyzer resolution of 12 arcsec, respectively. From maps around the symmetrical (004) and asymmetrical (224) reciprocal lattice points (see Fig. 2) the strain in the samples could be determined as a function of the Ge content [4].

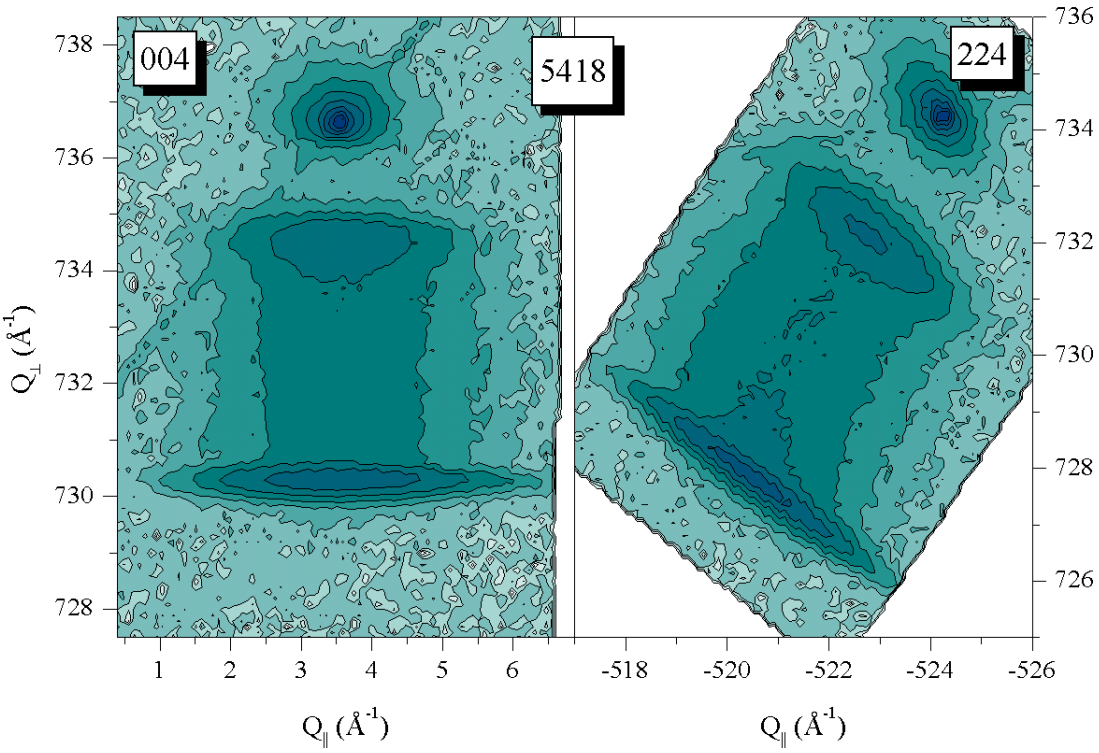

Fig. 2: Reciprocal space maps around the (004) and (224) reciprocal lattice points for LEPECVD grown sample 5418.

Asymmetrical maps have been recorded in different (110) azimuths to detect a possible anisotropy of strain relaxation, but no such effect has been observed. Combining the XRD results with the SIMS profiles of the depth-distribution of the Ge content, finally the strain as function of depth below the sample surface has been determined. Figure 3b shows a typical SIMS profile. From the combination of this profile with the strain data from the XRD maps, finally the strain as a function of depth can be determined (Fig. 3b).

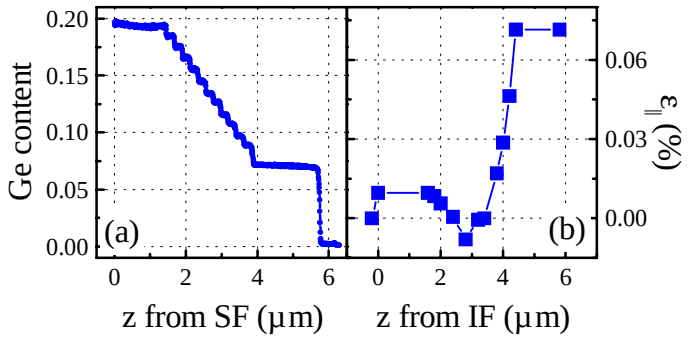

Fig. 3: (a) SIMS profile of the Ge content of sample 5418 as a function of depth below the sample surface. The graded region is grown as a sequence of small steps in the Ge content, which is clearly resolved by the SIMS. (b) Strain distribution of sample 5418 as a function of thickness above the interface between Si buffer and SiGe graded buffer.

As intended, the strain is virtually zero in the lower part of the graded buffer, and increases linearly in its upper part [5]. The constant composition part of the SiGe buffer as well as the active layers have been grown pseudomorphically on top of the graded buffer. Figure 4 shows an AFM image of the surface of a LEPECVD grown buffer layer. The typical "cross-hatch" pattern connected with the extended misfit dislocations within the graded part of the buffer is clearly visible.

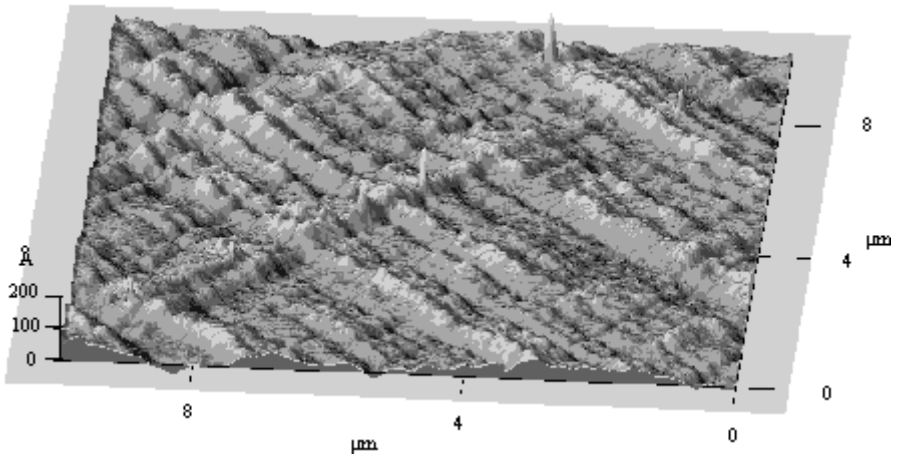

Fig. 4: AFM image of LEPECVD grown sample 5441. The typical cross-hatch pattern connected with the misfit dislocations along {110} directions in the graded buffer is clearly visible.

3. Conclusion

The comparison of these results with measurements on comparable samples grown by MBE shows that the structural quality of LEPECVD grown material is quite comparable to samples grown by conventional techniques. The FWHM along ω-direction in the reciprocal space maps is only slightly larger than in MBE grown samples. The surface roughness of the samples is typically 20 – 30Å (r.m.s. value), also comparable to MBE grown material. Thus LEPECVD seems to be a promising method for the fast growth of SiGe buffer layers for high-speed device applications on an industrial scale.

Acknowledgements

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Si/SiGe Layers on Patterned Substrates for MODFET Applications

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We present a systematic study on the strain status of Si channel in Si/SiGe MOD-FET structures grown on mesa structures with lateral dimensions ranging from 3 to 20 μm, as well of its surface morphology. With decreasing mesa size, the surface undulations flatten and the in-plane strain of the Si channel is decreased.

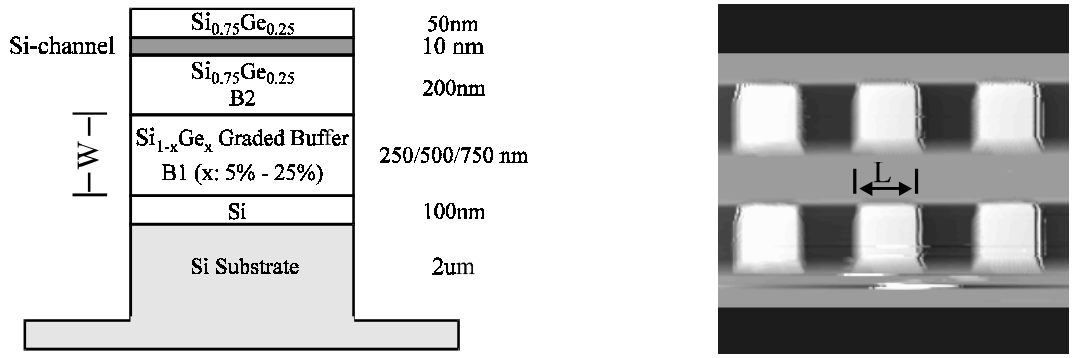
1. Introduction

In Si-channel n-MODFET structures, a two dimensional electron gas is confined in a strained about 100 Å thick Si layer [1]. For tensile strain, the six-fold degenerate conduction band of Si is split into a two-fold $\Delta 2$ and a fourfold $\Delta 4$ state. The confining potential for the electrons in this Si-channel layer is determined by the conduction band offset between the SiGe barrier and the $\Delta 2$ states of strained Si. In order to achieve the desired strain status, usually a graded SiGe buffer layer is deposited on (001) Si, on top of which a constant composition SiGe layer is deposited, followed by the Si channel and finally a modulation doped SiGe layer on top. The grading rate of the Ge content, the thickness of the graded layer (B1) and of the constant composition buffer (B2, see Fig.1) determine the amount of strain relaxation and thus the in-plane lattice constant of the top B2 SiGe layer. The subsequently grown Si channel is pseudomorphic, i.e. biaxially tensily strained with respect to buffer B2. The plastic relaxation of the SiGe buffer layer is through misfit dislocations, the stress fields of which give rise to the roughening of the epilayer and consequently also of the interface to the strained Si layer [1], [2] . The resulting cross-hatch surface or interface morphology has a lateral periodicity of typically 1 μm in the two orthogonal <110> directions, with rms heights of about 20 – 50 Å [2]. Too high values of this surface roughening might be not fully compatible with planar integrated circuit technology.

A concept for Si-based heterostructure devices has been developed, in which such devices could be integrated with conventional Si MOS technology on the same wafer (chip) by growing the layer sequence for heterostructure in selected areas. However, the quality of these devices always suffered from the high density of defects induced by the large lattice mismatch between Si and Ge. It has been found that reducing the lateral dimensions of the growth zone results to a dramatic decrease in the defect densities [3]. In this paper we describe a systematic study both of the strain status of the Si layer containing the 2D electron gas and of the surface morphology as a function of the lateral dimensions.

2. Experimental

The layer sequence as shown in Fig. 1 was grown on arrays of square Si (001) mesa pillars, oriented along the <110> directions, with lateral dimensions of 3, 4, 6, 10, 20 µm and for comparison also on an unpatterened region. The mesas were etched to a depth of 2 µm. By molecular beam epitaxy a Si buffer layer was deposited, followed by the graded SiGe buffer region (5 – 25%, with thicknesses ranging in three sample series from 250, 500 and 750 nm). A 200 nm thick SiGe buffer layer with constant Ge composition was followed by the 10 nm thick strained Si channel and a 50 nm thick SiGe layer for the n-type dopant Sb followed by a Si cap layer. The growth temperature was 550°.



(a) (b)

Fig. 1: (a) Sketch of a MODFET grown on lateral patterned sample; (b) Top view on the sample with (10 * 10) µm^2 mesa size by AFM.

From x-ray reciprocal space maps we have determined the in-plane lattice constant of the top SiGe buffer layer and thus strain status of the Si channel. The data for series of mesas with the 750 nm thick B1 buffer layer are shown in Fig. 2.

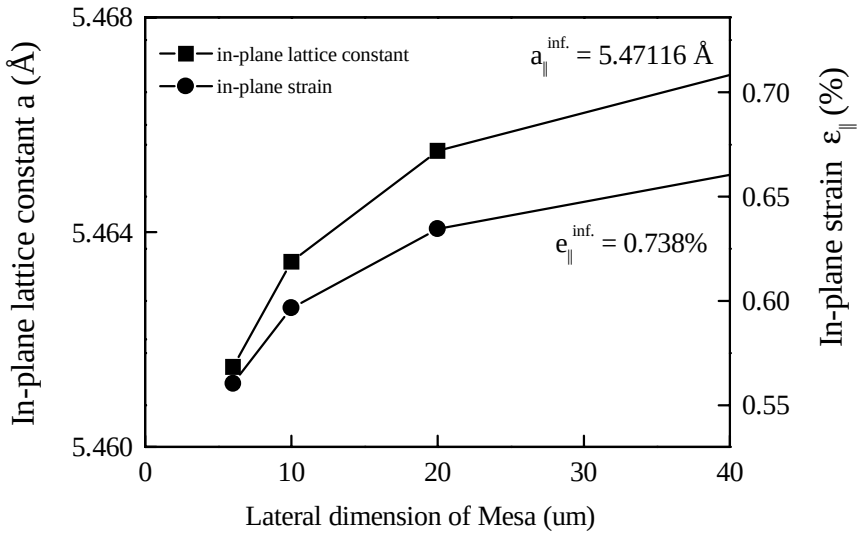
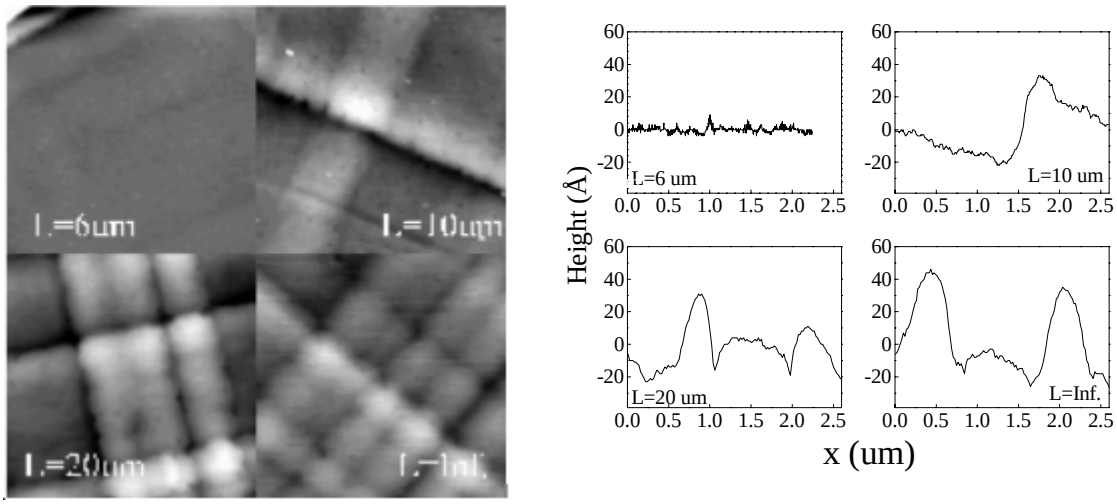


Fig. 2: In plane lattice constant ($a_{\parallel}$) and strain($\varepsilon_{\parallel}$) of Si-channel vs. mesa size. $\varepsilon_{\parallel} = (a_{\parallel} - a_{si})/a_{si}$. a_{si} is the cubic Si lattice constant.

With decreasing mesa size the in-plane lattice constant and thus the in-plane strain in the Si channel decreases, causing a decrease of the confining potential. Below 6 µm mesa size, due to the simultaneous SiGe growth on the Si substrate beneath the etched pillars, the data cannot be reliably interpreted. In Fig. 3 the surface morphology from atomic force microscopy is shown for a samples sequence with mesa sizes from 6 µm to 20 µm and for layers grown on the unpatterned substrate. The line scans exhibit remarkable differences: For the smallest mesa size of 6 µm, in an area of 2.6 x 2.6 μm^2 no cross hatch pattern is visible and the line scan shows a quite smooth surface morphology. With increasing mesa size the troughs and hills due to the cross hatch formation cause the observed surface undulations. However, the smoother surface morphology for mesa size below 10 µm is accompanied with less SiGe relaxation of the SiGe buffer layers, and thus a decreased tensile strain of the Si channel.

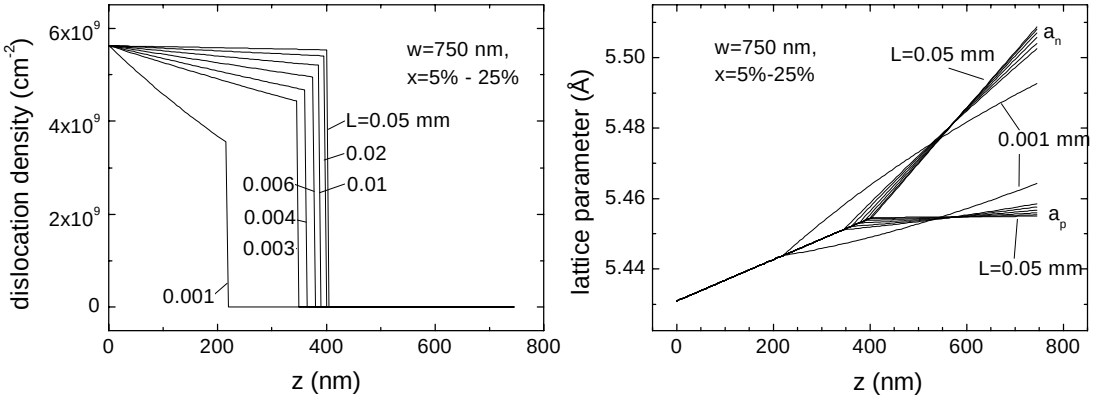


(a) (b)

Fig. 3: (a) Surface morphology of samples with different mesa size from 6, 10, 20 µm and for growth on unpatterned substrate (B1: 750 nm thick). (b) Line scans (height modulation) for these samples.

In principle for the strain relaxation in the SiGe buffers grown on mesas two mechanisms have to be considered which mainly affect the strain in the upper Si layer, namely the elastic strain relaxation due to the limited mesa size, and at the same time the decrease of the misfit dislocation density with shrinking lateral dimension. The first mechanism increases the lateral strain in the Si layer, while the second one decreases it. In order to model these trends we have calculated the dislocation density profile by minimizing the total deformation energy (the elastic energy and the energy due to the line tension of dislocation) on the basis of a phenomenological assumption of the elastic relaxation (degree of relaxation decreases exponentially from the bottom towards the free surface of the mesa). According to Tersoff [4], we obtained this profile as shown in Fig. 4 (a). Limiting the lateral mesa size, we decrease the dislocation density in the relaxed part of the buffer. In Fig. 4 (b) the lattice constant as a function of the z-coordinate in the graded buffer B1 above the Si substrate is plotted for different mesa sizes. One can distinguish regions for which the elastic relaxation dominates (for $z > 550$ nm, for the 750 nm thick graded B1 layer) from regions where the decrease of the dislocation density with decreasing lateral mesa size dominates (for $z < 500$ nm). From the experimental data it follows that actually the second mechanism dominates in the

samples studied. This is actually unfavorable for the total biaxial strain in the Si channel. Apparently for achieving a better correspondence between the calculations and the experimental data a more detailed finite element calculation of the strain status has to be performed.



(a) (b)

Fig. 4: (a) Dislocation density profile vs. depth in the graded buffer B1 for various mesa sizes L. (b) Lattice constants of B1(in plane: a_p and vertical: a_n) vs. z-coordinate. Origin of z-coordinate lies in the interface between Si buffer layer and B1 layer.

3. Conclusion

From the series of experiments on the strain status of Si/SiGe MODFET structures grown on mesa like pillars we draw the following conclusions: For mesa sizes below about 10 µm, the lateral period of the cross hatch pattern is substantially enlarged. The surface undulations are decreased. However, the reduction of dislocation density is accompanied by a decrease of the absolute value of the in-plane strain in the Si channel. In the samples studied, elastic relaxation might alter these conclusions for sufficient small mesa size does not yet play an important role.

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