Scanning Capacitance Microscopy with Zirconium Oxide as High-k Dielectric Material

W. Brezna, S. Harasek, H. Enichlmair, E. Bertagnolli, E. Gornik, J. Smoliner

Scanning Capacitance Microscopy (SCM) is an extension of conventional Atomic Force Microscopy (AFM) and a promising tool for semiconductor device characterization. The main application of this method is two-dimensional carrier profiling for failure analysis and process control. Unfortunately, SCM is not an easy and straightforward technique to use. Quantitative reproducible measurements are a serious problem, since the preparation of the insulator required on the sample surface (up to now exclusively SiO_2) has a dramatic influence on the results, especially in cross sectional measurements. As main problem, standard high temperature industrial oxidation techniques cannot be used because on processed devices, the high temperature broadens all doping profiles or destroys the samples completely. Thus, low temperature oxidation processes have to be used, which usually yield a much lower oxide quality and moreover, are not extremely reproducible.

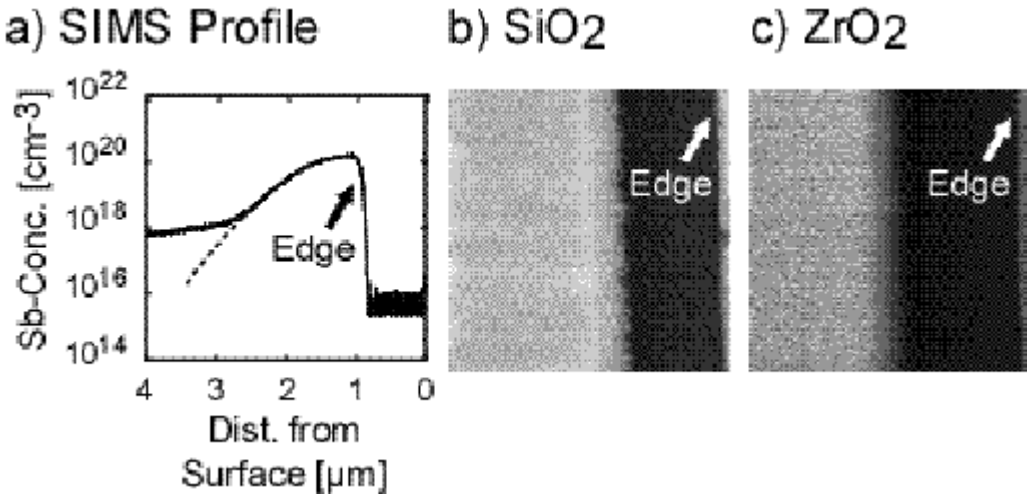

Fig. 1: The dopant profile of the n-type (Sb) region of the investigated pn-junction is plotted in picture a). SCM-images of a SiO_2 coated and ZrO_2 coated junction are shown in b) and c), respectively.

For this reason, we tried to replace the SiO_2 with high quality, low temperature CVD grown ZrO_2, which recently attracted much attention as a possible high-k gate dielectric in microelectronic metal-oxide-semiconductor (MOS) devices, because it is promising to overcome the tunneling limits of SiO_2. The effective dielectric constant of thin and ultra thin films in the range of k = 18, the wide band-gap of more than 5 eV, favorable band-mismatch to silicon and finally high thermodynamic stability on silicon make ZrO_2

a promising dielectric for scanning capacitance microscopy. To gain comparable results, the dielectric thicknesses were adjusted to get the same capacitance for both SiO_2 and ZrO_2 samples, which means that the SiO_2 layers were 4 nm and the ZrO_2 layers were approximately 20 nm thick. The greater thicknesses of the ZrO_2 layers should compensate for the material's bigger dielectric constant. To demonstrate the utilization of ZrO_2 as a dielectric material for SCM measurements, we first compare the SCM images of a pn-junction which were obtained with industrial quality SiO_2 and with ZrO_2 layers grown by CVD (Fig. 1). The pn-junctions were manufactured at Austria Mikro Systeme International AG (AMS) by implanting a highly doped buried layer (Sb) into a low boron (p-type) doped silicon wafer. The dopant profile obtained via SIMS is shown in Fig. 1 a). As one can see in Fig. 1 b), very good contrast was obtained between the p- and n-type regions on a sample with SiO_2 as dielectric. If we compare these data with the results obtained on the ZrO_2 layer, we see in Fig. 1 c) that ZrO_2 can compete easily in terms of contrast generation.

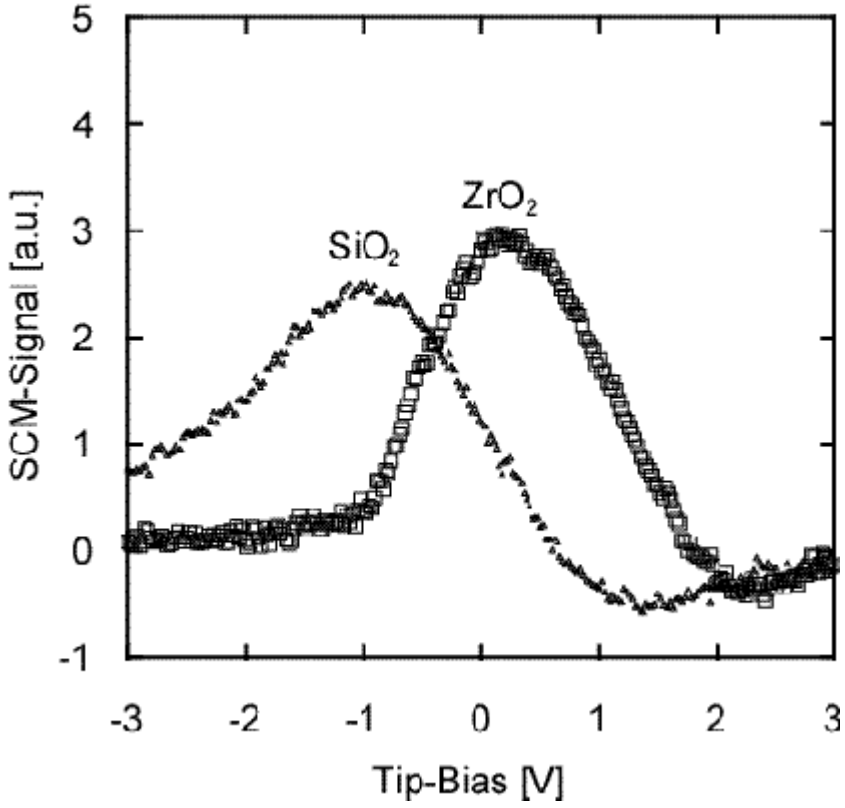

Fig. 2: dC/dV plots of p^--doped samples with different dielectric layers.

One of the most important parameters describing the oxide quality both for SCM analysis and gate dielectrics in MOS transistors is the amount of fixed oxide charges and interface trapped charges. Figure 2 compares the dC/dV plots obtained by SCM measurements both for SiO_2 and ZrO_2. According to MOS theory textbooks the different parasitic charges found in real oxides influence the formation of depletion and inversion zones and therefore influence the shape of signal versus voltage plots. Large amounts of either positive or negative fixed oxide charges move the plots vertically from their spe-

cial flatband condition to negative or positive tip bias values, respectively, because the fixed charges have to be compensated. The shapes of the curves remain unchanged. The nearer the peaks are to zero voltage position, the higher is the oxide quality. As one can see, the peak's position is +0.18 V for ZrO_2 and –1 V for high temperature SiO_2 respectively, which demonstrates the excellent electrical properties of the zirconium oxide layer. On the other hand, a large amount of interface trapped charges does not alter the peak's voltage-axis position, but broadens the plot.

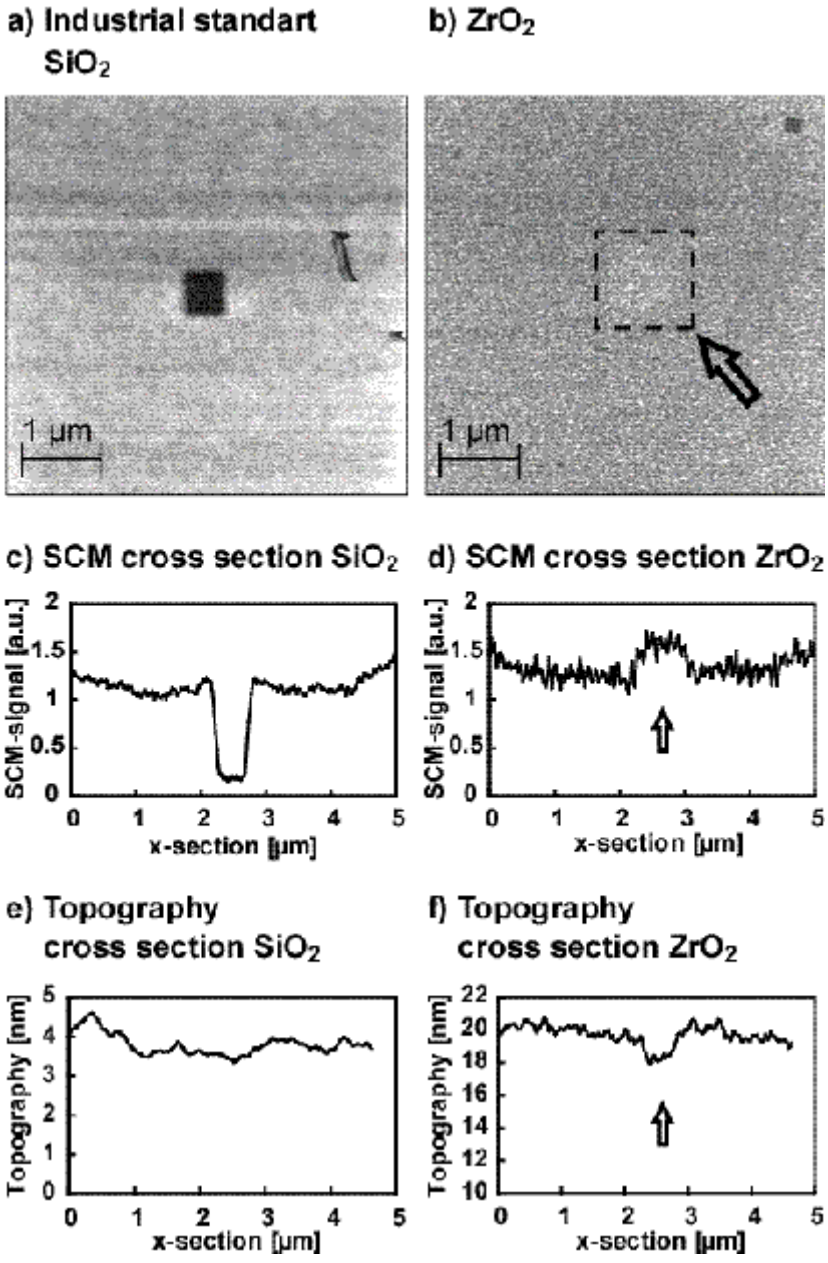

Fig. 3: Impact of dielectric layer degradation on SCM contrast. Degradation on a) SiO_2 leads to SCM signal lowering, on b) ZrO_2 the signal is higher in the stressed region. c) and d) show a signal cross section of the stressed areas for SiO_2 and ZrO_2, respectively. The topography of e) the SiO_2 layer remains unaltered, whereas f) the ZrO_2 layer was thinned due to scratching effects.

The broader peak of the SiO_2 sample is assumed to be due to anodic oxide growth and diffusion of contaminants which is more likely in thin (4 nm) SiO_2 than in the quite thick (20 nm) ZrO_2 layer. This shows the superior behavior of ZrO_2 in contrast to SiO_2. On the other hand, the reduction of oxide quality during SCM measurement can lead to contrast degradation, which is shown in Figs. 3 a) and b). Cross sections of both samples are shown in Figs. 3 c) and 3 d). In this experiment, a silicon oxide (Fig. 3 a)) and a zirconium oxide sample (Fig. 3 b)) were stressed by SCM scanning at a tip voltage of -3 V in a small area of about 500 x 500 nm. After 8 scans the resulting degradation was investigated by taking a 5 x 5 µm picture in capacitance mode with a tip bias adjusted to get the maximal signal. In the case of silicon oxide, the result is shown in Figs. 3 a) and 3 c), respectively. In the untreated region the normal signal for the investigated doping type was obtained whereas inside the stressed area the SCM signal was approximately zero. This indicates a severe degradation of the quality of the thin silicon oxide due to continuos SCM measurement. On the other hand, using zirconium oxide can prevent such problems concerning reproducibility as it is shown in Figs. 3 b) and 3 d), respectively. Only a slight signal increase occurs in the treated region, which is qualitatively different from the lowering in silicon oxide. Our interpretation concerning this fact is that material is scratched away by the tip which leads to a thinner dielectric. Subsequently the SCM signal is increased. Topographic investigations of the stressed region show an average lowering of 2 nm in Fig. 3 f).