Effect of Pulse Risetime on Trigger Homogeneity in Grounded Gate nMOSFET Electrostatic Discharge Protection Devices

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The inhomogeneities in the triggering of the parasitic bipolar transistor in grounded gate (gg) nMOS protection devices (PD) are known to reduce the ESD failure threshold. As well the risetime of the ESD pulse is known to have an influence on the triggering behavior of the CMOS ESD PD's. Short pulse risetime has been found to lead to a more homogeneous current flow along the device width and consequently to a higher ESD failure threshold. This has mainly been attributed to the contribution of the displacement current (depending on the device capacitance and the pulse risetime) to the total base trigger current. This effect is known as dU/dt-triggering. We have studied triggering behavior in submicron gg-nMOS ESD PD's by a backside laser interferometric method to investigate the current flow homogeneity in CMOS gg-nMOS ESD PD's of different technology as a function of pulse risetime.

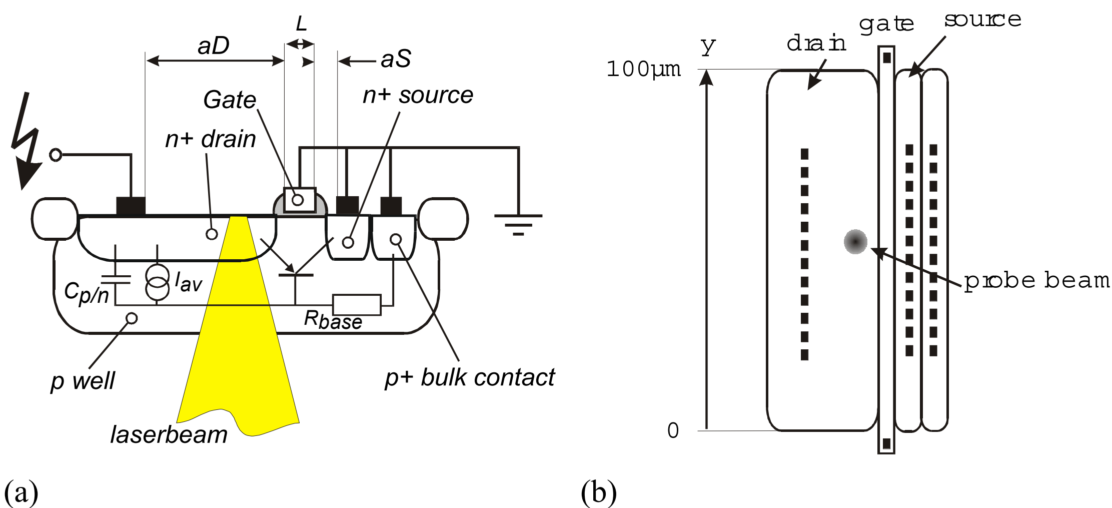
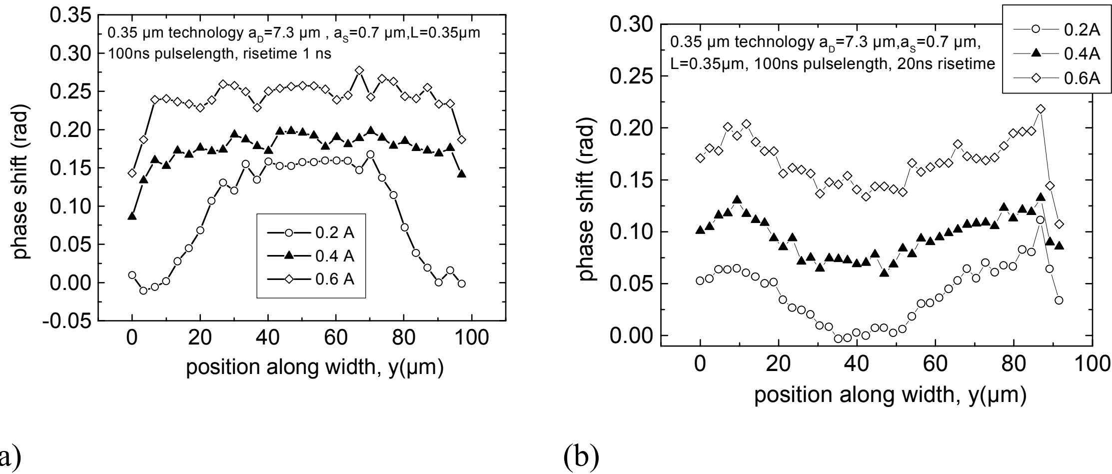


Fig. 1: (a) Cross-section of the gg-nMOS with equivalent circuit and the position of the probing laser beam indicated. The layout parameters a_S, a_D and L, as used in the paper are also indicated. (b) Top view of the gg-nMOS with the indication of the probing beam and the y-axis of the coordinate system used.

We have investigated single finger gg-nMOS ESD PD's of 0.35 and 0.18 µm technology with a variation of the drain contact to gate spacing a_D, source contact to gate spacing a_S, and gate length L. The source, gate, and the bulk contacts of the devices are connected to ground. Figure 1 shows the simplified cross section (a) and the layout (b) of the investigated devices. In Fig. 1 (a) the equivalent circuit of the gg-nMOS is also indicated.

To measure the current flow homogeneity we have used a scanning backside laser interferometric method. The temperature induced change in the Si refractive index (thermooptic effect) during current stress pulses of 100 ns and 150 ns length and different risetimes of 1 ns and 20 ns, respectively, is probed by measuring the phase shift of an infrared (IR) laser beam (wavelength $\lambda = 1.3$ µm). The phase shift of the probing laser beam is detected by a heterodyne interferometer setup and is in a first approximation a measure of the current density.

Figure 2 (a) shows a typical result for a measurement of the current flow homogeneity in a 0.35 µm technology gg-nMOS during ESD pulses of 1 ns risetime, for different stress currents. It can be seen that the MOSFET first triggers in the middle of the gate width at low stress currents, resulting in a current flow there. At higher stress currents the width of the triggered region increases and the current flow spreads towards the device corners. With a further increase of the stress current the device triggers over the whole width resulting in a homogenous current flow. Figure 2 (b) shows the current density distribution in the same device, when stressed with pulses of 20 ns risetime. For low stress currents the device first triggers at the gate corners.



(a) (b)

Fig. 2: Phase shift distribution along the device width at the end of a 100 ns long pulse with 1 ns (a) and 20 ns (b) risetime in the 0.35 µm gg-nMOS device for three different current pulse amplitudes.

With increasing stress current the current flow spreads to the middle of the device, leading to a homogenization of the current flow. However, the phase shift (so the current density) still exhibits two maxima at the two device corners, even at a stress current of 0.6 A. For the 0.18 µm technology devices, the current distribution does not show any qualitative difference between the stress with 1 ns and 20 ns risetime, and it is similar to that shown in Fig. 2 (a).

The difference in the triggering behavior for shorter and longer pulse risetime in the 0.35 µm technology devices indicates that the displacement current $I_{dU/dt}$ ($=C_{p/n}.dU/dt$) ($C_{p/n}$ is the substrate/drain capacitance, see equivalent circuit in Fig. 1 (a)) plays a crucial role in the device triggering. At 20 ns risetime, $I_{dU/dt}$ contribution to the substrate current I_{SUB} is negligible compared to that from the avalanche generation I_{AV} ($I_{SUB} = I_{dU/dt} + I_{AV}$). I_{AV} is dominant at the structure corners, due to a higher electrical field caused by the spherical shape of the drain diffusion at the corners. Therefore the device

triggers preferentially at the corners, independently on the stress current. At 1 ns risetime, the $I_{dU/dt}$ contribution is supposed to be comparable to I_{AV}. We have recently suggested that the triggering of the devices in the middle is due to a combined effect of the conductivity modulation in the drain/base region and a lower base resistance in the device middle. Our present results therefore imply that in order to "activate" the conductivity modulation in the 0.35 µm devices, a certain current density level has to exist in the device at the first moment of the triggering. This is reached by high value of $I_{dU/dt}$. The reason why the triggering in the middle (so also the conductivity modulation) in the 0.18 µm devices occurs also under long pulse risetime stress ($I_{dU/dt}$ is expected to be negligible here) is not yet understood. The effect of risetime on trigger homogeneity is therefore supposed to be technology dependent, at least for low stress currents.