Backside Interferometric Investigations of a DMOS Clamp Under ESD Stress

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Power DMOS transistors are building blocks of output drivers and switches in automotive applications. Their protection against electrostatic discharge (ESD) events can be obtained by self-protection or by appropriate gate-biasing active clamping. Such a clamp represents a circuit which may exhibit a complex behavior during an ESD event. The monitoring of a discharge paths in such circuit is important for understanding of the circuit behavior. Scanning backside interferometry is a useful tool for investigation of internal device behavior in semiconductor devices. In this work we have optically investigated thermal and free-carrier signals related to a discharge path in the active gate-biasing clamp circuit.

The gate-biasing active clamp circuit consist of a LDMOS transistor connected in series with a diode D added to block negative polarity stress; another diode that is in a parallel branch to the previous one to clamp the negative polarity stress; and the gate-biasing sub-circuit. Additionally, monitoring devices are used to monitor internal device voltages under the ESD event. Gate-biasing active clamp circuits with three different LDMOS areas (50%, 100% and 400% of a reference size) were investigated. The circuits were stressed by positive 100 ns and 300 ns long current pulses (up to 3.5 A) using a transmission line pulser (TLP). The optical mapping is performed using the backside laser scanning technique. A focused infrared laser beam (λ = 1.3 μm) scans the device, and the temperature induced (positive sign) and free-carrier induced (negative sign) contributions to the phase signal are interferometrically detected. For a dominant thermal contribution, the phase shift represents directly the 2D energy density in the device.

The differential resistance R_{diff} obtained from the pulsed IV measurements of the circuit is nearly stress current independent below the device failure threshold. $1/R_{diff}$ scales nearly linearly with the DMOS area, indicating that the current flow in the LDMOS device under ESD stress is homogeneous. This is confirmed by the thermal mapping across the fingers of the LDMOS (Fig. 1). It can be concluded that the gate-bias subcircuit effectively opens the channel of the LDMOS and supports the homogeneous current flow in the device.

During the positive ESD stress the diode D connected in series with the LDMOS transistor is forward biased. The optical mapping of the diode area exhibits a large negative signal during the stress pulse (Fig. 2), indicating a large free carrier injection. A linearly increasing thermal phase shift component is superimposed on the free-carrier signal. After the pulse end it becomes positive and reaches its maximum 400 ns after the end of the stress pulse. The effect of this delayed maximum cannot be explained by a lateral heat transfer from some different hot area of a circuit, because the maximum heat dissipating region is in the middle of the diode area. The closer analysis of the data suggests that the phase dynamics after the pulse is caused by an existence of a tail in the free-carrier evolution. The decay in the free-carrier signal is determined by the carrier recombination dynamics inside the diode region.

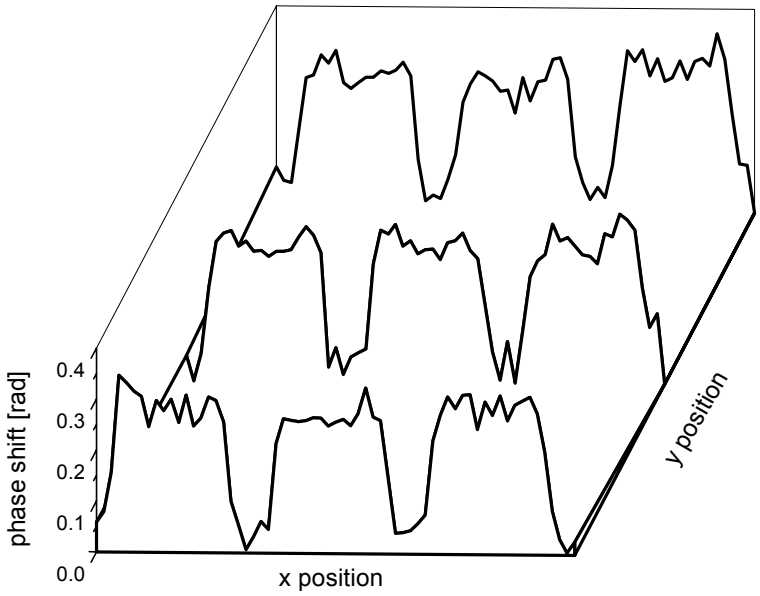

Fig. 1: The phase shift distribution in the 100% LDMOS at the end of the stress TLP pulse of 1.4A @ 300ns. Three fingers of the LDMOS are easy to distinguish. As the phase shift reaches the same values in all fingers in all scan lines, it can be concluded that the heat distribution in the LDMOS area is homogeneous.

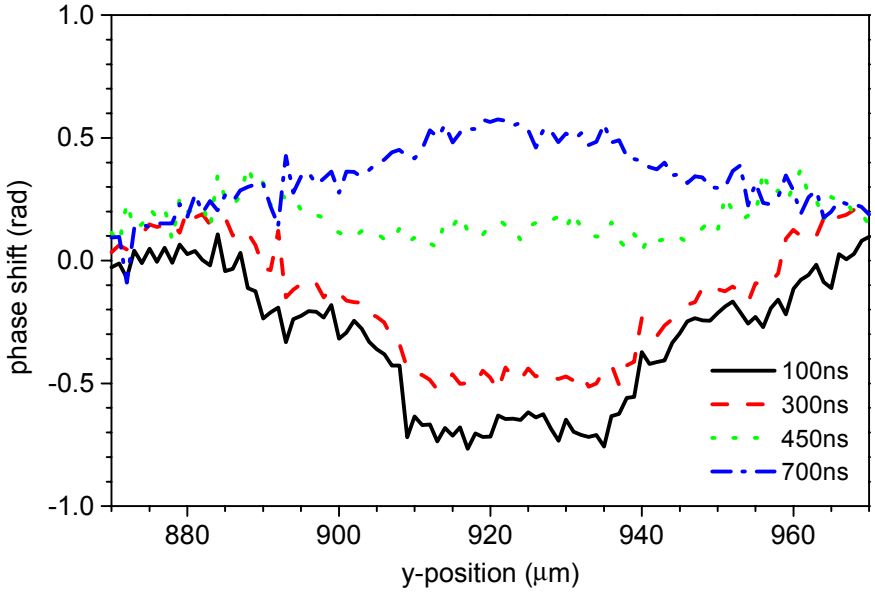

Fig. 2: The phase shift distribution in the diode D at the end of the stress TLP pulse of 1.4A @ 300ns. The time is a parameter (the stress starts at time 0 ns).

No other discharge paths were found in the gate-biasing active clamp circuit. Finally it was found that the circuit fails in the monitor sub-circuit.