Laser Interferometric Mapping of Smart Power ESD Protection Devices with Different Blocking Capabilities

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Protection against electrostatic discharge (ESD) in smart power technology devices has to take into account multiple bias source requirements. Consequently devices with different blocking capability, breakdown, and snapback voltages must be produced by simple layout variations. To optimize the design, physical failure analysis methods are usually used to get information on position of dominant hot spots causing the damage. The interferometric thermal and free carrier mapping techniques have a good potential to extract such information. In this contribution we investigate by this method the position of hot spots in two types of smart power ESD protection devices which block in one or in both polarities.

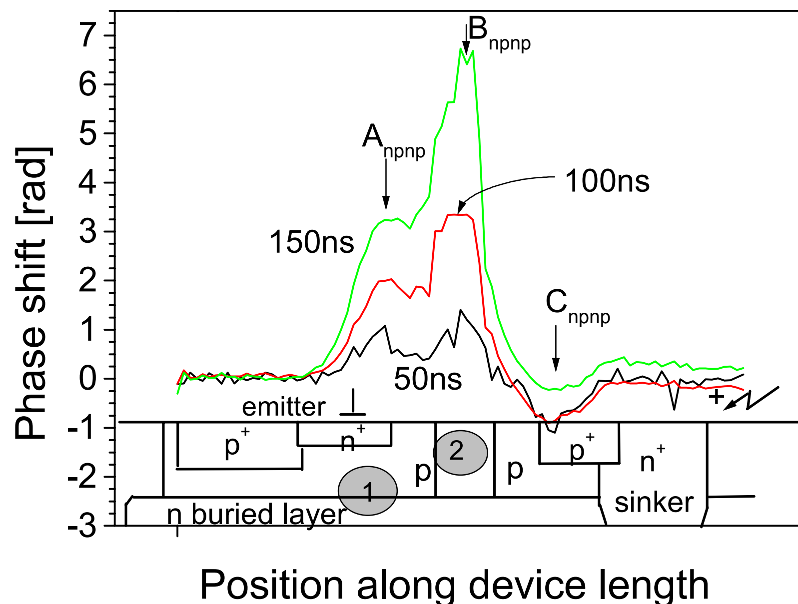

Fig. 1: Phase shift distributions along the length of the npnp structure at stress conditions 3.8 A, 150 ns and anti-serial device.

The thermal energy and free carrier distribution is studied using the measurements of temperature- and free carrier-induced optical phase shift. The phase shift distribution measurements in both devices exhibits two maxima (see Figs.1 and 2). The A peaks are related with heat source in the vertical npn that is marked as gray regions 1 in Fig.1 and 1, 3 in Fig. 2. The B peaks are due to a lateral current flow in the lateral pnp transistor

(marked as a gray region 2 in Figs.1 and 2). The negative phase shift C is attributed to plasma-optical effect due to carrier injection.

A failure analysis has been performed on the devices. An ESD damage in the npnp structure could not be observed for stress currents lower than 10 A (150 ns duration). The threshold for the defect creation in the anti-serial devices is in the 5 – 8 A range (for 150 ns pulses), depending on the stress polarity. This damage was established as a degradation of the contact metallization in the emitter region.

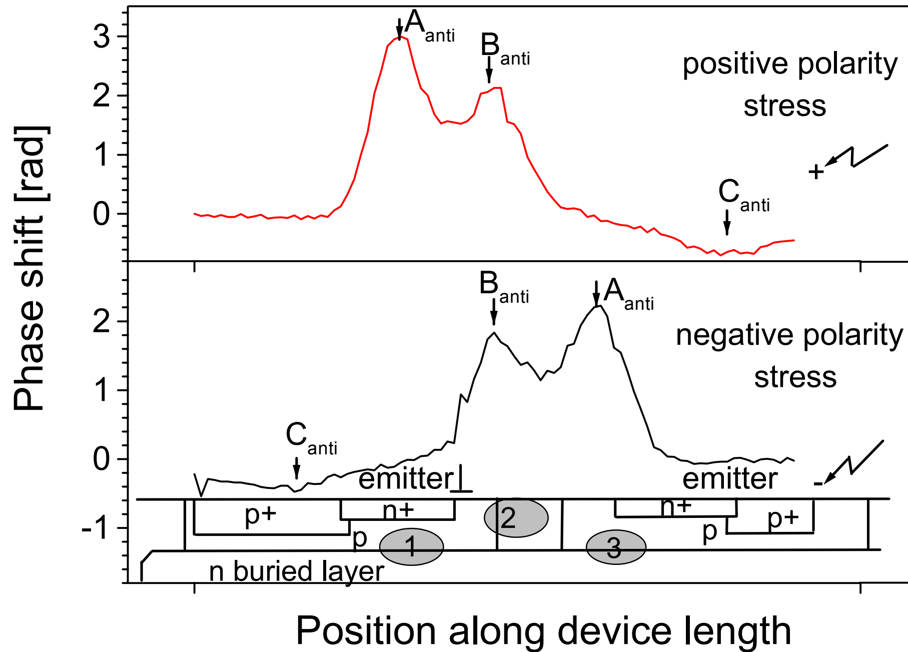

Fig. 2: Phase shift distributions along the length of the npnp structure at stress ±2 A, 150 ns.

The different ESD ruggedness of the two structures is attributed to different positions of the dominant hot spot. In the npnp device, the dominant hot spot is located under the LOCOS insulation. SiO_2 oxide or the Si/SiO_2 interface is known not to be very sensitive to thermal stress. In the anti-serial device, the dominant hot spot is located under the emitter, close to the contact metallization which is vulnerable to thermal damage.