An Optical Setup for Investigation of Internal Device Behavior Under CDM-Like ESD Stress

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Due to the increasing degree of automation in the integrated circuit production, electrostatic discharge (ESD) protection against the charge device model (CDM) stress becomes more and more important compared to the standard human body (HBM) stress. Backside laser interferometry is a unique and powerful tool to investigate internal device behavior under ESD stress. In the previous studies using the heterodyne setup, the duration of the high current stress was 100 ns or more. The time resolution of the heterodyne setup (about 3 ns) cannot be improved due to complicated optics. Therefore for investigation of CDM-like events occurring in the 1 – 10 ns scale a new Michelson-like interferometer was built.

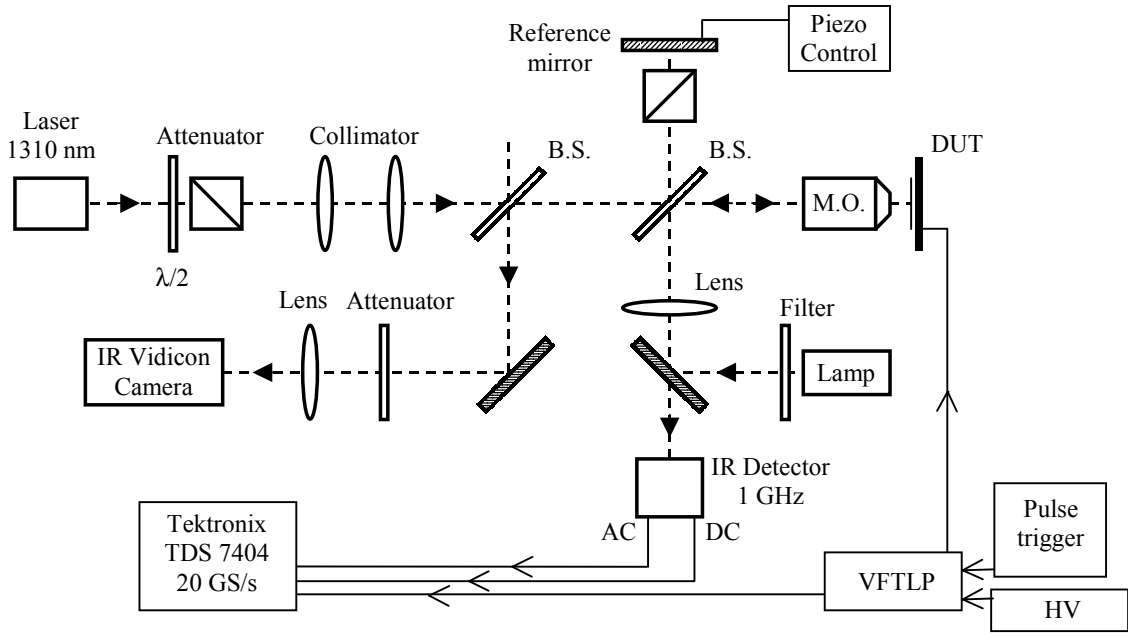

Fig. 1: Simplified scheme of the setup.

The scheme of the optical setup is depicted in Fig. 1. A DFB laser diode with the wavelength $\lambda = 1.3$ μm is used as a source of coherent light. The beam is collimated and then split by a beamsplitter into the probe and reference beams. The probe beam is focused by a microscope objective (M.O.) to the backside of the investigated device (DUT). The laser spot size of approx. 2 μm defines the space resolution. The beam is then reflected from the device surface, passes the same way back and reflects from the beamsplitter to the detector. The reference beam is reflected from a mirror mounted on a piezo mirror-

shifter. The intensity of the reference and probe beams can be controlled independently. Both beams are focused to the detector to get an interference signal. The signal from the detector (400 ps risetime) is recorded by a high sample rate oscilloscope (Tektronix TDS 7404). For the positioning of the beam on the device an IR vidicon camera is used. The stress was performed by a very fast transmission line pulser (VF-TLP) providing a CDM-like stress. The current and voltage on the device were calculated from the calibrated incident and reflected stress voltage waveform. The measurements are performed in an RF-shielded environment to reduce the pick-up of radiated noise from the fast-rising high-current pulses. The optical response was carefully time-aligned with the electrical stress pulse, taking into account all electrical and optical delays.

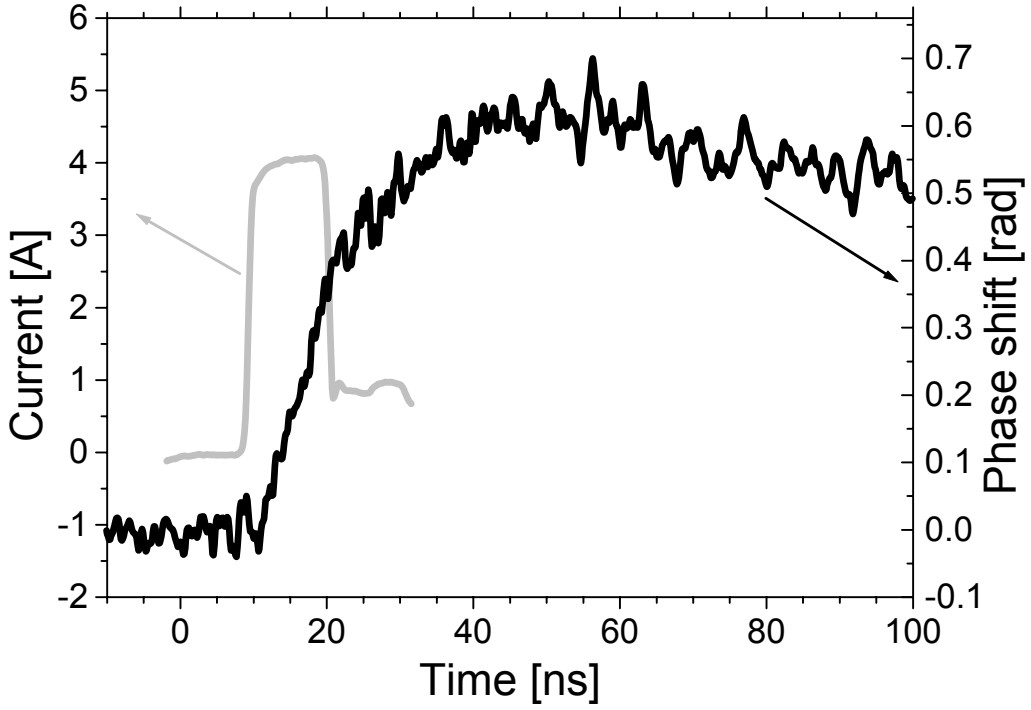

Fig. 2: Phase shift at a single point in the CMOS structure and corresponding current pulse. The curves are 20-times averaged.

The studied CMOS ESD protection devices are grounded gate (gg) NFETs of 0.35 µm technology with different gate to drain contact and gate to source contact spacings. Current pulses of 10 ns length and 4 A amplitude were applied, see Fig. 2. The current through the device causes a heating in the drain region. The optical signal shows a fast rise with a delayed maximum after the end of the pulse. The dynamics of the signal during the stress pulse reflects well the thermal energy dynamics. The delay is caused by the heat transfer effect as the probe laser beam is laterally shifted some 2 µm away from the position of the maximal heat dissipation. The setup is sufficiently sensitive to record phase shift related to a single stress event. This is important for the investigation of possible trigger instabilities. The method is useful for the verification of the results of device and circuit simulation models in the CDM time domain.