Investigation of the Parasitic FET in Sub-100 nm Trench-DRAM

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Miniaturization of DRAM trench cells quickly progresses towards design rules below 100 nm. This development faces the problem of an increased node resistance due to the continuous shrinkage of the connecting path to the inner trench electrode.

As shown in Fig. 1 (a), a heavily n-doped region, the so-called buried strap, connects the trench-electrode with the drain region of the switching transistor. To separate this region from the n-doped well forming the counter electrode of the trench capacitor, a p-doped well has to be inserted. As shown in Fig. 1 (b), this n-p-n sequence can be considered as the body of an n-channel FET. In this transistor structure the silicon-dioxide collar acts as a gate dielectric and the inner trench performs like a gate electrode. This FET facilitates a possible leakage path, which is capable of discharging the trench capacitor, leading to a malfunction of the DRAM cell. Thus, an accurate knowledge of the electrical behavior of this FET is a necessary precondition for a proper design of the trench, and is therefore a primary concern in any trench-cell based DRAM technology. To optimize the performance of the trench cell, a characterization of this parasitic FET is essential. Due to the fact, that its contacts are not directly accessible, standard electrical methods fail to characterize the parasitic FET. This work proposes a new approach allowing extracting the most important parameters of this embedded parasitic device.

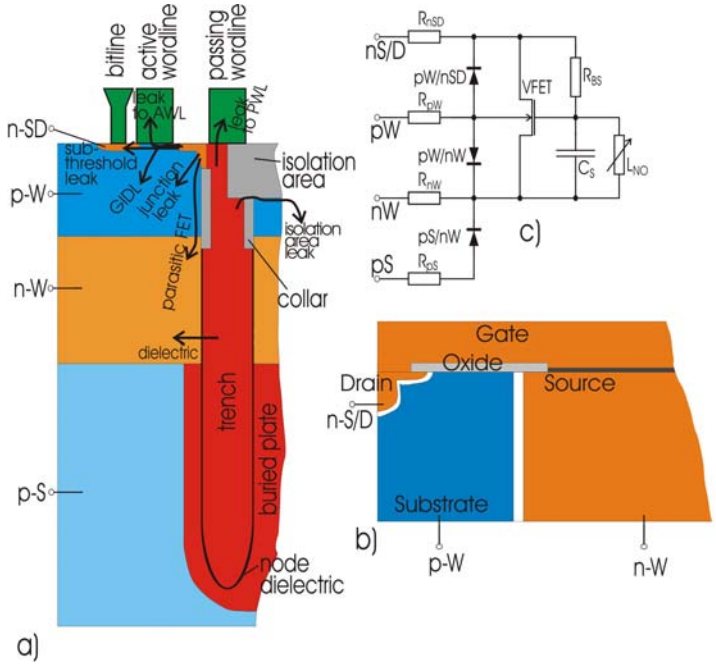

Fig. 1: n-SD…n-doped area of bypassed source and drain of the switching transistor; p-W…p-doped well; n-W…buried n-doped well; p-S…p-doped substrate
a) Schematic DRAM-trench cell. b) Parasitic FET. c) Circuit diagram of test structure.

As shown in Fig. 1 (a), several leakage paths may modify the charge of the trench capacitor. The key element of our investigation is the parasitic FET as depicted in Fig. 1 (b). Thus, for the electrical characterization a DRAM test-structure is used where the buried strap is directly accessible via a shorted switching transistor. Thereby, any subthreshold contribution of the switching transistor is excluded.

Setting the voltages for n-SD, p-W, and p-S equally to 0 V while ramping the voltage of n-W to positive values allows to measure the current from n-SD to n-W which is a branch of the leakage path through the oxidized silicon nitride (NO). By usage of the previously described test structure the leakage path through the NO of the capacitor can only be assessed in the polarity where the voltage of the n-W is higher than the voltage of the n-SD. If the inverse polarity is biased, the parasitic FET would turn on and the current through the FET would join the current through the NO. As the gate-dielectric NO consists of oxidized silicon nitride, the branches of current describing the leakage due to electrode polarity will not be symmetric. The measurable leakage current allows approximating the branch with inverse polarity and allows identifying the current through the NO.

Considering all separated leakage paths of the reverse-biased pn junction and taking into account the different magnitudes of the approximated NO leakage the current path through the parasitic FET can be obtained.

To measure the drain current of the parasitic FET in subthreshold or even in inversion mode the potentials applied to the bypassed gate and drain (n-SD) are ramped to positive voltages exceeding the assumed threshold voltage, the source (n-W) is held at 0 V while the bulk of the parasitic FET (p-W) is held at constant voltages equal or less 0 V (see Fig. 1c).

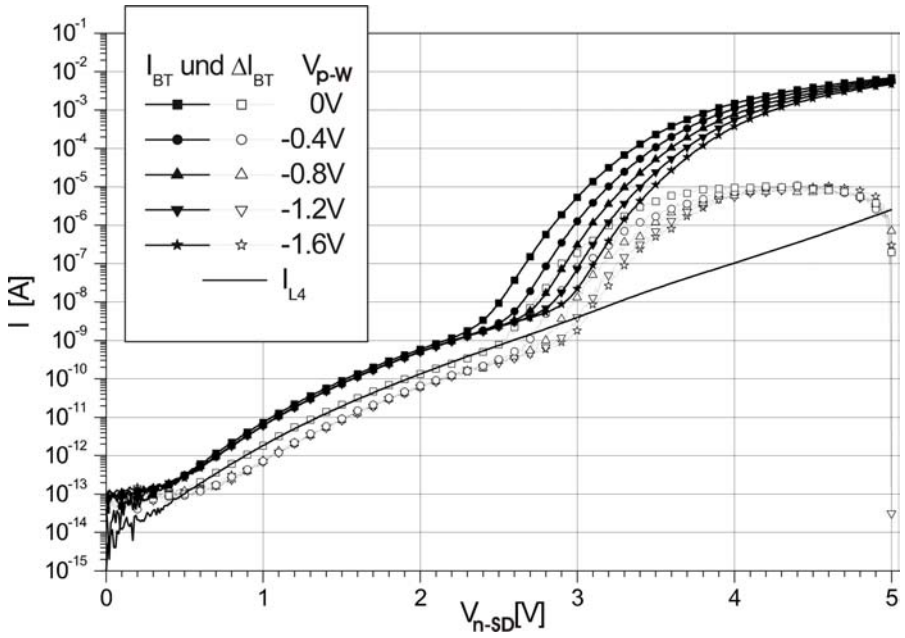

Fig. 2: I_{BT} for five different source-substrate bias-voltages. Empty symbols show the standard deviation of each measured value.

Figure 2 shows I_{BT} for five different source-substrate bias-voltages. The splitting-up shows the existence of a FET drain current due to the variation of the substrate reverse bias. Additionally, the measured current through the NO is shown. The curves below voltages of 2 V display a similar behavior about half an order of magnitude higher than the measured current through the NO and do not split up with different source-

substrate reverse bias. Consequently, the current below 2 V can be identified as the leakage path through the NO under the condition that the voltage of n-SD is higher than the voltage of n-W. Any potential current due to the parasitic FET in this regime is smaller and may be neglected. At a voltage of 2.3 V the transistor current exceeds the current through the NO. As a consequence the current curves coincide again at the end of the scala as the transistor moves towards saturation.

The subthreshold current displays a roughly exponential behavior in dependence on the gate voltage for the long channel approximation. The dimensions of the parasitic FET fulfill the conditions for a long channel FET following an empirical relationship found by Brews et al. [1]. As the substhreshold current of a FET is roughly independent of the source-to-drain voltage it may be extrapolated to the region where the current through the NO exceeds the FET current. This approximation allows estimating the leakage current of the parasitic FET and facilitates optimizing the operational regime in a trench DRAM-product (see Fig. 3).

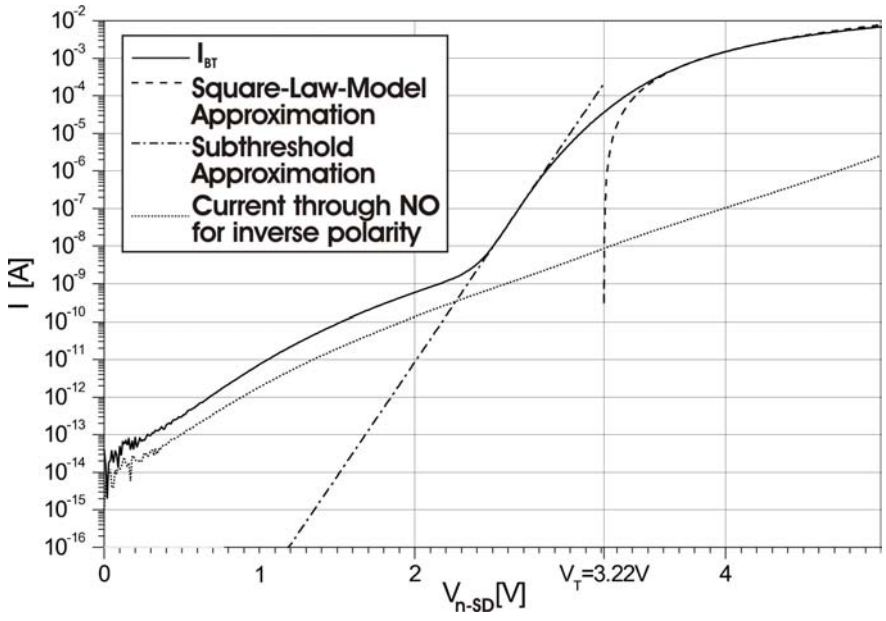

Fig. 3: Current through the parasitic FET.

As drain and gate are linked together the parasitic FET is always operating in saturation. Using the square-law model in saturation the measured data can be also fitted for the FET in inversion mode (see Fig. 3).

While the presented measurement methods were developed using a standard trench-DRAM this approach was already applied on new concepts of trench-DRAM with buried collar [2] at Infineon Technologies Dresden.

References

[1] J. R. Brews, W. Fichtner, E. H. Nicollian, S. M. Sze: *Generalized Guide for MOSFET Miniaturization,* IEEE Elect. Dev. Letters, vol. **EDL-1**, no. 1, 2 (1980).

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