Hot Spot Dynamics in Vertical DMOS under ESD Stress

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Double-diffused MOS (DMOS) transistors are widely used as high power switches in automotive applications. Due to harsh environment predominating in cars, these devices are exposed to stresses like electrostatic discharge (ESD). A high current, short duration ESD pulse drives the transistor into avalanche breakdown. Under such condition, the device may fail due to triggering of a parasitic bipolar NPN between source, body and drain.

This work studies experimentally the complex dynamics of grounded gate quasi-vertical DMOS transistors after non-destructive snap-back and explains it using electro-thermal simulations [1], [2]. In particular, the positive action of current delocalization on ESD capability is addressed. Formation, spreading, and movement of the hot spots are investigated under square current pulses of maximal 180 ns duration by means of the 2D Transient Interferometric Mapping (TIM) method. In this technique, a thermally induced phase shift is detected, the later being proportional to 2D thermal energy density in silicon. The thermal image can be obtained during a single stress pulse. The time and space resolutions are 5 ns and 3 µm, respectively. The current pulses are produced by a high power electronic switch. The stress currents were chosen above the snap-back current. The devices under test belong to a 1.2 µm, 90 V Smart Power Technology.

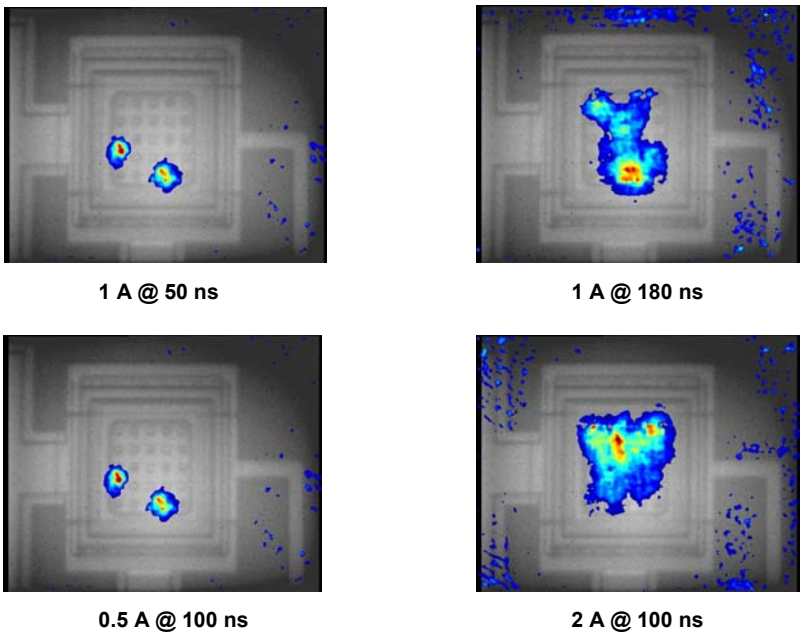
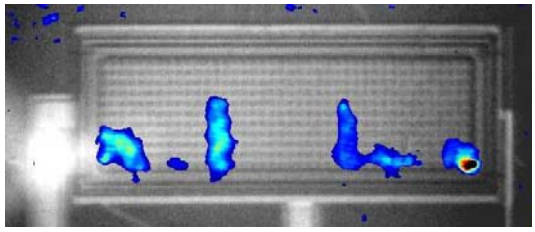


Fig. 1: Examples of extracted TIM pictures of studied small VDMOS device. The stress current level and time instant, when the picture was taken, are indicated below each picture (after [2]).

Figure 1 shows examples of the phase shift distributions in the small device at different time instances and under different stress currents. The phase shift profiles are aligned with the backside infrared images. The heat dissipation starts at the termination and spread with time into the area of the device. This indicates the existence of moving current filaments in the device during this operation condition. With increasing current, the heated area enlarges.

Figure 2 shows the phase shift distribution over a larger device stressed by the current pulse of 3.5 A @ 180 ns. Several hot spots can be observed along the termination of the device. It was found that several filaments could coexist in the device simultaneously.



3.5 A @ 180 ns

Fig. 2: Examples of extracted TIM pictures of studied large VDMOS device. The stress current level and time instant, when the picture was taken, are indicated below the picture (after [2]).

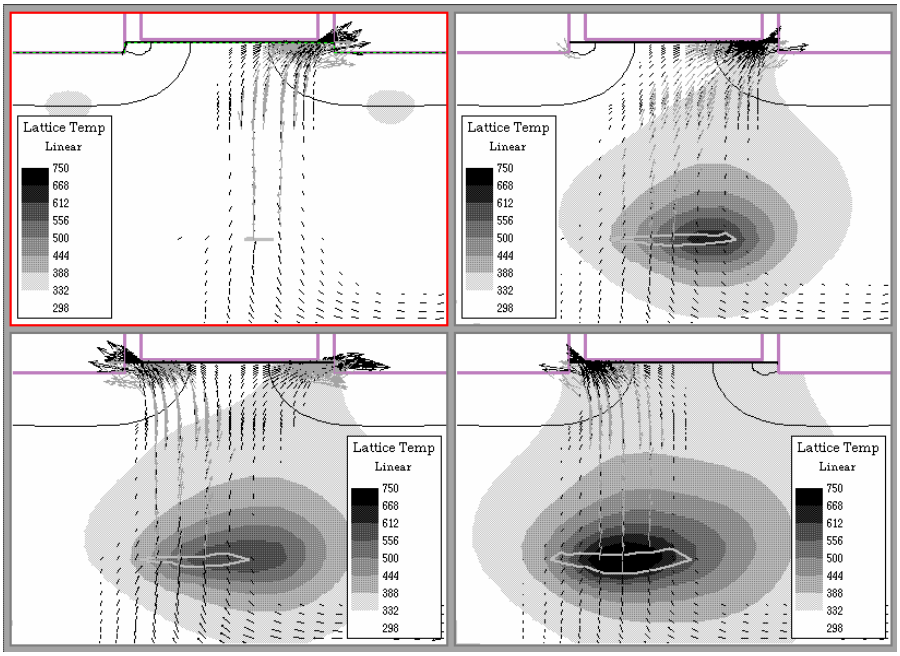


Fig. 3: Electro-thermal simulation of two neighbor VDMOS cells with drain contact on the right side of buried layer, stressed at a similar current density as in the experiments: lattice temperature, hole current density (gray arrows), electron current density (black arrows) and isoline for electric field (thick gray line) after: a) 15 ns: right cell active, b) 35 ns: avalanche region reaches left side, c) 45 ns: both cells triggered and d) 65 ns: left side active (after [1]).

Electro-thermal simulations were performed to help interpreting these results. Figure 3 shows the simulated time evolution of temperature and current densities in two neighbor in-cells for a stress current density of the same order as in the experiments. The right cell triggers first. This is accompanied by a push-out of the maximal field down to the n-epi/n^+-buried layer junction. A hot spot forms at this place and extends with time. After ca. 35 ns, the avalanching region reaches the left part of the structure. The generated holes first keep flowing to the right cell. At 45 ns however, avalanche multiplication beneath the left cell gets high enough to trigger it. After 65 ns, the left cell has taken over the current. In order to trigger a further cell, the hot spot has first to walk around its last triggered cell. At higher simulated currents, it is observed that the initial cell stays active. In such case one expects the activated area to increase in time as the region of maximal electric field moves through the device. A lower avalanche threshold at this location explains hot spot persistence observed at the termination in the TIM shots.

In conclusion, the mechanism proposed to explain hot spot dynamics in the investigated quasi-vertical DMOS consists in a sequence of hot spots walking around a triggered cell followed by a transfer to a neighbor cell. Under sufficiently high stress current this process leads to a homogenization of the area active in snap-back and allows the studied DMOS to reach an excellent ESD capability.

References

[1] M. Denison et al: “Hot spot dynamics in quasi vertical DMOS under ESD stress”, Proc. of ISPSD 2003, pp. 80-83

[2] M. Blaho et al: “Hot spot mapping in the DMOS devices for automotive applications”, Informationstagung Mikroelektonik 2003, pp. 329-334