# Thermal Mapping of the SMARTIS SOI Devices under the vf-TLP and TLP Stress Conditions

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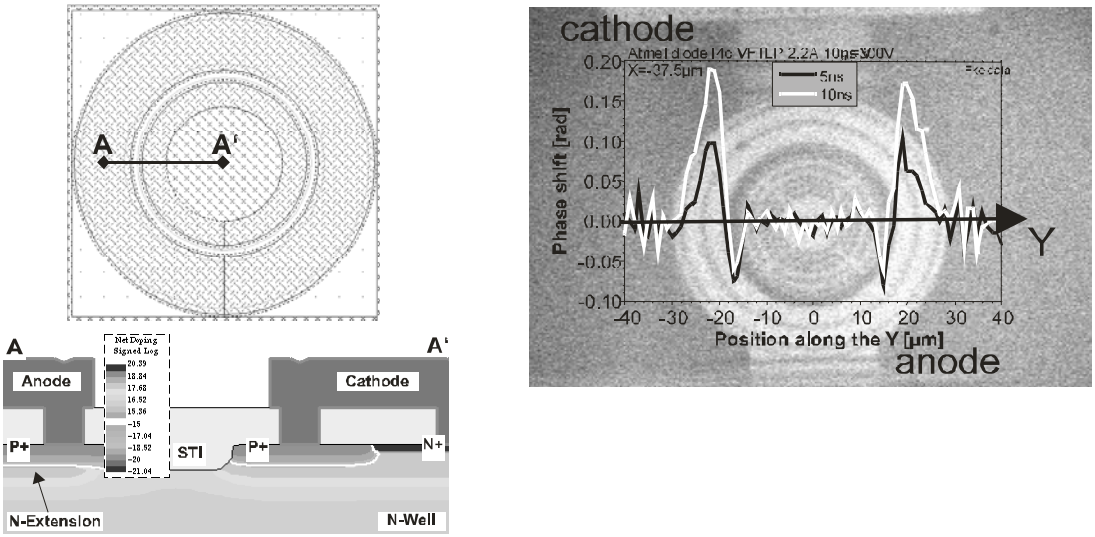
The importance of the microelectronics products in daily needs is steadily growing. The questions of the reliability and ESD robustness of microelectronic chips and circuits gain higher level of significance from year to year. Modern ASICs monitor and control security relevant operations in automotive applications. Electronics become responsible for the health of the passengers in case of an unforeseen event like an accident. Safety critical applications set a new demand for improvement of the ESD hardness of the protection devices. An obvious increase in the integration density and at the same time an improvement of ESD robustness is possible to obtain by using a new kind of technology based on SMARTIS SOI. The approved concepts of the BCD bulk technology cannot be transferred to the SMARTIS SOI due to technological peculiarities (absence of the buried conductive layer). Therefore the development of the effective ESD protection concept for the SOI devices has to start from the beginning.

The prototypes of bipolar protection elements (see Fig. 1 (a)) of SMARTIS SOI technology were investigated under the TLP (100ns) and CDM-like vf-TLP (10ns) stresses. The devices were processed on different kinds of SOI wafers with high variations of the active layer thickness. Pulsed IV characteristics of the devices exhibited variations in the maximum ESD current. These variations could be caused by the inhomogeneous triggering of the devices or by the influence of the active layer thickness on the failure currents.

Using backside thermal interferometric mapping the power dissipation inside of the devices was monitored during the TLP and vf-TLP stresses. Scans along two perpendicular axes (data along Y axis is shown in Fig. 1 (b), the results along the X-axis are similar to the Y-scan) show homogeneous power dissipation in the device. This result helps to understand that the variations in the maximum ESD current of devices are influenced by the active layer thickness only.

With help of the electro-thermal model of the device the influence of the active layer thickness variations on the failure current was simulated. The optical mapping and the simulated temperature profile are in a good qualitative agreement (see Fig. 2). This indicates the correctness of the electro-thermal model of the device that was chosen for simulations.

The results of the investigations could be used in the development of suitable ESD protection for smart power SOI technologies.




a) b)

Fig.1: Results of the transient interferometric mapping on SMARTIS SOI bipolar device under the vf-TLP stress 2.2 A 10 ns. The device layout is shown in (a). The thermally induced phase distribution along Y-axis (b) is shown for 5 ns and 10 ns time instants. The background image in (b) is the backside infrared picture of the device; after [1].

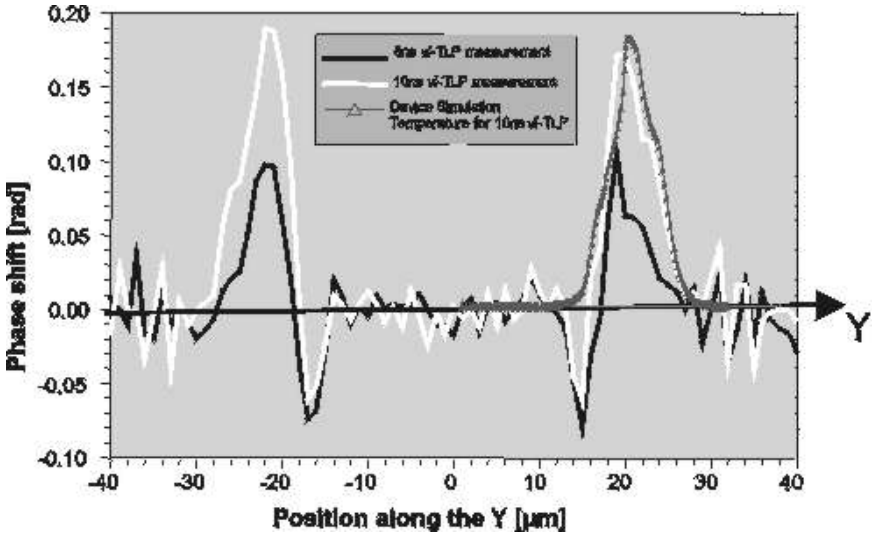



Fig. 2: Comparison between optical mapping (white/black) and simulation (gray line with triangle marks at right half of the Y-axis); after [1].

## Reference

[1] M. Graf, S. Bychikhin, F. Dietz, V. Dudek, D. Pogany, E. Gornik, W. Soppa, H. Wolf 'Impact of Layer Thickness Variations of SOI-Wafer on ESD-Robustness' Proc. EOS/ESD'2003 Symposium, p.116, 2003.