Fabrication of Dry Etched Planar Photonic Crystals for THz Regime

S. Golka, W.Schrenk and G. Strasser
Institute of Solid State Electronics, TU Vienna, Austria

Photonic Crystals (PhCs) in III-V semiconductors will play an decisive role in future telecom opticelectronic integrated circuits (OICs). Undoubtedly this is valid for related fields such as THz emitters and novel compound semiconductors as well. Besides the light guiding aspect many new phenomena which are very desirable for THz applications, such as enhancement of optical nonlinearities and efficient vertical coupling to continuum, can be observed in deep etched InGaAsP PhCs. In such devices the basic idea is to exploit the large degree of freedom one has with such PhCs in tailoring symmetries and shapes of cavity modes or high reflectivity mirrors but at the same time leaving a contiguous surface that allows for easy subsequent processing. In most cases the optical mode confinement is achieved by the "substrate approach", e.g. planar light guiding by deep hole patterns and vertical guiding by a epitaxially grown high index layer as opposed to membranes or surface plasmon guiding. Heat and electric conduction to the substrate are provided for and multi-step fabrication is much easier than in membranes for example. Furthermore, the comparatively large minimum pattern size as required for THz allows for subsequent processing that is aligned to and/or in the same area of the PhC [1], such as top contacts. Etch depth [2] becomes the most critical parameter for these emitters, since epitaxial layers typically are several micron thick and holes need to penetrate the substrate much further than the guided light mode.

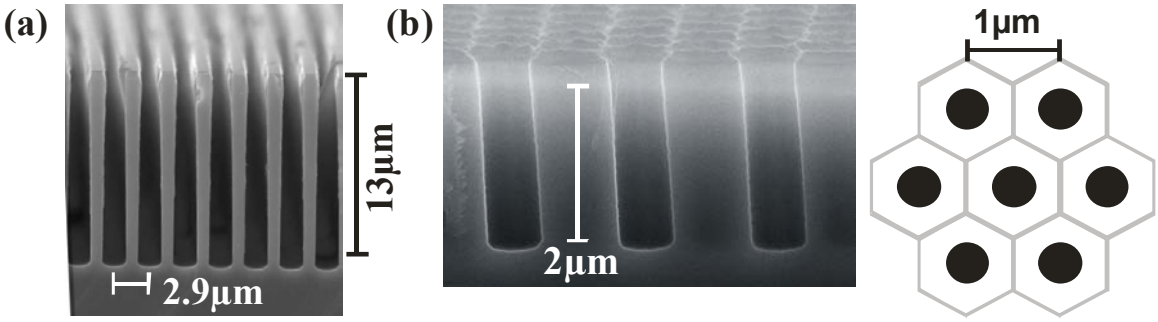

Fig. 1: (a) SEM picture of cleaved sample with $N_2/SiCl_4$ process with 1:1 molecular flow, duration 38 min, best sidewall protection obtained so far;
(b) same etch process applied on a two dimensional PhC with 1 µm pitch etched for only 13 min. Pattern was generated with 30 KV EBL in 400nm PMMA 950K resist. Roughness on the top is the remainder of the SiN_X mask after deep etching that could be easily removed by HF or SF_6 plasma. Etch duration was limited by stability of PMMA resist in SF_6.

Due to the importance of deep etching in a first step we solely focus on the process for GaAs. In order to achieve sufficient etch selectivity a hard mask with good adhesion such as SiN_X is needed. A two step process of first structuring the SiN_X from a resist with SF6 plasma and then, after resist removal, etching with $SiCl_4$ high density plasma

has proven very convenient. This also has the advantage of easy migration to novel lithography methods as stamp-imprinting or deep UV. In the case of standard UV lithography (Fig. 1 (a)) 500nm of AZ5214 resist will suffice to etch 500 nm of SiN_X. In the case of electron beam lithography (EBL, Fig. 1 (b)) a plasma-stable resist is needed.

In deep etching very high aspect ratio is needed in densely packed hole patterns, F=30%, so some mechanism must be present to inhibit underetch. With free standing walls, back-sputtering of etch products would serve as such mechanism, but in deep trenches/holes the ratio of floor to wall area is too small for efficient side wall coverage. In our inductively coupled plasma reactive ion etcher (ICP-RIE) we tried both an $Ar/SiCl_4$ and $N_2/SiCl_4$ gas mixture. Both mixtures showed fundamentally different behavior in the plasma (Fig. 2 (b)). For Ar [3] chemically sticky $GaCl_X$ might be expected for proper parameters that is sputtered off the floor by Ar but not off the walls. But decent results were obtained with N_2 only. We believe that the nitrogen in the plasma enhances saturation or deposition of some Si containing species on the hole sidewalls that is not volatile even at slightly elevated temperatures, which is not surprising thinking of $SiCl_4$ as a precursor in Silicon technology [4]. It therefore provides for sidewall protection even at very large etch depths (Fig. 1 (a)). This also is consistent with the dependence of etch rate on flow ratio (Fig. 2 (b)) in which the rate is slightly enhanced by Ar surface cleaning but degraded by too much N_2 induced deposition which is valid at least for the process window where we found each process to work at all for small patterns.

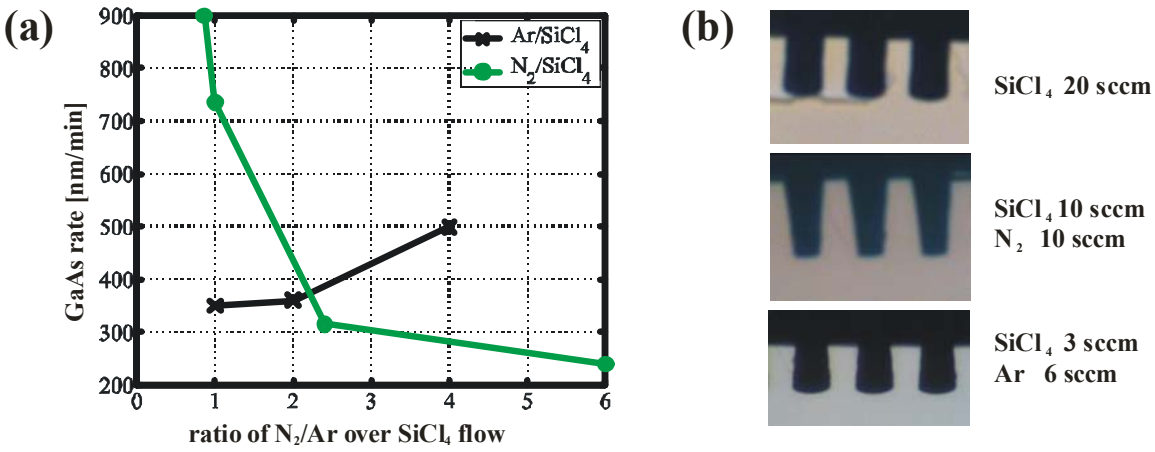

Fig. 2: (a) Typical trench profiles for different kinds of physical etching contribution in ICP processes;
(b) etch rate dependence on physical/chemical ratio at P = 3 mtorr, gas flows were 3 times lower in the case of Ar intentionally due to severe underetch, hence the lower vertical etch rate;

In conclusion, we have shown the main contribution of process parameters to $SiCl_4$ ICP- RIE where we distinguished between adding Ar or N_2. Etch depths of 13 µm were achieved for N_2 with a mask that could be easily fabricated in a 2 step procedure with one more SF_6 etch. The achieved trench depth will be sufficient for low scattering losses in high index guided structures. Furthermore we fabricated two dimensional PhCs with E-Beam lithography with the same process.

References

[1] R. Colombelli, M. Troccoli, K. Srinivasan, O. Painter, C. Gmachl, F. Capasso, D. M. Tennant, A.M. Sergent, D. L. Sivco, and A. Y. Cho, *Proc. ITQW 2003*, Evolene, Switzerland

[2] R. Ferrini, B. Lombardet, B. Wild, R. Houdr´e, and G.-H. Duan. Hole depth- and shape-induced radiation losses in two-dimensional photonic crystals, *Appl. Phys. Lett.* 82(7), 2003

[3] R. J. Shul, G. B. McClellan, R. D. Briggs, D. J. Rieger, S. J. Pearton, C. R. Abernathy, J. W. Lee, C. Constantine, and C. Barratt, *J. Vac. Sci. Technol.* 15(3), 1997

[4] I. Endler, A. Leonhardt, M. Schonherr, and E. Wolf, *J. of Materal Science* 26(3), 1991