Development of a Silicon Deep Reactive Ion Etching Process for the Fabrication of Large Area Silicon Phase Gratings

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We report on the development of a reactive ion etching (RIE) process using the new inductively coupled plasma reactive ion etcher Plasmalab 100, which was installed at the cleanroom area of the Microstructure Center recently. Periodic structures with aspect ratios up to 15 and periods from 12 μ m to 28 μ m were produced. The patterned areas in these samples were 22 x 22 mm².

Using the black silicon method (BSM) described in [1] we developed a process with etch rates of approximately 1 μ m/min and good profile control for aspect ratios up to 15. Photoresist Shipley 5214 was chosen as mask material with a layer thickness of 1 – 1.5 μ m. To go beyond aspect ratios of 15, SiO₂ would have to be used, since thicker layers of photoresist tend to crack under cryogenic conditions (–110°C in this process). On the other hand, layers thinner than 1 μ m showed premature erosion in this process [2].

The design of our samples made it necessary to use carrier wafers. It turned out that GaAs wafers influenced the etching process, so Si wafers were used instead. Sufficient thermal contact between sample and carrier was ensured by bonding with photoresist.

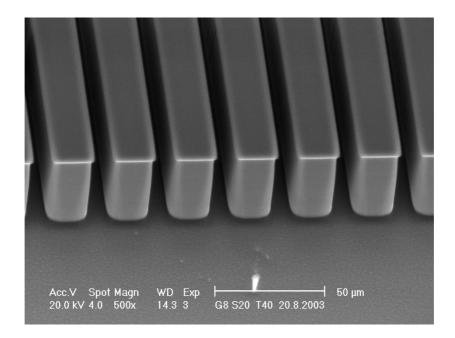


Fig. 1: trench 8µm, ridge 20µm, depth 40µm

Figure 1 shows one of the regular structures with a trench width of 8 μ m and a period of 28 μ m. Note the excellent trench profile. Figure 2 shows one of the high aspect ratio samples. The smallest feature in this sample is 4 μ m, giving an aspect ratio of 10.

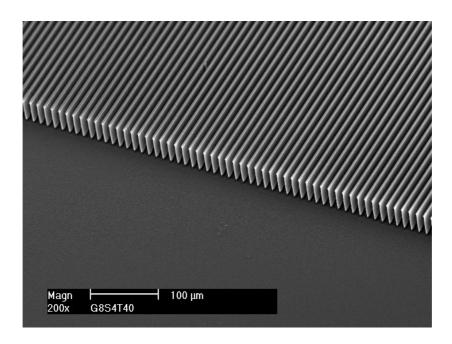


Fig. 2: trench 8µm, ridge 4µm, depth 40µm

These samples will provide unique test procedures in neutron scattering. For details, see [3].

References

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