GMe
Gesellschaft für Mikroelektronik

The Society for Microelectronics

Annual Report

1995

Vienna, April 1996

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c/o Technische Universität Wien
Institut für Allgemeine Elektrotechnik und Elektronik
Gußhausstraße 27-29/359, A-1040 Wien

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The Society for Microelectronics (GMe — Gesellschaft für Mikroelektronik)

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1. Goals of the Society for Microelectronics

The Society for Microelectronics (GMe) was founded in 1985 with the aim to "*support microelectronics technology and its applications in an interdisciplinary way*". The GMe defines its tasks as follows:

- Support of university-based high-technology research in the areas of microelectronics, semiconductor technology, sensors, and opto-electronics;
- Construction and operation of research facilities;
- Support and consulting for industry, in particular, for small and medium enterprises, within the area of microelectronics.

The central task of the GMe is the creation and maintenance of *infra-structure* for an internationally competitive microelectronics technology. The funds provided by the GMe support a variety of projects and activities in the fields of semiconductor technology, sensors, and opto-electronics. One of the criteria for the support of an activity by the GMe is a project area that needs seed money for infra-structure to obtain funding by other sources.

2. Activities of the Society

Currently, the GMe recognizes three focal points for its activities. In general, projects that expect support by the GMe must pertain to at least one of these areas. Other microelectronics-related projects may receive occasional support by the GMe, for example, for infra-structure that is a prerequisite to a funding by other sources, or in the case of an emergency. The current focal points of the GMe activities are:

- Construction and operation of university-based laboratories for microelectronics technology;
- Design of application specific integrated circuits (ASICs) — UNICHIP;
- Microsensors.

2.1 Microelectronics Technology — Cleanrooms Vienna and Linz

The currently most important task of the GMe is closely linked to the construction and the operation of technological installations, in particular, of the cleanroom laboratories in Vienna and Linz. In 1992, the Austrian Federal Ministry of Science and Research invited the GMe to act as a coordinator for the construction of the Microstructure Center (MISZ — Mikrostrukturzentrum) in Vienna. The MISZ Vienna finished construction by the end of 1993 and went into operation in June 1994. The GMe now provides with its funds a significant part of the operation costs for the cleanroom laboratories in Vienna and Linz.

The following university institutes are supported within this focal point activity:

- TU Wien:
    - Institut für Festkörperelektronik
    - Institut für Allgemeine Elektrotechnik und Elektronik
- Johannes Kepler Universität Linz:
    - Institut für Halbleiterphysik
    - Institut für Experimentalphysik
    - Institut für Mikroelektronik

The results of these activities are outlined in this report beginning with page 9 (for the groups at the TU Wien) and page 55 (for the groups at the Johannes Kepler Universität Linz), respectively. The first of the reports in either section summarizes the work that benefited from the general GMe contribution to the basic laboratory operation; the subsequent reports pertain to projects specifically supported by the GMe.

2.2 Application Specific Integrated Circuits (ASICs) — UNICHIP

The UNICHIP activities of the GMe are closely linked to the requirements of the Austrian industry: Based on groups at the Technical Universities in Graz and Vienna, and using equipment and software which were purchased from GMe funding, two major actions are pursued: (1) ASIC projects for partners in the Austrian industry, ranging from feasibility studies to the design of ASICs that are commercially produced; and (2) the education and training of engineers in the area of ASIC design. Due to its close links to industrial requirements, UNICHIP played a leading role in Austria. The UNICHIP groups also have a long-standing tradition in European cooperation; many years before Austria joined the EU, they participated in the “EUROCHIP” European project; currently, they are involved in the “EUROPRACTICE” program.

The following university institutes partake in this focal point activity:

- TU Wien:
    - Institut für Allgemeine Elektrotechnik und Elektronik
- TU Graz:
    - Institut für Elektronik

The results achieved by the UNICHIP groups are presented in this report beginning with page 101.

2.3 Microsensors

One of the most rewarding potentials of microelectronics technology is related to applications in sensors: A large variety of possible sensors can be realized with comparatively modest technological resources, which makes them commercially quite interesting. In recent years, the GMe supported activities, mainly at the Technical University in Vienna, that led to sensors for medical, environmental, and technical applications, many of which could meanwhile be commercialized or have, at least, found commercial interest. Examples for such sensors are biosensors for metabolic parameters such as the concentrations of glucose and lactate, or temperature sensors that can be inserted into the combustion chamber of a Diesel engine.

The following university institute participates in this focal point activity:

- TU Wien:
  - Institut für Allgemeine Elektrotechnik und Elektronik

The current work done within the microsensors focal point activity of the GMe is disclosed from page 123 on.

2.4 Other Projects

Projects that are closely linked to microelectronics but do not belong to one of the above focal points have been supported on a smaller scale at the following institutes in 1995:

- TU Wien:
  - Institut für Allgemeine Elektrotechnik und Elektronik
  - Institut für Analytische Chemie
- Montanuniversität Leoben:
  - Institut für Physik

This report presents these supplementary projects of the GMe in 1995 beginning with page 135.

3. Discontinued Focal Point Activity: Ion Projection Lithography — IPL

The GMe pursued this project in close cooperation with the Viennese company IMS (Ion Microfabrication Systems), which has developed ion projection lithography to the stage of practical application. The GMe bought one of their first IPL units. Researchers at the Technical University Vienna, supported by the GMe, also contributed essentially with their scientific and technical work to the establishment of the IPL technology. This technology permits a reduction of the structure dimensions of microelectronic devices and micro-mechanical components well below 100 nm. The results stemming from the joint efforts of IMS and the GMe led to a world-wide interest in IPL; currently, IMS is constructing the first fully commercial machine for an American consortium. For the GMe, the IPL project has thus been successfully completed. Concluding work that has been done in 1995 is presented in the contribution “Microstructure Lithography” on page 137 of this report.

4. Other Activities of the Society

In addition to its contributions to research infrastructure, the GMe also has a longstanding tradition in supporting microelectronics-related meetings. In 1995, the GMe organized the biennial seminar "*Grundlagen und Technologie elektronischer Bauelemente*" in Großarl, Salzburg. The seminar has first been held in 1977; since 1987, the GMe contributes financial support, and since 1993, the Society acts as its main organizer. The 10th Großarl seminar comprised five main lectures given by international experts, and 24 short presentations most (but not all) of which resulted from work supported by the GMe.

5. Evaluation of the Society

In July 1995, the Austrian Federal Ministry of Science, Research and the Arts organized a monitoring of the GMe by external experts. The monitoring confirmed that the strategy chosen by the GMe was a very successful way to support technology oriented research. In particular, they gave credit to the function of the GMe as a bridge between industry and the universities. Accordingly, the funds invested in the GMe lead to an improved cooperation between the universities and Austrian industry.

The concluding statement of the experts was:

- *Impressive organization; very positive impression created by the qualification of the staff and by the infra-structure of the laboratories;*
- *Projects pursued are of high quality and show close cooperation between industry and universities;*
- *The GMe plays an important role for the work with students in education and development;*
- *Well-balanced criteria for the selection of projects;*
- *Recommendation to increase funding for the GMe by 2 Mio ATS over the next three years, with a particular dedication to the operation of the cleanroom facilities.*

Contents

Microelectronics Technology — Cleanroom Vienna

Microstructure Research: Cleanroom Vienna

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In this paper, the main activities in the cleanroom of the MISZ (microstructure center) are described. The cleanroom of the MISZ was opened 1993; during 1994, most of the equipment for the production of semiconductor devices was installed. Since 1995, state of the art growth of III-V compounds as well as the production of patterned masks used in lithography is done on a regular basis. We also give a short description of all projects running in our institute that are involved in the cleanroom. Projects sponsored additionally by the GMe are not described in detail.

One of the main research areas of our institute is the preparation and characterization of III-V devices. Therefore the fke maintains several collaborations with national and international research institutions and companies by providing them with epitaxial layers (III-V-compounds). A second main research topic is the production of micron and sub-micron devices down to nanometer scale. Patterned masks for optical lithography are also provided to different institutions.

1. Introduction

Since 1995, the cleanroom of the MISZ is running on a regular basis. Main research areas are the state of the art growth of III-V compounds and the production of patterned masks. Supplementary to the normal operation and maintenance of the cleanroom equipment, an additional wet bench was installed. Testing of the cleanroom quality and adjustment (laminar air flow, filters, cooling, humidity…) if necessary is done periodically.

As additional equipment, a Reactive Ion Etching machine (Oxford Plasmalab 80+) was bought and installed in the cleanroom of the MISZ in 1995. As process media, Ar, O_2, SF_6, Cl and $SiCl_4$ were installed. The RIE will mainly be used for three projects: the fabrication of nanostructures, surface grating couplers for semiconductor lasers, and GaAlAs selective etching processes for base contact formation in three terminal resonant tunneling devices. For nanostructure fabrication, $SiCl_4$ processes will be employed. At present, the three above processes are optimized to perform the final acceptance tests of the machine as soon as possible.

2. Research Activities

2.1 Pattern Generator

The Pattern Generator GCA 3600F is a fully automatic instrument to generate circuit patterns in photoresist as well as in high resolution emulsion materials. To achieve best results, however, at present the PG is run exclusively on photoresist-coated masks.

The PG-system includes a 20X-reduction lens with automatic focus motion to compensate for plate wedge, it has two interchangeable light sources for emulsion (flash lamp) and photoresist exposure (Hg-lamp), and a laser metering of X- and Y-stage position over 150 mm of stage motion in each coordinate. The stage position over 150 mm is specified in increments of 0.1 µm. The system has a variable aperture system which provides height, width and angle control of individual rectangular image elements used to generate an arbitrary circuit pattern, an instrument control system and a vacuum plateholder that is capable of accommodating 2.5” through 7”-plates in standard thicknesses from 0.06” through 0.25”. The PG is supported by a vibration isolation table and is enclosed in a GCA Environmental Chamber to guard against vibration, temperature change (accuracy of 0.1^{o}) and to ensure an adequate volume of clean temperature controlled air flow across the instrument during operation.

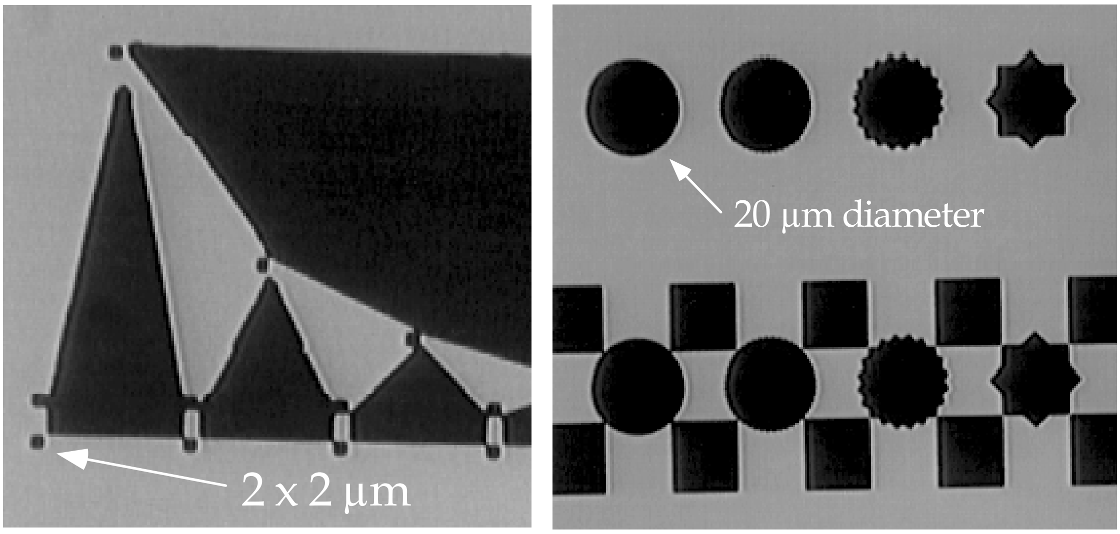

Fig. 1: Sample output of the pattern generator.

The PG is controlled by a DEC PDP 11 series digital controller, a 9 channel, 800 bit per inch, 10.5” reel magnetic tape unit, a system interface controller and a video keyboard terminal. The design of the mask patterns is done in AutoCad. The resulting dxf-files are translated in proper dwm-files by a special software (ASM 2600™ by Artwork Conversion Software). This allows the use of a PC 486 for the data transfer to the PG instead of the magnetic tape. The PG is used to expose patterns on standard photoplates, which are delivered by Hoya Corporation, Japan. A 350 W mercury-lamp is used as the light source. The photoplates are glass plates coated with a 800 Å thick Cr-layer and 500 nm thick AZ 1350 positive photoresist. The flatness of the plates is smaller than 5 µm over the whole plate size. The plate used are either 3.5”-size or 5”-size. The 5”-size are mainly used as master reticles for the photorepeater. The exposed plates are developed, etched with a chromium etch and finally cleaned with a photoresist remover.

The minimum feature size that can be exposed is 2 x 2 µm. The feature size can be increased up to 1300 µm in steps of 0.5 µm. Due to the useful conversion software the PG allows basically the generation of arbitrary patterns, rectangles, triangles and even circles, as is demonstrated in Fig. 1.

2.2 Photo Repeater

The GCA 3696 Photorepeater (PR) is a fully automatic instrument capable of exposing a 22 mm square image area on photoresist coated plates or directly on photoresist-coated wafers. A 5X g-line reduction lens (Zeiss Maximum 1000) permits the minimum feature size to a line width of 0.9 µm. System software allows conversational input dialogue to reduce errors and simplify specification of the system and the job to be exposed.

A laser position transducer with automatic compensation for atmospheric conditions and work piece temperature is employed to meter X- and Y-stage positioning over a 150 mm x 150 mm square exposable area. The system includes a matched illumination system with a 350 W mercury lamp, an automatic focus, a computer, and a video keyboard terminal. Like the PG, the PR is also supported by a vibration isolation table and is enclosed in a GCA Environmental Chamber.

5”-photomasks that were exposed with the PG are used as master reticles. The exposure of the structures can be either made on photomasks to achieve a minimum of 0.9 µm or directly on photoresist-coated wafers. If the wafers are coated with ultra-thin photoresist layers (thickness 100 nm up to 250 nm) the minimum feature size is as low as 0.4 µm. This size feature, however, can be only achieved under optimum conditions and is not a standard feature size for the PR.

This small feature size allows a direct exposure of sub-µm-structures to wafers. For the optimization of surface-plasmon-emitting LEDs, surface gratings with a period of 850 nm have been required. Conventional GaAs-LED’s have a non-directional emission and a low external quantum efficiency. If the surface of an LED is periodically structured and coated with a thin metal film, photons that usually would be lost by total reflection are coupled to surface plasmons (SP) at the metal-air interface. These SP decay by emitting p-polarized light. Depending on the grating’s shape, period, and groove depth, a strongly directional emission and an increased external quantum efficiency can be achieved.

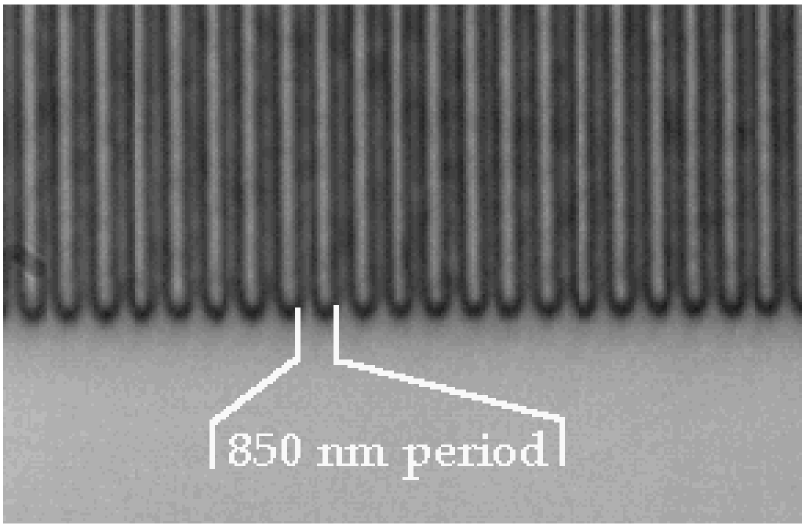

Fig. 2: Grating with a period of 850 nm exposed into a 250 nm thick photoresist layer on a GaAs-wafer

Rectangular gratings of 850 nm period with varying groove depths (55 nm to 180 nm) and different bar to space ratios had to be fabricated in order to find the optimal parameters for the excitation and light emission of surface plasmons. Due to the possible small feature size, the PR has been used to expose directly these required grating structures on the GaAs-LED-wafers. By changing the exposure time the width of the grating grooves has been systematically varied to find the optimum value for maximum surface-mode-emission from LEDs. Figure 2 shows a grating with a period of 850 nm exposed into a 250 nm thick photoresist layer on a GaAs-wafer. These gratings have been transferred into the substrate by ion-milling.

The good quality of the exposed gratings allowed an optimization of the LEDs. The far field radiation pattern and the external quantum efficiency of the LEDs have been measured. For p-polarized light the maximal peak-intensity was obtained at 90 nm and 120 nm groove-depth and a 1:1 bar to space ratio. The intensity was about 4 times higher than that of an unstructured LED. The beam divergences of the LED's were 7° (90 nm) and 10° (120 nm).

2.3 Growth of III-V Materials

MBE (molecular beam epitaxy) techniques allow the epitaxial growth of various compounds. Model materials for optoelectronics are epitaxial layers of III-V semiconductors, mainly GaAs and related compounds. The controlled growth of single crystalline layers on an atomic scale makes it possible to design new materials with optimized electrical and optical characteristics.

Epitaxial growth of $Al_xGa_{1-x}As$ on GaAs gives a band discontinuity in the conduction and valence band. Intentional doping influences the Fermi levels and increases the band offset at the interface. Electrons move from the n-doped $Al_xGa_{1-x}As$ into the non-doped GaAs and form a two dimensional electron gas (2DEG). The offset and the bending of the bands prohibit the recombination of the carriers with the ionized impurities in the $Al_xGa_{1-x}As$. Impurity scattering is the most dominant scattering mechanism at low temperatures. In a 2DEG this scattering process is drastically reduced due to the separation of carriers and impurities (”remote impurities”). This leads to electron mobilities up to 10^7 cm^2/Vs (4.2 K).

The modular GEN II solid source MBE machine is a system specially designed for high quality growth of III-V materials. Eight different sources can be used to grow AlAs, InAs, GaAs and any ternary compound (AlGaAs, InGaAs, AlGaAs) with different doping concentrations of Si. *In situ* RHEED measurements are used to monitor surface conditions and growth rate.

2.3.1 Installation and Setup of a Molecular Beam Epitaxy System for the Growth of III-V Semiconductors (G. Strasser)

A molecular beam epitaxy system for the growth of GaAs/GaAlAs heterostructures was installed and made “epiready” in 1994. The first epitaxial GaAs layers were grown in October 94 after baking and outgassing procedures of the system and the effusion cells. The first GaAs/AlGaAs layers with a 2DEG having mobilities exceeding 10^6 cm^2/Vs (at 4 K, without illumination) could be realized within one year. Since May 1995, heterostructures with international quality can be produced on a regular basis.

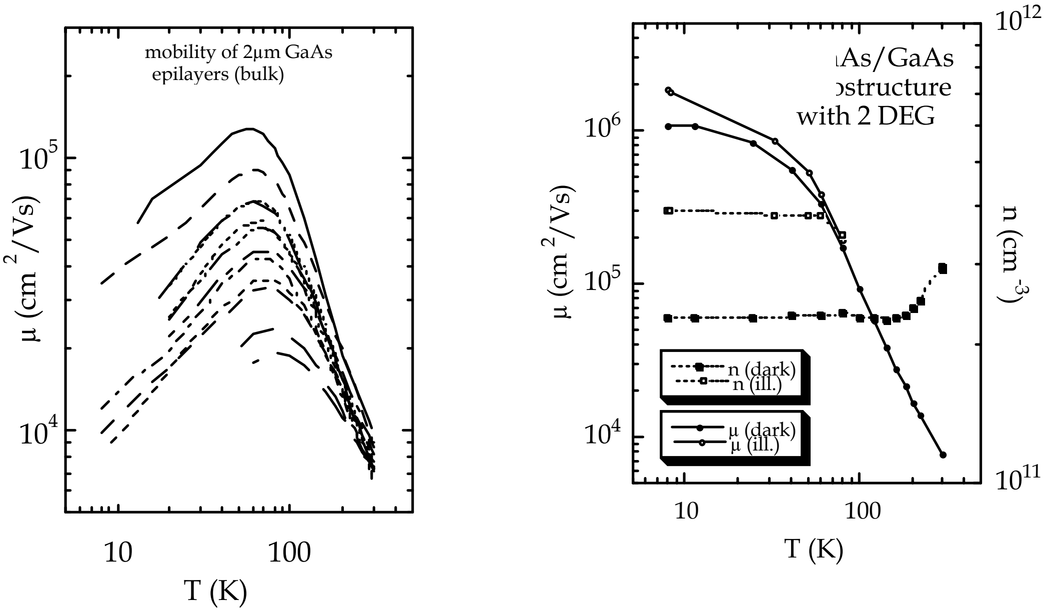

Fig. 3: Properties of the MBE grown epilayers.

2.3.2 Growth and Characterization of Modulation Doped High Mobility 2DEGs (G. Strasser, J. Smoliner, C. Eder, G. Ploner, V. Roßkopf, P. Auer, L. Hvozdara)

Two dimensional electron gases (GaAs/AlGaAs heterostructures) were grown with mobilities up to $1.5\cdot10^6$ cm^2/Vs at 4 K and $2.5\cdot10^6$ cm^2/Vs after exposure to red light. The sheet carrier concentrations vary from 0.5 to $5\cdot10^{11}$ $/cm^2$. Characterization was done via temperature dependent hall measurements (4 K to 300 K), SdH measurements, and cyclotron resonance absorption. Additional confinement by structuring and etching leads to quantum wire and quantum dot regimes. The optical and transport behavior of these low dimensional systems is investigated (for a more detailed description please see section 3.1 "Nano- and microelectronics").

2.3.3 Design, Growth and Characterization of Single and Multiple Quantum Wells (G. Strasser, W. Heiß, V. Roßkopf, J. Liu, C. Gmachl, N. Finger)

Quantum wells were designed to have subband transition energies in the FIR regime below the optical phonon energies (36 meV). Sheet carrier concentrations from 1 to $4\cdot10^{11}/cm^2$ were realized by remote delta doping to have reasonable mobilities (reduced scattering) in the wells. Well thickness, growth temperatures, spacer thickness between wells and doped layers, and doping concentration were systematically varied from growth to growth. Carrier concentrations were determined from hall and SdH measurements, subband transition energies from transmission studies in an FFT spectrometer. Relaxation times of intersubband energies were measured with a free electron laser (FELIX, Amsterdam). For growth rate and well thickness analysis, a photoluminescence setup was installed (for a more detailed description please see sections 3.3 "Far-Infrared-Spectroscopy" and 3.2 "Optoelectronics").

Fig. 4: TEM (left) and REM (right) pictures of MBE-grown Multiple Quantum Wells.

Multi Quantum Well structures (MQW) are grown on a diffusion stop layer (superlattice, not shown) and an 1 µm thick buffer layer to prevent diffusion of impurities from the bulk into the epilayers.

Carriers in the wells are set to $2 \cdot 10^{11}\mathrm{cm}^{-2}$ by doping profiles in the AlGaAs barriers 300 Å remote from the wells (Si delta doping).

2.3.4 Design, Growth and Characterization of RTDs and SIs (G. Strasser, C. Rauch, K. Unterrainer, W. Heiß, L. Hvozdara)

Resonant tunneling diodes (RTDs) with GaAs quantum wells and AlGaAs barriers were prepared. After characterization and optimization of these diodes, samples including stop layers (some monolayers consisting of pure AlAs) were fabricated. The first working “three terminal devices” with electron injectors, drift regions and a “filter” to separate ballistic from thermal carriers were realized in December 1995. Parallel to these activities, superlattice structures (GaAs/AlGaAs-superlattices with periods from 2 to 20 monolayers) were grown to investigate the doping behavior. Aim of this work is the realization of terahertz detectors and emitters (for a more detailed description please see section 3.3 “Far-Infrared-Spectroscopy”).

3. Summary

In this summary a short description of all those running projects of the institute of solid state electronics (fke) is given that are not directly involved in the growth of semiconductor materials but rely on III-V based samples and/or use devices patterned in the cleanroom (by optical, laser- or electron-beam lithography).

3.1 Nano- and Microelectronics

3.1.1 Vertical and Lateral Transport in Low-Dimensional Electron Systems (M. Hauser, G. Ploner, G. Rainer, J. Smoliner)

For vertical transport, tunneling spectroscopy is used to investigate nanostructured systems. Using a special double 2D GaAs-AlGaAs heterostructure, a situation can be achieved where electrons tunnel between a 2D electron system and quantum wires or quantum dots. By applying a voltage to the sample, the quantized states are shifted energetically with respect to each other, and therefore transitions between states of different dimensionality can be investigated. In terms of a transfer Hamiltonian formalism, the tunneling characteristics turn out to be the Fourier transforms of the wave functions in the 1D (0D) states, and therefore the experiments can be regarded as “Fourier transform tunneling spectroscopy”.

Lateral transport experiments have been performed on systems consisting of few quantum wires. The lateral patterning of the sample surfaces has been achieved by electron beam lithography and laser holography. The electronic transport properties of these quasi-one-dimensional electronic systems were investigated at low temperatures using magnetic depopulation experiments. At higher temperatures, magnetophonon resonances (MPR) were investigated systematically for the first time. It has been shown that both methods yield the same results for 1D subband spacing, and that MPR are particularly useful for the investigation of samples with high quantization energies and a small number of occupied subbands. In the quantum limit, this is the only way to determine the subband spacing, since magnetic depopulation experiments do not work in this case.

3.1.2 STM Studies on Quantum Wires (C. Eder, J. Smoliner)

Low temperature scanning tunneling microscopy (STM) studies were performed on quantum wires fabricated on GaAs-AlGaAs by laser holography and wet chemical etching. It was found that both tip and surface preparation have dramatic influence on the obtained results. Current-voltage curves were measured on the quantum wires and also in the depleted areas between the wires. On the wires, a tunneling current is observed for positive and negative sample bias, whereas in the depleted areas, tunneling is only observed for electron transitions from the valence band of the semiconductor into the STM tip. These features are due to surface depletion effects in the depleted areas. By comparison of current imaging spectroscopy data taken at room temperature and at $T = 4.2$ K, the width of the edge depletion can be determined directly.

3.1.3 Reliability and Characterization of Integrated Semiconductor Devices (P. Habas)

The hot-carrier reliability of fully overlapped-LDD CMOS devices called FOND (Fully Overlapped Nitride-etch Defined device) is investigated. Significant improvement in the hot-carrier resistance of FOND technology compared to standard LDD devices with the same effective channel length is completely explained by modeling and various experiments. The results provide understanding of the experimentally obtained reliability behavior of 0.35 µm MOSFETs and can be applied to optimize the design rules for these devices.

The applicability of charge-pumping technique to characterize the oxide/silicon interface in standard power VDMOSFETs (Vertical Double-diffused MOSFETs) is studied.

Qualitative analysis and analytical and numerical modeling show that charge-pumping measurements can be carried out in the subthreshold region. This conclusion is confirmed by various experimental results.

3.2 Optoelectronics

3.2.1 Laser-Probing of Integrated Semiconductor Devices (P. Habas, N. Seliger, D. Pogany)

Within a cooperation between the Institute and Siemens Munich, an optical measurement system has been developed that allows the contactless detection of free carrier concentrations and of the local lattice temperature in integrated semiconductor devices from the backside of the chip. With that new measurement set-up (heterodyne interferometer), switching operation in single bipolar transistors and MOSFETs, as well as in complex integrated circuits, has been analyzed. Self-consistent modeling of the probed device has been carried out. Studies of laser-probe signals in MOSFETs (in depletion conditions) show the applicability of the optical system for the determination of the substrate doping level.

3.2.2 Analysis of Thermal Effects in Power-VDMOSFETs and SOI-MOSFETs (P. Habas, N. Seliger)

Our current activities are focused on the study of heating phenomena in power VDMOSFETs, where the local temperature of the silicon substrate is optically determined by laser-probe measurements. The experiments are supported by numerical modeling of the heat propagation and by conventional measurement techniques (pulsed I-V). In addition, we apply a homodyne interferometer for the experiments on power MOSFETs in order to enhance the detection sensitivity. Results of this analysis are the basis for studies of heating phenomena in SOI-MOS structures and MOSFETs on SIMOX-wafers.

3.2.3 Application of the Laserprober for Microwave Systems (P. Habas, N. Seliger, D. Pogany)

At the end of 1995, a project has been started part of which considers the applicability of the backside-laserprober to the analysis of microwave signals (up to 20 GHz) in submicron devices.

3.2.4 Optimization of Surface Emitting LED's by Surface Plasmons (R. Hainberger, A. Köck)

Conventional AlGaAs/GaAs-DH LED's have a non-directional emission and a low external quantum efficiency. If, however, the surface of an LED is periodically structured and coated with a thin metal film, photons, which usually would be lost by total reflection, are coupled to surface plasmon (SP) at the metal-air interface. These SP decay by emitting p-polarized light.

In this work, rectangular gratings of 850 nm period with varying groove depths (55 nm to 180 nm) and various bar to space ratios were etched in order to find the optimal parameters for the excitation and light emission of surface plasmons. A 30 nm gold film was deposited on the grating.

The far field radiation pattern and the external quantum efficiency of the LEDs have been measured.. The beam divergences of the LEDs were 7° (90 nm) and 10° (120 nm). Broadening and a splitting of the peaks with increasing groove depths has been observed. This is due to a shift of the SP dispersion relation to higher k-values. An increase of the external quantum efficiency has also been observed, but this increase is mainly caused by the reduced light absorption in the GaAs top-layer.

3.2.5 Fabrication of Vertical Semiconductor Laser Structures by Ion Milling (N. Finger, C. Gmachl)

Structuring of vertical cavity surface emitting semiconductor laser diodes (VCSEL) based on GaAs/AlGaAs-structures with vertical and lateral dimensions in the order of magnitude of a few microns can only be achieved successfully by etching-techniques with anisotropic characteristics and little material selectivity. Ion milling complies with both demands to a high degree: It could be shown that etching of cavities based on VCSEL structures with vertical dimensions up to 3.5 microns with steep flanks (70 degrees) by using standard-techniques for the production of etch-masks (optical lithography) is possible. A numerical simulation was developed to calculate the development of the surface of the sample under ion-bombardment.

Furthermore it was shown that the monolithic integration of VCSEL and photodetectors is possible: An integrated LED-detector device was developed by using the vertical VCSEL structure both as LED and detector.

3.3 Far Infrared Spectroscopy

3.3.1 Studies on the Lifetime of Intersubband Transitions in Semiconductor Superlattices (W. Heiß, G. Strasser, E. Gornik)

Whether a semiconductor can be used for laser operation or not is determined by a population inversion of charge carriers, which is governed by the lifetime of electrons in excited states. In this work, the lifetime of electrons in excited states is investigated. The intersubband lifetime in GaAs/AlGaAs quantum well samples was directly measured. These pump and probe experiments were performed using the free electron laser "FELIX" in Nieuwegein (the Netherlands). The measured lifetimes of 400 ps in GaAs/AlGaAs are compared to calculated results of a theoretical model. This comparison shows that a combination of electron-electron scattering and optical and acoustical phonon scattering is limiting the electronic lifetime.

3.3.2 Development of p-Ge Far Infrared Lasers (W. Heiss, B. Fabianek, R. Zobl, K. Unterrainer, E. Gornik)

Up to now there is a large number of semiconductor lasers delivering coherent radiation in the spectral range of the visible and the near infrared. In the spectral range of the far infrared ($30\ \mu m < \lambda < 1000\ \mu m$) there are only two types of semiconductor lasers. These are the p-Ge cyclotron resonance laser and the p-Ge intervalenceband laser. Both laser types are tunable over a large frequency range. In this work, p-Ge lasers with various crystallographic orientations, sizes, and impurity concentrations are produced and investigated. It was shown in detail that the spectrum of the intervalenceband laser does depend sensitively on the acceptor species.

3.3.3 Far Infrared Spectroscopy of the Low Dimensional Electron Gas in GaAs/AlGaAs Material (V. Rosskopf, P. Auer)

In this work, various methods for characterizing low dimensional electron systems on GaAs/AlGaAs heterostructures are presented and discussed. The main focus is on magnetotransport measurements and the spectroscopy in the far infrared. Starting from non-structured two dimensional systems, the impact of lateral potential modulations on the electronic properties is investigated. Using holographic lithography and wet chemical etching, weakly and strongly modulated one- and zero-dimensional systems as well as isolated quantum wires are prepared. In these low dimensional systems, one expects to find collective charge density and single particle excitations.

In modulated 1D systems, the magnetoresistance shows a negative differential behavior and the appearance of a prominent maximum in the low magnetic field region, which can be explained in terms of the commensurability of the cyclotron radius and the lateral period of the wire pattern. The optically detected excitations in the far infrared reveal the occurrence of magnetoplasmons due to the quantization of the electronic states in the wires. From the frequency of this localized plasmons the subband quantization and the electrical width of the quantum wires are derived. Applying the above bandgap illumination to the wet chemical etched samples, a change from an isolated quantum wire via a modulated 1D system to a pure two-dimensional system could be achieved.

3.3.4 FIR and Tunneling Spectroscopy on HTc (Y. Sun, G. Strasser, V. Rosskopf)

In the project Po8179-MAT, ceramic high temperature superconductors (HTc) were composed, and out of these polycrystalline samples single crystalline films were prepared that were investigated in transport and optical measurements. The technology for preparing, doping, and structuring was developed, and the impact of the carrier concentration on the superconducting properties of the HTc-films was analyzed. In this project, thin YBCO-films with grating structures of the width 5 µm were defined. Experimental data and theoretical analysis show that these films could be used as a bolometer for the IR and may be suited for imaging systems at 77 K.

3.3.5 Ballistic Electrons in Semiconductor Heterostructures (C. Rauch, G. Strasser, J. Smoliner, W. Boxleitner, E. Gornik)

The improvements in the perfection of growth of semiconductor heterostructures (e.g. superlattices) using molecular beam epitaxy (MBE) have revived interest in making an extremely fast emitter of electromagnetic radiation. One of the basic requirements to realize the so-called Bloch oscillator is a long enough mean free path (mfp) of the oscillating hot electrons.

In order to investigate the mfp of ballistic hot electrons, a three terminal device was designed. In such devices, hot electrons are injected into a thin (10 nm) highly doped GaAs base via an AlGaAs tunnel barrier and are collected at the collector. As the hot electrons traverse the superlattice that has been grown in between the base and collector layer, they are used to probe scattering events.

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Publications in Reviewed Journals

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3. C. Eder, J. Smoliner, G. Strasser: “Local barrier heights on quantum wires determined by ballistic electron emission microscopy”, Appl. Phys. Lett., to be published.
4. P. Habas, R. Bellens and G. Groeseneken: “A Model Study of the Hot-Carrier Problem in LDD and overlapped LDD MOSFETs”, in Proc. of Int. Conf. on Insulating Films on Semicond. (INFOS), Grenoble (F), pp.285 – 288, June 1995.
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7. N. Seliger, P. Habas and E. Gornik: “Modeling and Measurements of Back-Side Laser-Probe Signals in MOSFETs”, in Proc. of ESSDERC, The Hague (1995), to be published.
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10. B. N. Murdin, W. Heiß, C. R. Pidgeon, E. Gornik, S-C. Lee, I. Galbraith, C. J. G. M. Langerak, H. Hertle and M. Helm: “Time resolved studies of intersubband relaxation using the free electron laser (invited)”, Proceedings of “Hot Carriers in Semiconductors IX”, Chicago, Illinois (July 31 – August 4, 1995), to be published in Plenum Press.
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21. V. Roßkopf, P. Auer, E. Gornik, R. Strenz, G. Abstreiter G.Böhm, G. Weimann: “Far-Infrared-Study of shallow etched Quantum Wires on High Mobility GaAs Heterostructures and Quantum-Wells”, Solid State Electronics, accepted for publication (1995).
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32. W. Heiß, K.Unterrainer, E. Gornik, B.N. Murdin, C.R. Pidgeon: “Observation of two emission lines inthe p-type Ge cyclotron resonance laser”, Proc. of the 22nd Int. Conf. on the Physics of Semiconductors (ed. D. J. Lockwood, World Scientific, 1995), p. 285.
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Presentations

1. P. Habas, R. Bellens and G. Groeseneken: “A Model Study of the Hot-Carrier Problem in LDD and overlapped LDD MOSFETs”, in Proc. of Int. Conf. on Insulating Films on Semicond. (INFOS), Grenoble (F), pp.285 – 288, June 1995.
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11. E. Gornik, W. Heiß, K. Unterrainer: "Far-infrared germanium cyclotron resonance lasers (invited)", submitted to International Semiconductor Device Research Symposium, Charlottsville, USA (December 5 – 8, 1995).
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17. W. Heiß, K.Unterrainer, E. Gornik, B.N. Murdin, C.R. Pidgeon: "Observation of two emission lines inthe p-type Ge cyclotron resonance laser", Proc. of the 22nd Int. Conf. on the Physics of Semiconductors (ed. D. J. Lockwood, World Scientific, 1995), p. 285.

Doctor's Theses

1. W. Boxleitner: "Untersuchung der Smith-Purcell-Emission in modulierten Halbleiterstrukturen", in progress.
2. C. Eder: "Temperaturabhängige Untersuchungen der elektronischen Eigenschaften niedrigdimensionaler Systeme", in progress.
3. C. Gmachl: "Frequenzverstimmbare, oberflächenemittierende Halbleiterlaserdioden mit vertikalem Resonator" (10/95).
4. A. Golshani: "Tunable Twin Guide Laser Diode for Steerable Surface Emission", in progress.
5. R. Hainberger: "Optoelektronische Verbindungstechnik mittels Halbleiter-Laserdioden", in progress.
6. W. Heiß: "Ferninfrarotspektroskopie an unipolaren Halbleitern — Relaxation und Emission" (7/95).
7. S. J. Michaelis: "Zwei-Photonen-Spektroskopie an GaAs und niedrig-dimensionalen GaAs/GaAlAs-Systemen" (3/95).
8. G. Ploner: "Tunnelspektroskopie und Transportphänomene bei niedrig-dimensionalen Elektronensystemen", in progress.
9. V. Roßkopf: "Spektroskopie strukturierter Elektronengase" (10/95).
10. N. Seliger: "Entwicklung von optischen Meßmethoden zur Analyse von hochfrequenten elektronischen Baulementen", in progress.
11. C. M. Rauch: "Smith Purcell Emission aus Halbleiterheterostrukturen", in progress.

Diploma Theses

1. P. Auer: "FIR-Spektroskopie niedrigdimensionaler Elektronengase in GaAs/AlGaAs-Heterostrukturen und Quantum Wells", in progress.
2. N. Finger: "Herstellung von vertikalen Halbleiterlaserlaserstrukturen mittels Ionenstrahlätzen", in progress
3. S. Freisleben: "Technologie von oberflächenemittierenden Halbleiterlasern basierend auf Oberflächenmodenkopplung" (9/95)
4. R. Hainberger: "Optimierung des Abstrahlverhaltens von LED's mittels Oberflächenplasmonen" (10/95)
5. L. Hvozdara: "Transporteigenschaften von Heterostrukturen und Übergittern", in progress.
6. J. Liu: "Elektrische und optische Charakterisierung von MBE-Schichten", in progress.
7. R. Zobl: "Optimierung von p-Ge Ferninfrarot - Laserkristallen", in progress.
8. E. Zotl: "Elektronenstrahllithographie für THz Bauelemente und Antennenstrukturen", in progress.

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18. Institut für Halbleiterphysik, Universität Linz, Doz. Helm (SLs, Qws)
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20. High Pressure Research Center, Academy of Sciences, Poland, Prof. Treciakowski (QWs) und Prof. Suski (QWs, 2DEGs)
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Fabrication of Two-Dimensional Arrays of Vertical-Cavity-Surface-Emitting Laser Diodes

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Two-dimensional arrays of vertical-cavity-surface-emitting laser diodes (VCSELs) have been fabricated by an ion-milling etching-technique. The etching of large-area VCSEL-arrays has been successfully demonstrated. A 2 x 2 array of VCSELs has been fully processed and characterized. The results achieved from these VCSELs clearly demonstrate that ion-milling is a very useful technique for the etching of VCSELs.

1. Introduction

Vertical surface emitting laser diodes (VCSELs) are an excellent answer to the need of surface-emitting lasers due to their small size, planar geometry, integrability and potentials for high power and high quality beams. VCSELs can be fabricated in two-dimensional arrays, because they have integrated resonator mirrors (Bragg-mirrors) and require no cleavage. Therefore VCSELs are ideal candidates as light emitters in integrated optoelectronics devices.

The goal of this project was the fabrication of two-dimensional arrays of VCSELs through application of a proper etching technique. The complex processing of VCSELs requires more sophisticated etching techniques than the simple wet-chemical etching technique. Therefore, an Ion-milling etching technique was used for the fabrication of two-dimensional VCSEL-arrays.

2. Sample Structure

VCSELs are grown by molecular-beam-epitaxy (MBE) or by metal-organic-chemical-vapor deposition (MOCVD). The geometry of a VCSEL-structure is shown in Fig. 1. First a Bragg-mirror, which consists of 20 – 30 pairs of alternating (λ/4) GaAs/Al(Ga)As layers, is grown on the substrate. The thickness of a (λ/4) layer is typically between 60 nm and 80 nm. Next is a cladding layer of AlGaAs, the GaAs active region and a further cladding layer of AlGaAs. The structure is completed by a second Bragg-mirror on top, which consists of another 20 – 30 pairs alternating (λ/4) GaAs/AlGaAs layers. The total thickness of the entire grown structure is 3 – 5 µm.

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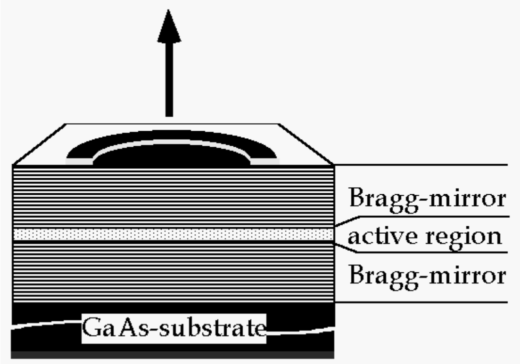

Fig. 1: The geometry of a VCSEL-structure with a Bragg-mirror both on the substrate-side and on top. The Bragg-mirror consists of 20 – 30 pairs of alternating (λ/4)-layers of GaAs/Al(Ga)As.

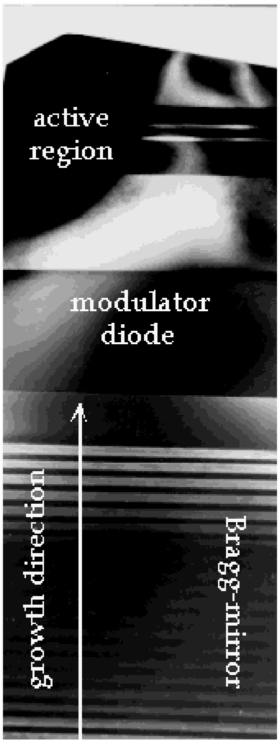

Fig. 2: TEM photograph of a frequency tunable VCSEL.

In addition to conventional VCSELs with Bragg-mirrors on the substrate side and on the top side, frequency tunable VCSELs with integrated modulators have been processed. This type of VCSEL is of high importance for wavelength-division-multiplexing techniques in optical communication. These special VCSELs have an integrated modulator diode in the cavity, but no Bragg-mirror on top. To illustrate the real geometry of a VCSEL-structure, a TEM photograph of a frequency tunable VCSEL is shown in Fig. 2. This sample consists of a p-n-p structure embedded between an undoped Bragg mirror with 24 pairs of alternating layers of AlAs and $Al_{0.10}Ga_{0.90}As$ at the bottom and a 500 Å thick silver mirror on top. The modulator diode is formed by an $Al_{0.15}Ga_{0.85}As$ pn-junction with an intermediate $Al_xGa_{1-x}As$ ($x = 30/15$) grading layer. The modulator is directly followed by a GaAs/AlGaAs double-hetero junction laser diode. The two diodes share the same n-contact layer, which is directly connected to ground during experiments thus electrically separating the two diodes.

3. Etching Technique and Experimental Results

For processing VCSELs, single mesas have to be etched into the substrate. This requires at least one etching step where the whole structure is etched down to the substrate. The etching of the alternating GaAs/Al(Ga)As mirror-layers cannot be achieved by conventional wet-chemical etching techniques, because the different etching-rates of the GaAs- and the Al(Ga)As layers result in highly non-uniform etching walls. This limits the minimum size-feature, which can be etched and strongly limits the electronic and optical characteristics of the VCSEL. In addition, wet chemical etching is not suitable due to very strong underetching in the upper Bragg mirror.

Therefore, the processing of VCSELs requires a more sophisticated etching technique, which is less material selective than the wet-chemical etching technique. An ion-milling machine (Millatron 8) using Ar^+-Ions with energies between 200 eV and 1000 eV was used to develop the etching technique for processing the VCSEL structure into mesas.

First of all, the etching rates of proper etching-masks have been measured. Photoresist was found to be a useful mask for the etching process. The etching rate of photoresist is around 4 nm/min. Also Ti-films and Cr-films were used as etching masks. The etching rates of both metals, however, are approximately the same as in case of the photoresist. As the evaporation of the metal-masks requires an additional processing step, photoresist is more suitable.

The etching rates of GaAs and AlGaAs are 17 – 19 nm/min and 15 – 18 nm/min, respectively, depending on the angle of incidence of the sputtering Ar^+-Ions. As the difference between both rates is small, this technique is very well suited for the etching of the Bragg-mirrors. An Ion-milling simulation program has been developed to predict etching profiles and has been found to be in excellent agreement with the experimental results [1], [2].

Fig. 3 shows the result of etched two-dimensional VCSEL-arrays with Bragg-mirrors on the top and on the substrate side. While in GaAs-substrates even vertical walls have been achieved by ion-milling, Bragg-mirrors of VCSELs show a steepness between 60^o and 80^o. This, however, can still be optimized to achieve vertical walls.

After the setup of the ion-milling etching technique and the demonstration of etched two-dimensional VCSEL-arrays, a 2 x 2 array of VCSELs was fully processed and electrically contacted to measure the performance of ion-milled VCSELs. For these arrays, VCSELs with integrated modulator-diodes have been used. First the laser diode is mesa etched (30 x 30 μm) to the common n-contact layer. Further etching defines a rectangular mesa for the modulator diode. Subsequent evaporation of the top, intermediate, and bottom contacts gives independent access to the laser and the modulator diode. The top contact shows a window with a silver coating where the laser emission is coupled out.

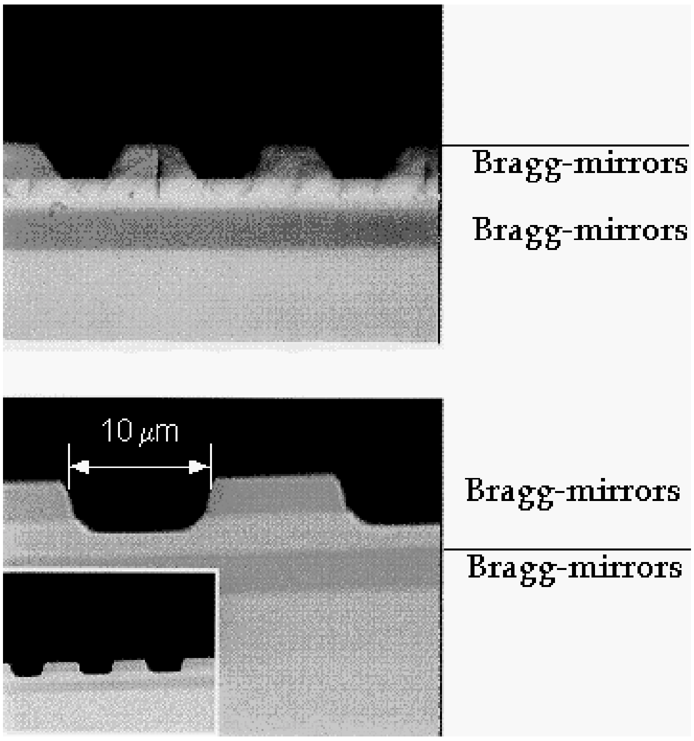

Fig. 3: Arrays of VCSEL-structures etched by ion-milling.

All measurements were carried out at room temperature under pulsed current operation. Fig. 4 shows the characteristic P-I-V diagram of a typical VCSEL. Its threshold current density varies from 3 kA/cm^2 to 9 kA/cm^2, which is a very reasonable value for this structure. Fig. 5 shows an emission spectrum of the laser diode, which demonstrates the influence of lateral variations of the injected current on their transversal mode spectra. For high modulator current (higher than 50 mA) the VCSELs showed a transversal mode switching from TEM_{00} to TEM_{10} as a result of a laterally inhomogeneous modulation of the cavity. (The order of the modes has been identified by means of spectral evaluation and their near field patterns.) The wavelength tuning of these VCSELs and the effect of the modulator current is discussed in detail in [3] – [8].

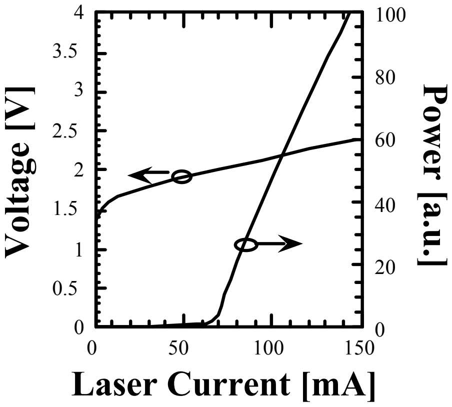

Fig. 4: P-I-V diagram of a GaAs/AlGaAs double-hetero junction VCSEL with an integrated AlGaAs pn-modulator diode.

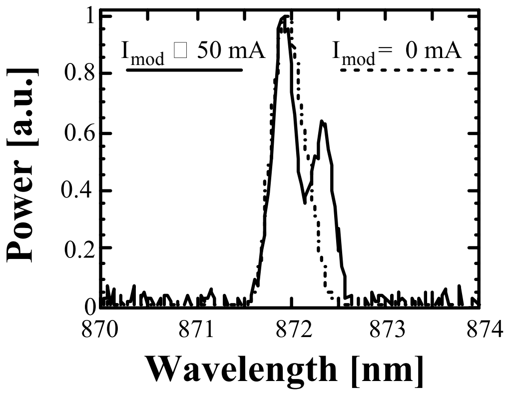

Fig. 5: Emission spectra of a longitudinally single-mode VCSEL showing transversal mode switching with the modulator current.

4. Conclusion and Outlook

Within this project, two-dimensional arrays of VCSELs have been fabricated by an ion-milling etching-technique, which has been set up. The etching of large-area VCSEL arrays has been successfully demonstrated. A 2 x 2 array of VCSELs has been fully processed and characterized. The results achieved from these VCSELs clearly demonstrate that ion-milling is a very useful technique for the etching of VCSELs. It will be used for the fabrication of larger VCSEL arrays as a source for direct optical interconnects between stacked boards in computers.

Acknowledgment

This work was partly supported by the “Stiftung Volkswagenwerk”, Hannover, Germany.

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[2] A. Köck: “Präparation und Charakterisierung von frequenzdurchstimmbaren VCSEL”, *Photonik-Symposium, der Volkswagen-Stiftung*, 4. – 6. Oktober 1995, Braunschweig, Germany.

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[4] C. Gmachl, A. Golshani, N. Finger, A. Köck, E. Gornik: “Preparation and characterization of vertical-cavity surface-emitting lasers with integrated modulators”, *7th*

Brazilian Workshop on Semiconductor Physics, 16. – 17. Juli 1995, Rio de Janeiro, Brasil.

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[6] C. Gmachl, A. Golshani, A. Köck, E. Gornik; J.F. Walker: “Vertical-cavity surface-emitting lasers with monolithically integrated modulators”, Proceedings of the *NATO-Workshop* “*Quantum Optics in Wavelength Scale Structures*”, 26. August – 2. September 1995, Cargese, Corsica, France, to be published in NATO Series, Kluwer Academic.

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[8] C. Gmachl: “Frequency tuning of VCSELs by a monolithically integrated modulator diode”, Oral presentation at AT&T Bell Laboratories, Murray Hill, NJ, USA 1995.

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Publications in Reviewed Journals

1. C. Gmachl, A. Golshani, N. Finger, A. Köck, E. Gornik: “Preparation and characterization of vertical-cavity surface-emitting lasers with integrated modulators”, Proceedings of the “7th Brazilian Workshop on Semiconductor Physics”, 16. – 17. Juli 1995, Rio de Janeiro, Brasilien, in print.

2. C. Gmachl, A. Golshani, A. Köck, E. Gornik; J.F. Walker: “Vertical-cavity surface-emitting lasers with monolithically integrated modulators”, Proceedings of the NATO-Workshop “Quantum Optics in Wavelength Scale Structures”, 26. August – 2. September 1995, Cargese, Corsica, France, to be published in NATO Series, Kluwer Academic (1995).
3. C. Gmachl, A. Golshani, A. Köck, E. Gornik; J.F. Walker: “Frequency tuning of VCSELs by a monolithically integrated modulator diode”, Proceedings of the “8th Annual Meeting IEEE Lasers and Electro-Optics Society”, 30. October – 2. November 1995, San Francisco, CA, USA.

Presentations :

1. C. Gmachl, A. Köck, A. Golshani, S. Freisleben, E. Gornik, J.F. Walker: “Emissionscharakteristik von frequenzverstimmbaren oberflächenemittierenden GaAs/AlGaAs-Halbleiterlaserdioden mit vertikalem Resonator”, Frühjahrstagung der Deutschen Physikalischen Gesellschaft, Fachverband Quantenoptik, 27. Februar – 3. März 1995, Innsbruck, Austria.
2. C. Gmachl, A. Golshani, A. Köck, E. Gornik; J.F. Walker: “Vertical-cavity surface-emitting lasers with monolithically integrated modulators”, NATO-Workshop “Quantum Optics in Wavelength Scale Structures”, 26. August – 2. September 1995, Cargese, Corsica, France.
3. N. Finger, R. Hainberger, C. Gmachl, A. Köck, E. Gornik, J.F. Walker: “Herstellung von zweidimensionalen Feldern oberflächenemittierender Halbleiter-Laserdioden mit vertikalem Resonator mittels Ion-Milling”, 45. Jahrestagung der Österreichischen Physikalischen Gesellschaft, 18.-22. September 1995, Leoben, Austria.
4. A. Köck: “Präparation und Charakterisierung von frequenzdurchstimmbaren VCSEL”, Photonik-Symposium der Volkswagen-Stiftung, 4. – 6. Oktober 1995, Braunschweig, Germany.
5. C. Gmachl: “Frequency tuning of VCSELs by a monolithically integrated modulator diode”, Oral presentation at AT&T Bell Laboratories, Murray Hill, NJ, USA 1995.

Doctor’s Thesis

1. Claire Gmachl: “Frequency tunable vertical-cavity surface-emitting lasers”, 1995.

Cooperations

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2. Siemens AG München

Scanning Tunneling Spectroscopy on Nanometer Scale Semiconductors

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In this project, Scanning Tunneling Spectroscopy (STM) studies on (100) surfaces of GaAs/AlGaAs quantum wire structures in dry nitrogen ambient are reported. For this purpose, ultrafine tungsten tips were fabricated by electrochemical etching. Measuring the IV-curves on the wires and in the etched areas between the wires, distinct local differences between *I-V* are found even at room temperatures. This enables us to clearly observe quantum wire regions with current imaging tunneling spectroscopy at 300K. The observed differences are ascribed to the internal potential profile in the sub surface regions of the sample. In this sense, the STM tip can be understood as a potential probe of the sub surface regions of a laterally structured sample.

1. Introduction

The goal of the project was to use a scanning tunneling microscope (STM) on nanostructures that were fabricated by laser holography on GaAs-AlGaAs heterostructures. As the scanning range of the STM is limited to a range of 10 µm x 10 µm, large arrays of quantum wires having a period of typically 0.5 µm were fabricated on the samples. Thus, several quantum wires are always within the scanning range of the STM.

On such a large array of laserholographic quantum wires or quantum dots a STM can be used to establish a contact to individual structures inside the array. The STM at the Institut für Festkörperelektronik is capable to work at low temperatures and at high magnetic fields allowing magnetotunneling experiments on single quantum structures. Thus, low temperature images of the samples can be recorded and due to the atomic resolution, even local tunneling characteristics can be measured on single structures.

2. Tip Preparation

To perform successful measurements on nanostructured systems like quantum wires and quantum dots, one has to make sure that the radius of the used tip is small compared to the size of the investigated structures. Especially the large aspect ratio of the surface profile (stepsize ≈ 10 nm) requires ultrafine STM tips for proper surface scans. To minimize the influence of the STM tip geometry on the results, special electrochemically etched tips were used. A wire acts as an electrode in an electrochemical cell and is etched by an external voltage. Figure 1 schematically shows the corresponding experimental setup. To produce ultrafine tips, a process was realized that is sensitive to strong changes in the cell current and stops the etching process when the part of the wire that is below the surface of the etchant falls off. For this purpose, a tungsten wire (0.5 mm diameter) is dipped 1 mm into a 1 mol NaOH etchant.

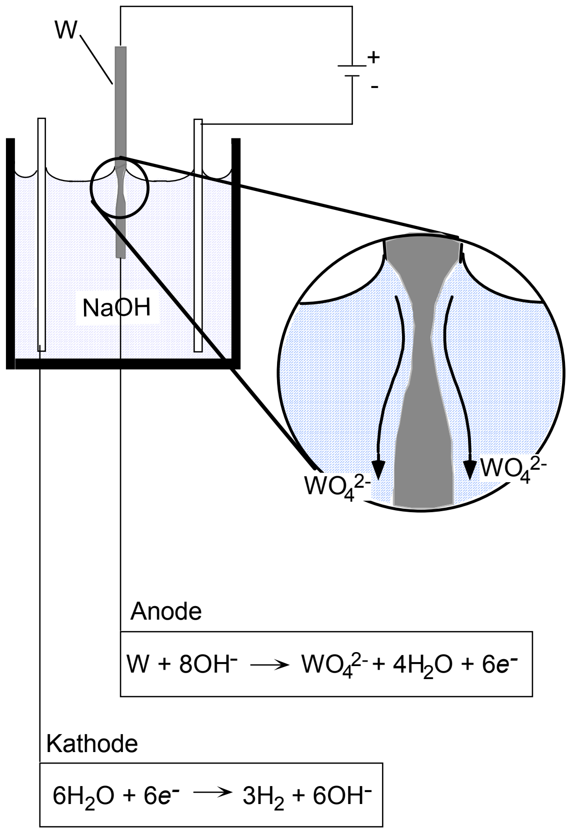

Fig. 1: Experimental setup for electrochemical tip fabrication.

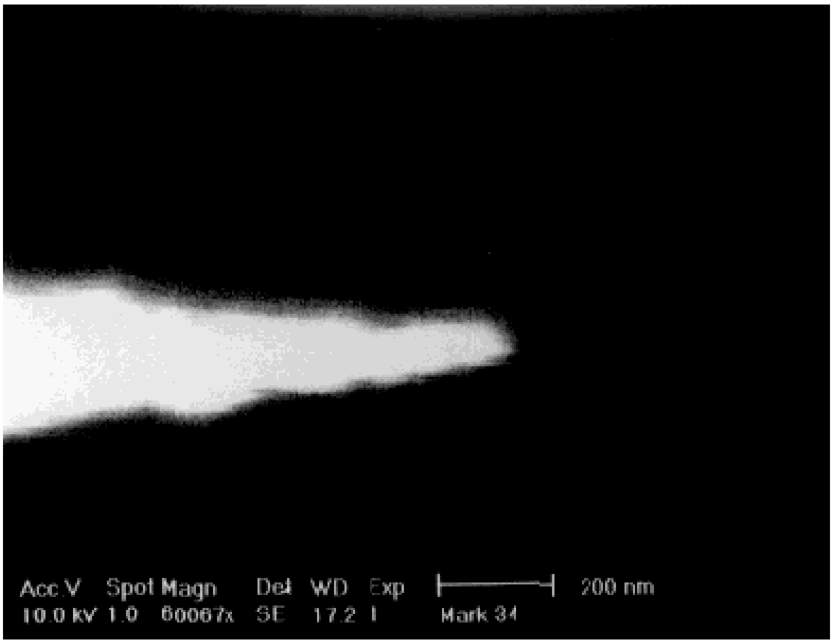

Fig. 2: Scanning electron microscope image of a typical tip. The tip radius is smaller than 50 nm.

The initial voltage is in the range between +6V and +20V. Changes in the cell resistance are electronically derived and compared with a reference value V_{th}. This value is chosen in a way that a comparator triggers at that moment when the lower part of the wire falls off. The trigger signal switches the external voltage off and stops further etching, which would result in a destruction of the tip. In this way, tips with radii below 50 nm and arbitrary aspect ratio can be realized (see Fig. 2).

3. Current Imaging Spectroscopy on Quantum Wires

One of the most difficult things for successful STM measurements was the choice of STM suitable samples on the basis of GaAs-AlGaAs heterostructures. In STM measurements on conventional samples, electrons have to tunnel through the vacuum barrier, then through an GaAs cap layer, and finally through a thick AlGaAs barrier, before they can reach the collector electrode. The resulting transmission coefficients of all barriers together result in extremely small tunneling currents, which cannot be measured with the present electronics of our STM. To overcome these problems, inverted heterostructures were used. On such samples, the 2DEG is located on top of the AlGaAs directly below the surface. If the surface doping is high enough, the barrier to the surface is thin and the resistance between the 2D channel and the surface can be neglected. Now tunneling processes between tip and 2D gas can be investigated directly.

In the following, we report on first STM studies of wet chemically etched quantum wire structures on inverted heterostructure samples in a dry nitrogen ambient at room temperature. Even at 300 K we find a distinct spectroscopic difference between non etched sample regions and regions where the underlying electron gas has been depleted by etching. This difference enables us to detect the quantum wire regions from CITS and not only from topographic imaging.

The samples which we used for the experiments were inverted GaAs/AlGaAs heterostructures that consist of a semi-insulating substrate, a 2 μm GaAs buffer layer, followed by a 200 Å undoped $Al_XGa_{1-x}As$ layer, a 50Å doped $Al_xGa_{1-x}As$ ($N_D = 2x10^{18}$ cm^{-3}) layer and again by a 250Å undoped $Al_xGa_{1-x}As$ spacer layer ($x = 0.35$). On top, the samples consist of 800Å of low doped GaAs ($N_D = 1.2x10^{15}$ cm^{-3}) and finally of a 150 Å highly doped GaAs surface layer ($N_D = 6.2x10^{18}$ cm^{-3}). The structure results in a concentration of free electrons close to both the GaAs/AlGaAs interface and the AlGaAs/GaAs interface[1] even at 300K.

Lateral pattering of the sample was achieved by laser holography and subsequent wet chemical etching, which partially depleted the underlying upper electron layer of free carriers. The electron layer underneath the AlGaAs barrier is not affected by this treatment. This procedure yielded large arrays of quantum wires with a period of 475 nm with an etch depth of about 120Å. Note that despite this fine etching the uppermost layer of the sample does not have an altered dopant concentration, as some 30 Å of the highly doped surface layer are still left. At least two ohmic contacts were prepared by standard Au-Au/Ge-Ni alloying. The STM tip is then used to probe the sample by measuring the tunneling current between tip and sample as a function of applied voltage and/or position (Fig. 3).

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[1] Band profiles were calculated using the one dimensional Poisson/Schrödinger equation solver by Greg Snider, Applied and Engineering Physics department, Cornell University, Rev. 3/12/93

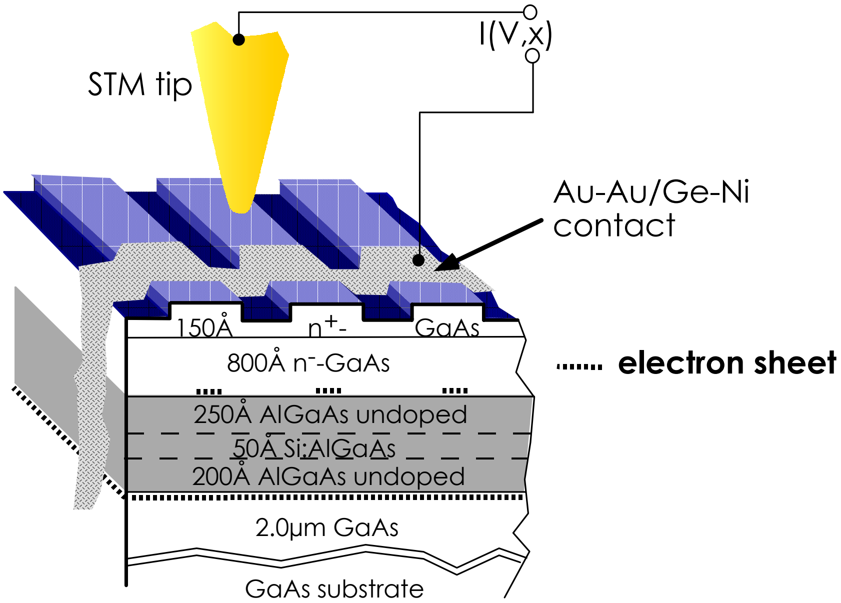

Fig. 3: Sample structure used for the measurements. Carriers are concentrated close to both the GaAs/AlGaAs and the AlGaAs/GaAs interfaces. After etching, some regions of the upper electron layer are depleted of free carriers.

A key element for the experiments was surface preparation, as all measurements were carried out in ambient pressure. In order to remove native oxides, the samples were dipped into a HCl:H_2O solution for 30 sec, shortly rinsed in DI water and blown dry with nitrogen. Afterwards they were immediately transferred into the STM chamber, which was purged with dry N_2 to prevent further oxidation of the surface. After this treatment, only a thin oxide layer remains, resulting in exact topographic profiles of the etched structures. The dry N_2 flow was continued during the measurements as otherwise the STM image deteriorated within minutes. A comparable effect was found by Pischow *et al.* [1]. They state that the water bound to the native oxide layer of polished Si wafers, not so much the oxide layer itself, causes difficulties associated with STM work. We conclude that the N_2 flow prevents condensation of water at the surface and allows satisfying tunneling conditions despite a possible thin oxide layer.

Special attention was also paid to tip geometry. For sample structures with large corrugations in comparison to atomic dimensions, artifacts are readily introduced into topographic images due to the influence of tip shape. To prevent this, only sharp Au-sputtered W-tips with radii of less than 20 nm have been used. The aim of this work was to identify quantum wire regions on (100) surfaces from spectroscopic studies, not only from topographic imaging. This is not straightforward, since at the etched regions the sample is depleted of free carriers. This could lead to charging effects that prevent STM studies. Fig. 4 (a) shows *I-V* curves obtained at 300K on non-etched — i.e. on the wire — and on etched regions of the sample. A distinct qualitative spectroscopic difference between the etched and the non-etched regions is found. In the non-etched regions *I-V* curves resemble curves expected for a metal-vacuum-metal (highly doped semiconductor) junction in the intermediate emission regime between vacuum tunneling and the Fowler-Nordheim region [2]. We obtained equivalent curves on unstructured reference samples. In the etched regions, however, the *I-V* curves show a diode-like behavior with no current flow for positive sample bias. As mentioned above, in this case one might even expect current flow to be prohibited for both bias directions, as charging of the sample in the depleted areas might be expected immediately due to the lack of free carriers. This was not observed. Rather, standard topographic imaging and tunnel gap control are still possible for all sample regions if the sample bias V_t is chosen to be negative.

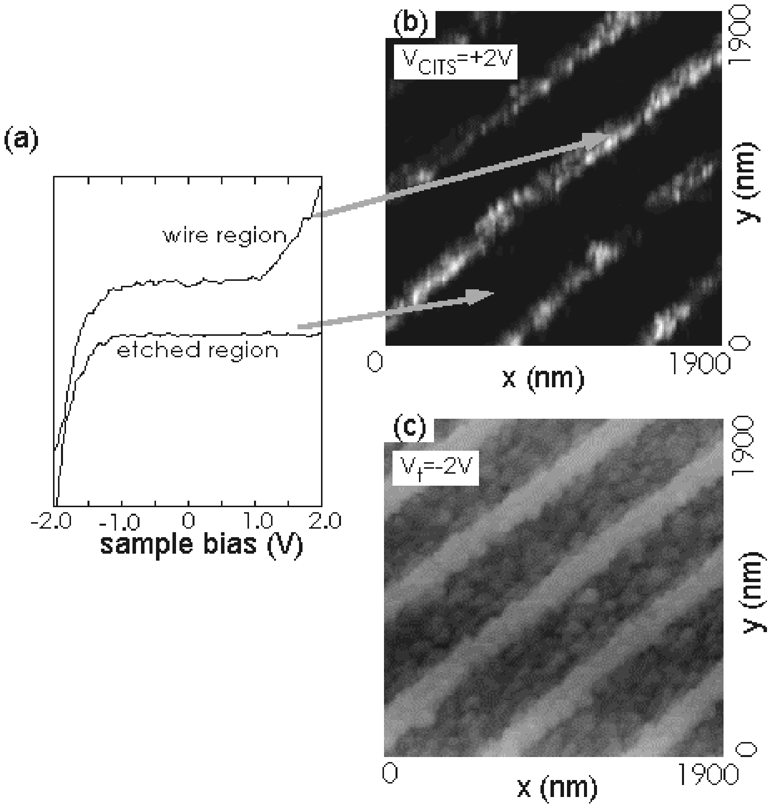

Fig. 4: *I-V* curves obtained on non-etched (i.e. wire) and etched areas of the quantum wire sample with $\Lambda = 475$ nm (a). For the etched regions, injection of electrons into the sample is not possible. Current flow (bright lines) in the CITS image measured at $V_{CITS} = +2$ V thus corresponds to the quantum wire regions (b). Quantum wires in the simultaneously obtained topographic image (c). Tunneling parameters for the gap hold were set to -2 V/-100 pA in all cases.

The measured spectroscopic features can be utilized for CITS. For CITS, the sample surface is scanned in standard constant current mode with suitable parameters for the tunnel gap hold. Additionally, the feedback control loop is opened for specified pixels. The voltage is then set to some chosen value and the resulting current is measured without feedback control. The current image thus represents the current value for a given voltage as a function of the lateral x and y coordinates. CITS can have the same resolution as the topographic image.

Fig. 4 (b) shows the 1.9 µm x 1.9 µm CITS image, Fig. 4 (c) the simultaneously obtained topographic image of a quantum wire array with a period of $\Lambda = 475$ nm. For fixing the tunnel gap and for topographic imaging, a negative sample bias was chosen. The CITS image was measured at positive sample bias. As expected, no current can be detected in between the wires (dark region). The quantum wire regions, however, are clearly visible in the CITS image (bright).

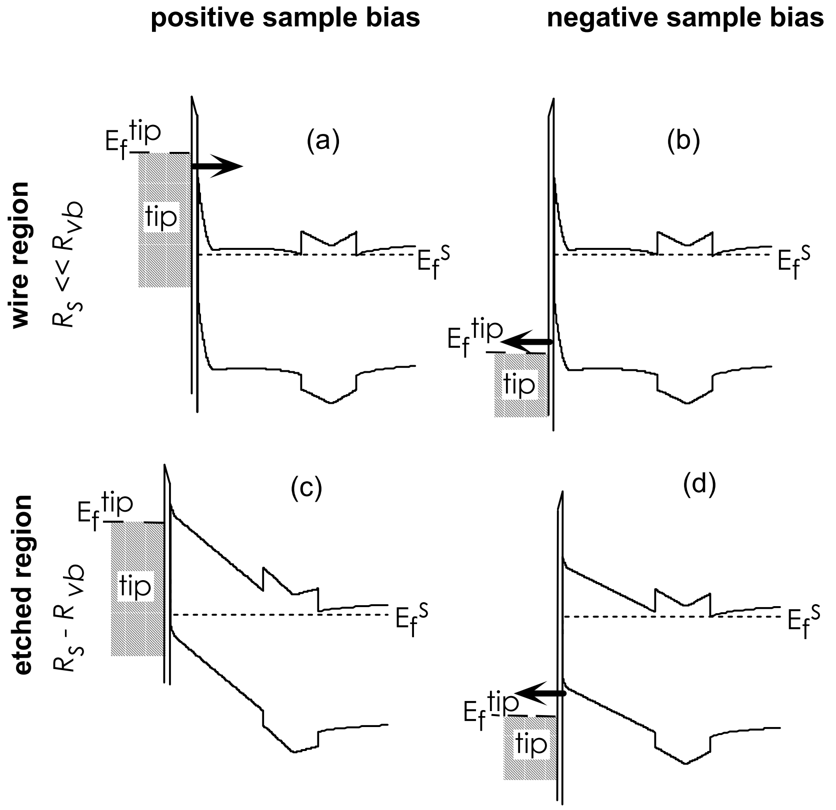

Fig. 5: Sample band profiles and tip Fermi level position for the wire region at positive (a) and negative sample bias (b) as well as for the etched sample region at positive (c) and negative sample bias (d). The arrows indicate current flow across the vacuum barrier. At the etched region, current flow is prohibited for positive sample bias due to the large voltage drop in the sample.

Figure 5 explains the observed spectroscopic differences by taking into account self consistently calculated semiconductor band profiles and tip Fermi level positions. Figure 5 (a) shows the situation for non etched regions of the sample. Due to the special structure of our samples (very small surface space charge region due to high doping), the resistance R_s from the upper electron layer to the sample surface is very low compared to the tunneling resistance R_{vb} across the vacuum barrier. This could be confirmed in previous measurements [3]. An electron injected from the STM into the sample will thus be collected in the upper electron layer. The collection will take place by surface states and subsequent tunneling through the surface space charge layer or by direct injection into the semiconductor conduction band. For negative sample bias (Fig. 5 (b)), mainly electrons from the valence band of the semiconductor will tunnel through the vacuum barrier. Recombination of holes with free electrons from the sub surface electron layer via surface states will prevent charging of the sample.

In the etched regions of the sample where the upper electron layer is depleted, R_s is much larger due to the enhanced depletion region at the sample surface. Thus a part of the applied voltage will also drop across the sample, not only across the vacuum barrier.

Additionally, there exists an n^{-}-n^{+}-junction between the etched and the non-etched regions, where free carriers are present. This leads to an internal diode R_d.

Figure 5 (c) shows the situation for positive sample bias. Due to the large voltage drop *in the sample* the tip Fermi level can not be raised above the Schottky barrier at the sample surface. This rules out carrier injection into the conduction band. However, for negative sample bias, electrons are injected into the etched region from the wire regions by forward biasing the internal n^{+}-n^{-}-diode. These will be able to reach the sample surface as the tunneling voltage this time reduces R_s. Thus current flow without charging of the sample is possible despite the fact that this region of the sample is depleted of free carriers. As mentioned above, this is very important as it allows standard topographic imaging of our samples at $V_t < 0$.

4. Summary

In summary, it was shown that an STM can be used to characterize sub surface quantum wire arrays at 300K and in ambient pressure. By local injection of carriers into a special sample structure, the spectroscopic differences between etched and non-etched regions can be utilized for CITS. The observed differences are ascribed to the internal potential profile in the sub surface regions of the sample. In this sense, the STM tip can be understood as a potential probe of the sub surface regions of a laterally structured sample.

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Publications in Reviewed Journals

1. C. Eder, J. Smoliner, G. Strasser: “Local barrier heights on quantum wires determined by ballistic electron emission microscopy”, to be published in Appl. Phys. Lett.
2. C. Eder, J. Smoliner, G. Böhm, G. Weimann: “Room temperature current imaging tunneling spectroscopy of GaAs/AlGaAs quantum wires at ambient pressure”, submitted to Appl. Phys. Lett.
3. C. Eder, J. Smoliner, G. Böhm, G. Weimann: “Low Temperature Current Imaging Tunneling Spectroscopy on Wet Chemically Etched Quantum Wires”

Presentations

1. J. Smoliner, STM Studies on Quantum Wire Systems, *Int. Workshop on Superconductors and Correlated Systems*, Planneralm (1996).

Doctor’s Thesis

1. Claudia Eder, STM studies on nanostructured systems, in progress.

Cooperations :

1. Walter Schottky Institut, TU-München
2. Weizmann Institute of Sciences, Rehovot, Israel

Installation and Operation of the Electron Beam Lithography System

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The existing electron beam lithography (EBL) system consisting of a slightly modified JEOL 6400F with beam steering soft- and hardware was enhanced by an additional lithography control system. The combined EBL system yields higher resolution and is capable of marker recognition, correction of field distortion, size and rotational corrections implemented in fast hardware. It was used to realize nanostructured resist masks on GaAs substrates produced by G. Straßer, Prof. M. Heiblum (Weizmann Institute of Science, Israel) and Dr. J. Walker (Laboratorio TASC, Italy). These masks were wet chemically etched to form semiconductor quantum wire arrays and single quantum wires. Investigations of lateral transport of the wire arrays revealed new correlation effects. On single wires high field transport was investigated. The EBL system was also used as a tool for the optimization of vertical emitting heterostructure lasers, which led to strongly enhanced far field patterns.

1. Introduction

The EBL system at the Institute of Solid State Electronics was used for miscellaneous applications, ranging from low temperature lateral transport investigations of quantum wire arrays and single quantum wires to air bridged high speed Schottky diodes for THz devices and fs-correlation detectors operating at room temperature. It was also found to be an essential analysis tool used in the optimization process for surface gratings used in vertical emitting laser diodes.

2. Electronic Properties of Low Dimensional Electron Systems

Magnetophonon resonances (MPR) have been clearly resolved on nanoscale arrays of quasi one dimensional quantum wires and were used for the first time to systematically study the characteristic properties of such systems.

At temperatures around 100 K, MPR result from resonant scattering of electrons by LO phonons between electronic sublevels induced by the confining potential. The resulting resonant structures were used to investigate subband spacings and the polaron mass of electrons in these one dimensional systems. This is particularly useful for quantum wires near the quantum limit when traditional methods for the characterization of 1D systems fail due to the low number of occupied subbands. By variation of the electron density in the quantum wire systems a situation can be achieved where a decreasing number of subbands are occupied. It was found that the MPR is strongest in cases where the electron density is too low for classical magnetic depopulation experiments to yield reliable information. We found that the subband spacing in these quantum wire systems increases steeply when the electron density is decreased. Compared to the 2DES, the polaron mass in 1D systems is larger and increases with decreasing 1D electron density, which is caused by stronger electron-LO phonon coupling due to reduced screening.

In systems containing only a few (up to five) ballistic quantum wires, which were prepared by electron beam lithography and wet chemical etching (Fig. 1), additional structures in the magnetoresistance at low magnetic fields could be observed (Fig. 2). Channel resistance peaks with a superimposed fine structure develop at relatively high current densities. They can be explained by the assumption that electrons exiting one quantum wire into the 2DES are magnetically focused into the adjacent wire after specular scattering at the boundary of the etched region forming the spacing between the 1D wires (Fig. 3). This coherent focusing causes interference effects which lead to fine structured peaks in the magnetoresistance. In further experiments the dependence of this effect on temperature and on the length of the quantum wires is investigated. It is expected that the results of forthcoming measurements can be used to determine the phase coherence lengths in quantum wires.

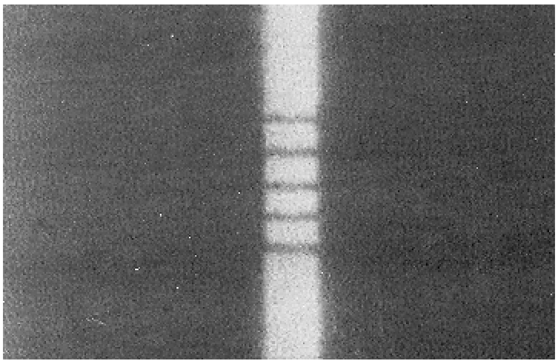

Fig. 1: Five wet chemically etched quantum wires (optical microscope, magnification = 2500x). The quantum wires are 2 μm long. The dark areas to the left and to the right are 2DEG used as 'contacts' to the quantum wires. The annealed contacts to the 2DEG are not shown.

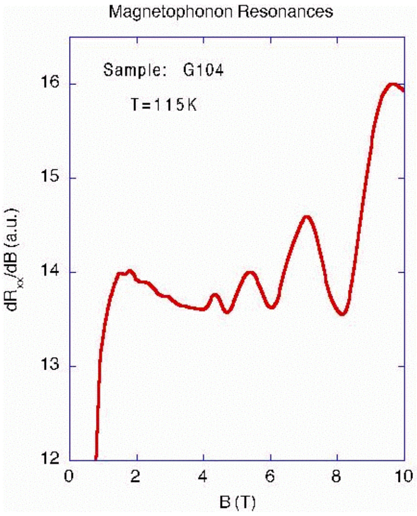

Fig. 2: Magnetophonon resonances at a temperature of 115 K in an array of quantum wires.

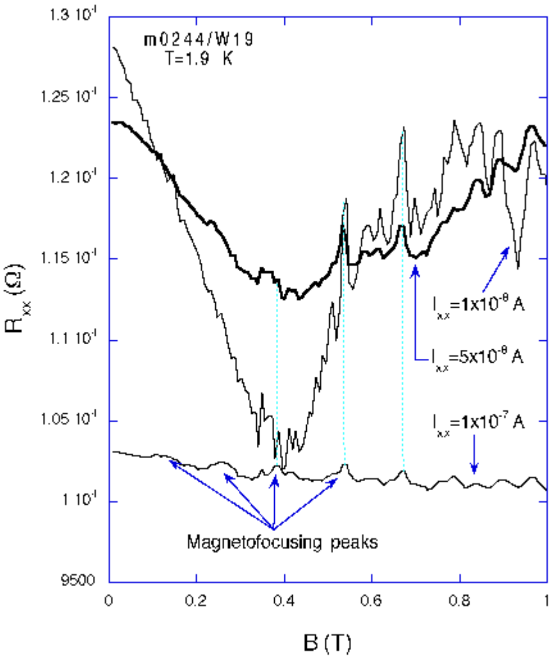

Fig. 3: Additional structures in the magnetoresistance of an array of quantum wires for three different currents (magnetofocusing peaks).

3. High Field Transport on Single Wires

Investigations of high field transport measurements on single wires etched into the 2DEG of standard GaAs/AlGaAs heterostructures a reduction of the channel resistance at high fields was found. It can be attributed to the reduced dimension of the charge carriers due to strongly reduced electron-electron scattering and a grossly changed interaction of electrons and phonons in one dimension [2].

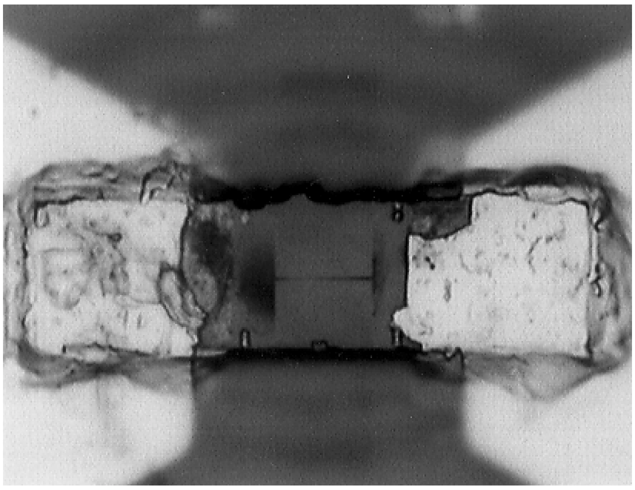

Fig. 4: Single quantum wire 20 µm long (optical microscope). The mesa is 60 µm x 20 µm. The resist mask used to produce the quantum wire by wet chemical etching is clearly distinguished, since the electron beam resist is removed in a later processing step.

4. Fast GaAs Schottky Diodes for THz Applications

Performance of GaAs based Schottky diodes for the THz regime is strongly influenced by the capacity of the Schottky contact and therefore its area. A reduction of the size of the contact pad has been shown to result in very fast diodes suitable for THz applications. A new method for the fabrication of such diodes is being developed. It is based on an air bridged Schottky contact with extremely small capacity. The size of the contact pad is in the range of 100 nm x 100 nm or smaller. The stray capacity of the leads is further reduced by air bridging.

A tri-level PMMA-based electron beam resist system is employed to form one lead of the THz diode. By variation of the exposure dose the lift off behavior of this system can be changed. Regions with higher dose form contacts to the GaAs substrate, whereas lower dose areas lead to bridges remote of the substrate. This can clearly be seen in Fig. 5 showing part of an array of rather large sized Au-air bridges on a GaAs substrate. This test pattern was used during development of the EBL air bridge technology. Further optimization of this process together with standard optical lithography steps is necessary to develop fully functional THz diodes.

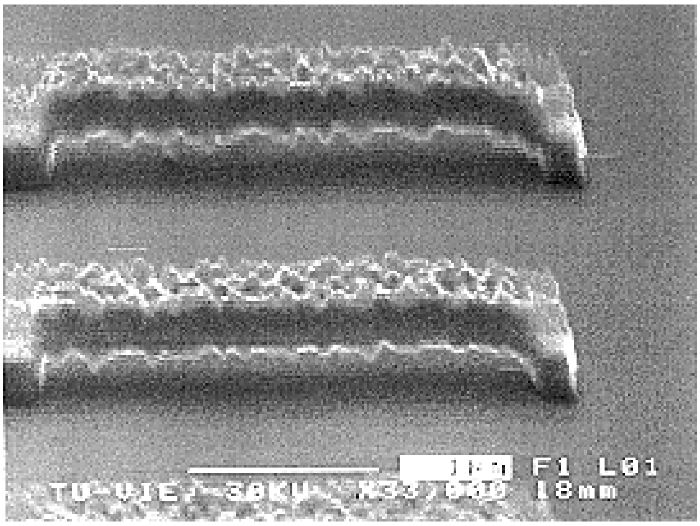

Fig. 5: Two air-bridges made of 100 nm thick gold (electron microscope). It can clearly be seen that the gold, later to be used as Schottky contact for THz diodes, clears the substrate at a distance of about 2 μm. The bridge is about 250 nm high. The size of the contact pads at the right hand side is about 100 nm x 1 μm. For application in a high speed device, further optimization is obviously needed.

5. Fabrication and Optimization of Surface Gratings for Vertical Emitting Laser Diodes

In semiconductor laser technology one is usually faced with the fabrication of very small structures such as gratings with periods varying from 200 – 750 nm used as couplers in DFB/DBR and SME laser diodes.

Effective techniques to fabricate these small structures are laser holography and EBL, since conventional optical lithography techniques are limited in fabricating structures of such small sizes. Obviously, standard optical microscopy can not be employed for the analysis of such small sized structures. Therefore, EB microscopy was used as a vital analysis tool (Figs. 6 and 7). Many repeated steps of photolithography, ion milling and analysis by electron beam microscopy led to optimized surface gratings [3, 4].

5.1 Laser Holography

Laser holography is based on the interference of two laser beams used to expose standard photoresists. The period of the interference pattern depends on the angle between the two incident beams and the laser wavelength and is therefore limited to half of the laser wavelength. In our setup, the angle between the sample and the reflecting mirror is chosen to be 90°, and the distance between the source and the sample holder assembly is very large compared to the laser wavelength, so that the curvature of the interference pattern is practically zero. The laser source is a He-Cd laser operating at 325 nm with 28 mW of output power. The grating period can be calculated as $\Lambda_g = \frac{\lambda}{2\sin\theta}$, where Λ_g and λ are grating period and laser wavelength and θ is the incident angle.

5.2 Photo Resists and Fabrication Process

Photo resists used to fabricate surface gratings must satisfy the following conditions in order to fulfill the requirements for successful grating fabrication:

- Capability of submicron resolution with high contrast;
- Suitability for broadband and monochromatic exposure;
- Good adhesion for etching;
- High thermal stability;
- Wide process latitude.

Unfortunately, standard photo resists are not optimized for requirements such as stated above.

5.2.1 Positive Resist AZ 6615

In order to achieve a reasonable grating depth by wet chemical etching the resist must reveal steep edges. Positive resist characteristics make it possible to fabricate such structures. The optimized process used for fabrication of 425 nm surface gratings is given in the following:

1. HCl dip; HCl dip serves to remove organic compounds from the sample’s surface in order to achieve a better adhesion to the surface.
1. Spin coating the sample with AZ 6615 resist for 35 s at 10000 rpm. This corresponds to a resist thickness of 1.2µm.
1. Pre-exposure bake for 45 s at 100 °C.
1. Exposure by laser for 45 s.
1. Develop in AZ 726 MIF for 30 s and rinse thoroughly.
1. Post-exposure bake for 60 s at 120 °C.

1. O_2-Plasma etching for 3 minutes with 100 W power. This removes the rest of resist from the sample's surface and helps to achieve a homogeneous etched surface.
1. Wet chemical etching by a solution of AZ 726 MIF, H_2O, H_2O_2 and tenside

The etching rate is about 20 nm/min and is fully reproducible.

To fabricate gratings with other periods and duty ratios one should change the exposure duration and development time, i.e., longer exposures decrease the bridge to trench ratio. For smaller grating periods the exposure time should be increased to achieve a one to one duty ratio. The developing time should be kept minimum provided the exposed surface is completely developed. Figure 6 shows a grating of period 425 nm fabricated by positive photo resist.

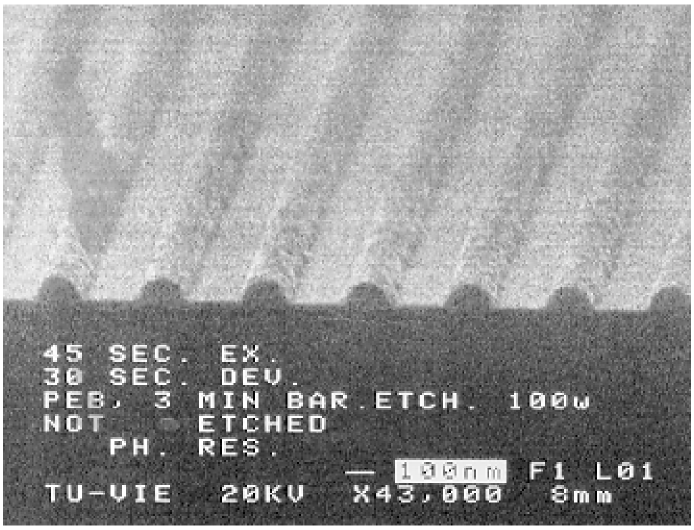

Fig. 6: Photoresist grating analyzed by electron beam microscopy. The grating consists of positive photo resist, later used for wet chemical etching.

5.2.2 *Image Reversal Resist AZ 5206*

The image reversal resist AZ 5206 is suitable for fabrication of gratings with periods under 500 nm and subsequent lift off processes. The side walls of this resist form undercut edges and are therefore not suitable for wet chemical etching. On the other hand wet chemical etching is known not to be appropriate for such small structures, since the etchant cannot reach the substrate due to surface tension. The etching mechanism used with this resist is ion milling. A grating period of 425 nm with steep side walls is achieved with the optimized parameters following:

1. HCl dip.
2. Spin coating with diluted resist AZ 5206 (1:1 with AZ 1500) for 35 s at 10000 rpm. This corresponds to a resist thickness of about 500 nm.
3. Pre-exposure bake for 60 s at 100°C.
4. Exposure by laser for 530 s.
5. Post-exposure bake for 60 s at 130°C.

6. Flood exposure for 10 s with ultraviolet light.
7. Development for 25 s with AZ 726 MIF.
8. Post bake for 45 s at 140°C.
9. Ion milling etching for 10 minutes at 20° incidence. This corresponds to an etched depth of 110 nm with steep side walls.

The fabrication process is very sensitive to exposure time, post-exposure bake, flood exposure and developing time. To produce smaller periods with image reversal resist the exposure time should be kept shorter and the flood exposure must be longer to achieve a one to one duty ratio. Figure 7 shows an etched grating processed as described above.

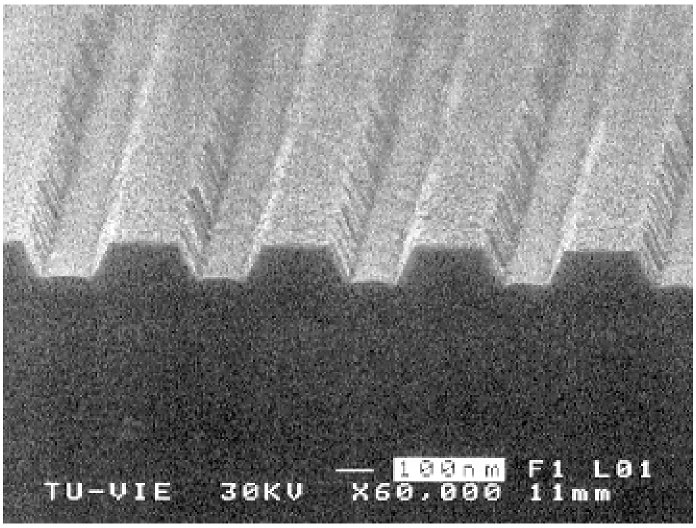

Fig. 7: Surface grating etched by ion milling.

6. Conclusion

EBL was used to produce arrays of quantum wires for transport measurements showing interference effects between carriers emerging out of adjacent wires. Single wires fabricated by EBL were used for high field measurements. Technology for air bridged Schottky contacts to be used in THz diodes has been developed. Surface gratings for emitting laser diodes have been optimized using parts of the EBL system.

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Presentations

1. M. Hauser, G. Strasser: “Elektronenstrahllithographie von niedrigdimensionalen GaAs/AlGaAs Heterostrukturen”, oral paper *at Fortbildungsseminar: Grundlagen und Technologie elektronischer Bauelemente*, Großarl 1995, ISBN 3-901578-01-3

Diploma Theses

1. E. Zotl: “Elektronenstrahllithographie für THz Bauelemente und Antennenstrukturen”, in progress.

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Microelectronics Technology — Cleanroom Linz

Microstructure Research: Cleanroom Linz

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Various activities taking place in the cleanroom are described, such as MBE growth of group IV heterostructures, of II-VI and IV-VI compounds, surface analysis by UHV-STM and Auger spectroscopy, as well as lateral patterning by photolithography and reactive ion etching for fabrication of infrared detectors, quantum wires and dots.

1. MBE of Si/$Si_{1-x}Ge_x$ and of Si/$Si_{1-y}C_y$ Heterostructures

In the last couple of years intensive studies on Si/SiGe heterostructures and quantum wells have been reported by several groups. Apart from the investigation of fundamental physical properties of Si-based heterostructures as opposed to III-V compounds, the driving force behind these studies was the hope for an improvement of devices based on Si/SiGe in comparison to conventional Si homostructures. Indeed, Si/SiGe heterobipolar transistors with high-frequency properties superior to conventional Si devices were fabricated as well as Si/SiGe based MODFET's.

Recently another class of Si based heterostructures, namely Si/$Si_{1-y}C_y$, has attracted a lot of interest because it can extend the possibilities to other applications than offered by Si/SiGe. In 1995, in the clean room of the semiconductor physics group at Linz a RIBER SIVA 45 MBE has been installed for the growth of Si/Ge/C heterostructures. It is equipped with three e-beam evaporators for Si, Ge, and C. For n-and p-doping effusion cells for antimony and boron are available. The beam fluxes are monitored by a Hiden quadrupole mass spectrometer, which is also used for a feedback regulation of the evaporator. Compared to a carbon filament source, the e-beam evaporator for carbon has a much higher capacity and in principle the possibility to use higher C-fluxes.

So far, Si/SiGe heterostructures and quantum well structures were grown with this MBE, as well as Si/$Si_{1-y}C_y$ layers, MQW's and superlattices. Also strain compensated $Si_{1-x}Ge_x$/$Si_{1-y}C_y$ superlattices were fabricated and structurally investigated. In particular, silicon/carbon/silicon superlattices were grown, with the C-layers confined to about one monolayer, but with extremely high carbon contents. The structural data of these superlattices as obtained from high-resolution X-Ray diffraction, transmission electron microscopy, and reciprocal space mapping indicate a satisfactory quality, not much inferior to pseudomorphic Si/SiGe superlattices.

The electrical properties of the $Si_{1-y}C_y$ layers are dominated so far by a background electron concentration of 4×10^{16} cm^{-3} with mobilities comparable to those of similarly doped Si. In the epilayers no evidence was found for a mobility reduction due to the strong lattice deformation around the C-lattice sites.

At the moment, Si-shields are inserted into the MBE system in order to reduce the background doping substantially, a requirement for achieving high carrier mobilities.

A preliminary attempt was made to grow modulation doped Si/ $Si_{1-y}C_y$ heterostructures. On top of a (001) Si substrate, after depositing a 1 µm thick Si buffer layer (undoped), a 17 nm thick $Si_{0.98}C_{0.02}$ layer was deposited followed by a 12 nm Si spacer-layer, a 17 nm thick Sb doped Si layer, and finally a 45 nm Si cap layer. The exact thicknesses were determined from a simulation of the dynamic x-ray diffraction data of this heterostructure. The main findings were: compared to bulk Si, the 2D electron mobilities in the $Si_{1-y}C_y$ layer were clearly enhanced. The conduction band of $Si_{1-y}C_y$ is indeed lowered with respect to that of Si, an effect that is mainly due to the biaxial tensile strain in the $Si_{1-y}C_y$ layer. The mobilities in the 2D channel are, however, still limited by residual background impurities.

Selected references: [1], [2].

2. Surface Modifications in Strained-Layer Heteroepitaxy Studied by UHV Scanning Tunneling Microscopy

The growth of lattice-mismatched semiconductor heterostructures is of considerable importance for advanced microelectronic devices. Since the performance of these devices is strongly affected by structural defects such as misfit dislocations, the understanding and the control of strain relaxation are a critical issue for lattice mismatched heteroepitaxy. We have recently shown that the formation of misfit dislocations at the heterointerfaces leads to atomic scale changes of the surface structure of the epilayer, which are directly detectable by UHV scanning tunneling microscopy (STM) or even by atomic force microscopy (AFM). In the previous year we have shown experimentally that the formation of the interfacial dislocations produces atomic glide steps on the epitaxial surface. Therefore, the onset of strain relaxation as well as the degree of strain relaxation can be determined by STM.

In this year we have performed a quantitative scanning tunneling microscopy study of surface deformations induced by misfit dislocations formed during strained heteroepitaxy of the antiferromagnetic semiconductor EuTe on PbTe (111). Both compounds crystallize in the rocksalt structure with a lattice mismatch of 2.1%. The EuTe layer was grown by MBE on a PbTe buffer which was deposited on (111) BaF_2 substrates. After interrupting the growth the samples were transferred to an attached UHV chamber, where the STM investigations were carried out.

According to the Matthews-Blakeslee mechanism, pre-existing threading dislocations form misfit segments at the EuTe/PbTe interface above the critical layer thickness. We observe pronounced surface deformations caused by single dislocations and dislocation reactions. The observed surface deformations exhibit a characteristic dependence on the orientation of the Burgers vector, which is in excellent quantitative agreement with calculations based on elasticity theory, taking into account the relaxation of the local strain fields due to the existence of a free surface. The use of the STM allows also for a study of the misfit dislocation reactions, even for dislocations located many monolayers below the epitaxial surface.

From our calculations we find that at the critical layer thickness about half of the total strain energy is locally relaxed by misfit dislocations. We have found direct experimental evidence that due to this local reduction of the strain energy, ridge-like structures are formed by stress-driven surface diffusion, which is a direct experimental evidence for a local dislocation-induced enhancement of the epitaxial growth.

Selected references: [3] – [9].

3. Fabrication of Si/SiGe Quantum Well Infrared Photodetectors

Detector elements were fabricated from MBE grown pseudomorphic Si/SiGe MQW structures by photolithography, reactive ion etching and metal-evaporation/lift-off techniques.

In 1995 the reactive ion etching facility in the clean room of the semiconductor physics building was modified to enable the use of gases like SF_6 and CF_4 for the reactive ion etching of the Si/SiGe structures.

A systematic study on the influence of the etch gas composition, its partial pressure (10 – 50 mbar), the mass flow (10 – 15 SCCM), the rf power (30 – 200 W) on the etching rates as well as on the side wall steepness of Si/SiGe microstructures has been made.

Concerning the side-wall steepness we observed a strong dependence on gas composition for similar plasma parameters. The admixture of oxygen to SF_6 (mass flow ratio SF_6:O_2 5:1) improves the side-wall steepness considerably.

The MQW detector structures have typically lateral dimensions of 100 μm x 100 μm. The ratio of the Si-barrier width (20 – 30 nm) to the $Si_{1-x}Ge_x$ well width (3 nm, with a Ge content $x = 0.3$) is so small that the difference between the etching rates for Si and SiGe is not relevant for the fabrication of these quantum well detectors.

Rather more important is the reproducibility of the etching depth (total depth: about 500 nm) within an accuracy of about 20 nm, which is required for contacting the lower buried highly p-doped bottom contact layer, which has a total thickness of 100 nm.

Selected references: [10], [11].

4. Damage in Reactive Ion Etched Nanostructures

Elastic strain present in reactive ion etched quantum wires and quantum dot structures as well as the side wall damage was investigated by high-resolution x-ray diffraction. From measurements of both the coherent as well as the diffusely scattered radiation not only information on the strain status of these nanostructures but also on the random elastic strain fields can be obtained.

We have investigated both III-V compound nanostructures (GaAs/AlAs) as well as II-VI compound structures (CdTe/MnTe, CdTe/CdZnTe, etc.). For the III-V compounds as etching gases $SiCl_4$ and O_2 were used for magnetically confined plasma etching. The II-VI compounds were reactively ion etched with a mixture of CH_4 and H_2.

The general findings are as follows: due to the patterning process, in quantum wires an elastic relaxation takes place. In addition, the reactive ion process induces an expansion of the mean lattice constant along the growth direction, both for III-V as well as for the II-VI compound heterostructures. These facts can be tentatively explained by the incorporation of chemical species into the sidewalls during the reactive ion etching process. In the II-VI nanostructures we found that annealing after the fabrication process reduces this additional expansion along the growth direction. In the latter case we attribute this behavior to the incorporation of H_2 during the etching process and its outdiffusion during annealing.

The diffuse scattering is caused by random strains due to defects introduced by the fabrication process. From detailed simulations of the high resolution x-ray data it became apparent that the random strains, which cause the diffuse scattering (accompanying the coherent one), are caused by the fabrication process itself. In order to produce steep sidewalls, certain flow rates of e.g. $SiCl_4$ and O_2 (13.5 SCCM and 1.5 SCCM, respectively, at an operating pressure of 0.5 mTorr), microwave and r.f. powers (55 W and 35 W) turned out to be necessary. However, these etching conditions induce strain fields that extend nearly throughout the entire volume of dot-like structures with diameters of 300 nm and heights of about 2000 nm, as evidenced from the experimental data.

The x-ray diffraction analysis also reveals that after the reactive ion etching the nanostructures have a crystalline inner core the diameter of which is about 20 – 30% smaller than the apparent one as obtained from scanning electron microscopy. The outer layer is heavily distorted after the etching process, almost amorphous, which explains nicely the often reported discrepancy between, e.g., the photoluminescence yield of nanostructures and expectations based on the assumption of their geometrical shape.

Selected references: [12] – [15].

5. Fabrication and Optical Properties of CdTe/CdZnTe and ZnSe/ZnCdSe Quantum Wires and Dots by Nanolithography

With the advent of blue-green heterostructure lasers based on II-VI compounds it has become important to investigate optical properties of quantum wire and dot structures too, in order to evaluate attractive properties like a possible increase of oscillator strength and consequently lower laser thresholds in the nanostructures.

However, it is well known that the dry etching fabrication process induces defects, which seem to be less severe in II-VI compounds as compared to III-V compounds. In collaboration with two French groups in Grenoble and in Bagneux we have fabricated CdTe/CdZnTe and ZnSe/ZnCdSe wire and dot structures that were defined by electron beam lithography in France and etched by reactive ion etching (CH_4 + H_2) in Linz. Typical scanning electron microscopy images of these etched structures are shown in the relevant publications as cited below.

High density periodic patterns were written by e-beam nanolithography in a 150 nm thick polymethylmethacrylate resist layer. Arrays of 40x40 μm^2 with wires and dots of different sizes were obtained. After deposition of a 40 nm titanium layer, a lift-off process was used to produce a metallic patterned mask on top of the sample. This pattern was transferred by reactive ion etching into the QW heterostructures.

A CH_4/H_2 gas mixture (1:8 volume ratio) at a pressure of 15 mTorr was used with a RF power of 180 W. The shape of the walls depends strongly on the II-VI material. Whereas for pure CdTe strong etching under the mask is observed, this is not the case for the selenide based QW structures.

The photoluminescence studies made on these structures include measurements of the PL efficiency and time resolved spectroscopy and reflect the crucial role of a damage layer induced by the etching process. This allows also to give quantitative data on the luminescence degradation in the smallest dry etched nanostructures.

The ZnSe based structures exhibit photoluminescence emission down to the smallest widths of 40 nm and 60 nm, respectively. The wider wires and dots of about 200 to 1000 nm show even an increase of the normalized photoluminescence intensity for the emission line in CdZnSe/ZnSe as compared to the unetched QW structure. With decreasing lateral size, the nanostructures first exhibit a red-shift of the emission line, which is attributed to the before-mentioned strain relaxation process. Further size reduction causes an apparent blue shift at about 70 nm lateral width. However, this width is still too large so that this spectral shift of the luminescence cannot be attributed to size quantization, which should become significant for less than 40 nm.

Selected references: [16] – [22].

6. In-situ Auger Electron Spectroscopy of MBE Grown II-VI Compound Epilayers

The GMe has supported an UHV tunnel between the MBE systems in the clean room in Linz. This tunnel has now been used for transferring samples from the MBE to a newly acquired Auger electron spectrometer, without the necessity for breaking the UHV. Thus nearly *in situ* investigations of near surface and buried layer regions can be made of MBE grown II-VI epilayers.

This Auger electron spectrometer has been used for the investigation of (001) oriented ZnS layers deposited on Silicon substrates, and for the structural and elemental analysis of ZnSe, CdSe, ZnTe and CdTe.

A particular advantage of the Auger electron spectrometer, namely the investigation of impurities on the surface of the MBE grown films (with the exception of oxygen and helium) has been used for surface related studies of binary and ternary II-VI compounds. With the scanning Auger spectrometer, a lateral resolution in the micrometer range can be achieved, which is advantageous for the detection of surface clusters as well as for island formation.

Ar-ion sputtering in combination with AES yields information on depth profiles of various elements, which is required for the analysis of II-VI compound multilayers.

The analysis of the line-shape of the AES spectra gives information on the chemical bonding of the analyzed atoms.

The Auger electron spectrometer has been used in particular for the investigation of the reactive ion etch process of II-VI compounds for which a mixture of CH_4 and H_2 is commonly used. The carbon and oxygen content at the etching front have been analyzed systematically. It turned out that carbon or oxygen penetration into the II-VI layers is minimized if the gas mixture for the reactive ion etching CH_4 and H_2 has a ratio of 1:6 to 1:8. This information is quite useful for minimizing the defect incorporation during the etching process.

Selected references: [23] – [26].

Acknowledgments

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Project Information

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Schäffler	Friedrich	Professor	
Helm	Manfred	Univ.-Doz.	
Brunthaler	Gerhard	Ph.D.	
Faschinger	Wolfgang	Univ.-Doz.	until 30 August 1995
Fromherz	Thomas	postdoc	
Darhuber	Anton A.	dissertation	
Kruck	Peter	dissertation	
Penn	Christian	dissertation	
Springholz	Gunther	postdoc	
Sitter	Helmut	Univ.-Doz.	
Wirthl	Edwin	dissertation	
Stifter	David	dissertation	
Pichler	Christian	diploma thesis	
Ueta	Yukio	dissertation	
Wirtl	Elisabeth	technician	
Rabeder	Klaus	technician	
Schmid	Michael	diploma thesis	
Kainz	Ursula	technician	
Stangl	Julian	dissertation	
Straub	Hubert	dissertation	50%GMe funding
Zerlauth	Stefan	dissertation	

Publications in Reviewed Journals

1. A.A. Darhuber, G. Bauer, P.D. Wang, Y.P. Song, C.M. Sotomayor Torres, M.C. Holland: "Determination of the strain status of GaAs/AlAs quantum wires and quantum dots", *Mat. Res. Soc. Symp. Proc.* 358, 975 (1995).

2. A.A. Darhuber, E. Koppensteiner, G. Bauer, P.D. Wang, Y.P. Song, C.M. Sotomayor Torres, M.C. Holland: “X-ray reciprocal space-mapping of GaAs/AlAs quantum wires and quantum dots”, *Appl. Phys. Lett.* 66, 947 (1995).
3. A.A. Darhuber, H. Straub, S. Ferreira, W. Faschinger, E. Koppensteiner, G. Brunthaler, G. Bauer: “Structural investigation of II-VI compound semiconductor quantum wires using triple axis x-ray diffractometry”, *J. Crystal Growth* 150, 775 (1995).
4. A.A. Darhuber, H. Straub, S. Ferreira, W. Faschinger, H. Sitter, E. Koppensteiner, G. Brunthaler, G. Bauer: “Fabrication and x-ray diffractometry investigation of CdTe/MnTe multiple quantum wires”, European Workshop on II-VI Semiconductors, Linz, Austria 1994; *Materials Science Forum* 182 – 184, 423 (1995), Trans Tech Publications, Switzerland.
5. A.A. Darhuber, E. Koppensteiner, G. Bauer, P.D. Wang, Y.P. Song, C.M. Sotomayor Torres, M.C. Holland: “Structural investigations of GaAs/AlAs quantum wires and quantum dots by x-ray reciprocal space mapping”, *Phys. D: Appl. Phys.* 28, A 195 (1995).
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7. W. Faschinger: “Doping of wide gap II-VI compounds”, *J. Crystal Growth* 146, 80 (1995).
8. W. Faschinger: “Fundamental doping limits in wide gap II-VI compounds”, *Semiconductor Heteroepitaxy: Growth, Characterization and Device Applications*, eds.: B. Gil, R.-L. Aulombard. World Scientific Publishing, Singapore 1995, p. 17.
9. W. Faschinger, S. Ferreira, H. Sitter: “Band structure engineering and doping of wide gap II-VI superlattices”, *Appl. Phys. Lett.* 66, 2516 (1995).
10. W. Faschinger, S. Zerlauth, G. Bauer, L. Palmetshofer: “Electrical properties of $Si_{1-x}C_x$ alloys and modulation doped $Si/Si_{1-x}C_x/Si$ structures”, *Appl. Phys. Lett.* 67, 3933 (1995).
11. W. Faschinger, G. Brunthaler, R. Krump, A. Darhuber, S. Ferreira, H. Sitter: “MBE growth of heterostructures and superlattices containing MgTe”, European Workshop on II-VI semiconductors, Linz, Austria 1994; *Materials Science Forum Vols*. 182 – 184, 407 (1995), Trans Tech Publications, Switzerland.
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22. G. Springholz: “Molecular beam epitaxy and structural properties of PbTe/EuTe short period superlattices”, *Materials Science Forum* 182 – 184, 573 (1995), Trans Tech Publications, Switzerland.

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24. H. Straub, G. Brunthaler, W. Faschinger, G. Bauer, C. Gourgon, L.S. Dang, H. Mariette, C. Vieu: “Photoluminescence of CdZnTe and CdZnSe quantum well wires fabricated by reactive ion etching”, *Materials Science Forum* 182 – 184, 179 (1995), Trans Tech Publications, Switzerland.

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39. S. Ferreira, H. Sitter, R. Krump, W. Faschinger, G. Brunthaler: “Room temperature blue electroluminescence from the ZnMgCdSe quaternary system”, Submitted to *J. Crystal Growth*.
40. W. Hilber, M. Helm, F.M. Peeters, K. Alavi, R.N. Pathak: “Study of the impurity band and the magnetic field induced metal-insulator transition in a doped GaAs/ AlGaAs superlattice”, *Phys. Rev. B*, in print.
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RHEED", *Semiconductor Heteroepitaxy: Growth, Characterization and Device Application*, Ed. B. Gil and R.L. Aulombard, World Scientific, Singapore 1995, p. 222.

43. G. Springholz, G. Bauer: "A scanning tunneling microscopy study of surface modifications induced by misfit dislocation formation in strained layer hetereoepitaxy", *Applied Surface Science*, submitted.
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45. G. Springholz, N. Frank, G. Bauer: "Surface modifications in strained-layer heteroepitaxy studied by UHV-scanning tunneling microscopy", *Solid State Electronics*, in print.
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52. T. Fromherz, P. Kruck, M. Helm, G. Bauer, J.F. Nützel, G. Abstreiter: "Polarization dependence of intersubband absorption and photoconductivity in p-type SiGe quantum wells", *Superlattices and Microstructures*, submitted.
53. G. Bauer, A. Darhuber, V. Holy: "Structural characterization of reactive ion etched semiconductor nanostructures using x-ray reciprocal space mapping", *Mat. Res. Soc. Symp. Proc.*, in print.
54. G. Springholz, G. Bauer, V. Holy: "Direct observation of stress driven surface diffusion due to localized strain fields of misfit dislocations in heteroepitaxy", *Surface Science*, in print.
55. M. Shima, L. Salamanca-Riba, G. Springholz, G. Bauer: "Double periodicity formation in EuTe/PbTe superlattices", *Mat. Res. Soc. Symp. Proc.*, in print.
56. E. Wirthl, H. Sitter, P. Bauer: "Monocristalline (100)-oriented ZnS Layers grown on Si by Molecular Beam Epitaxy", *J. Cryst. Growth* 146, 404 (1995).
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58. E. Wirthl, H. Straub, H. Sitter, G. Brunthaler, M. Schmid, D. Stifter, P. Bauer: “AES Investigations on Plasma-etched II-VI Binary Compounds”*, Proc. Int. Symp. on Blue Laser and Light Emitting Diodes*, Chiba, Japan 1996, Ohmsha Press, in print.
59. T. Fromherz, P. Kruck, M. Helm, G. Bauer, J.F. Nützel, G. Abstreiter: “TM and TE polarized intersubband absorption and photoconductivity in p-typ SiGe quantum wells”, *Applied Physics Letters*, submitted.

Presentations

Invited Talks

1. G. Bauer, A.A. Darhuber, V. Holy: “Structural characterization of reactive ion etched semiconductor nanostructures using x-ray reciprocal space mapping”, Materials Research Society 1995 Fall Meeting, Boston, MA, 27.Nov. – 1.Dez. 1995.
2. T. Fromherz, P. Kruck, M. Helm, G. Bauer, J.F. Nützel, G. Abstreiter: “Polarization dependence of intersubband absorption and photoconductivity in p-type SiGe quantum wells”, International Conference on Intersubband Transitions in Quantum Wells: Physics and Applications, Oct.23 – 26, 1995, Kibbutz Ginosar (Sea of Galilee), Israel.
3. G. Bauer, J.H. Li, V. Holy: “X-ray reciprocal space mapping: new developments for precise information on strain in heteroepitaxy”, 2nd Symposium on Physics in Material Science, Jaszowiec, Polen, 17. – 22. Sept. 1995.
4. W. Faschinger: “Fundamental doping limits in wide gap II-VI compounds”, 7th International Conference on II-VI Compounds and Devices, Edinburgh, August 13 – 18, 1995.
5. G. Brunthaler, G. Stöger, A. Prinz, C. Penn, G. Bauer: “Beeinflussung der elektronischen Eigenschaften von Halbleiterheterostrukturen durch störstelleninduzierte Unordnung”, Fachausschuß für Festkörperphysik der Jahrestagung der ÖPG, Leoben, Sept. 1995.
6. M. Helm: “Infrarotspektroskopie von Löchern in Si/SiGe Quantum Wells / Intersubbandrelaxation in GaAs/AlGaAs Quantum Wells”, Universität Marburg, 28.11.1995.
7. M. Helm, W. Hilber, P. Kruck, T. Fromherz, M. Seto, G. Bauer: “Intersubband-übergänge in Halbleiter-Quantentöpfen und -Übergittern”, Fachausschuß für Festkörperphysik, Jahrestagung der ÖPG, Leoben, Sept. 1995.
8. G. Bauer, N. Frank, G. Springholz: “Misfit dislocation formation in heteroepitaxy observed by UHV-STM”, Workshop on interface structure and electronic transport properties of heterostructures, University of Minnesota, Minneapolis, USA, 4. – 6. Mai 1995.
9. G. Bauer, J.H. Li, E. Koppensteiner: “X-ray reciprocal space mapping of Si/SiGe heterostructures”, European Materials Research Society, Strasbourg, France, 22. – 26. Mai 1995.
10. G. Bauer: “UHV-STM investigations of EuTe epitaxial layers”, Physik-Kolloquium, Masaryk Universität Brünn, Tschechien, 7. Juni 1995.

11. G. Bauer: “Semimagnetic semiconductor heterostructures and superlattices”, DPG Frühjahrstagung Berlin, 20. – 24. März 1995.
12. A. Darhuber, V. Holy, G. Bauer: “Quantitative analysis of elastic strains in GaAs/AlAs quantum dots”, 3rd International Symposium on New Phenomena in Mesoscopic Structures, Mauii, Hawaii, 4. – 8. Dez. 1995.
13. T. Fromherz, J.H. Li, P. Kruck, M. Helm, G. Bauer: “Intersubband spectroscopy on Si/SiGe multi quantum wells and their structural characterization”, Heterostructures de semiconducteurs IV-VI, Orsay, 26. – 27. Okt. 1995.
14. G. Bauer, A.A. Darhuber, V. Holy, J.H. Li: “X-ray diffraction on two-, one- and zero-dimensional structures”, Heterostructures in Science and Technology (W.C. Röntgen 100 year anniversary), Universität Würzburg, 13. – 17. März 1995.
15. G. Springholz, N. Frank, G. Bauer: “Surface modifications due to strain relaxation in lattice-mismatched heteroepitaxy”, Frühjahrstagung der Deutschen Physikalischen Gesellschaft, Berlin, 20. – 24. März 1995.

Conference Presentations

1. H. Straub, G. Brunthaler, W. Faschinger, G. Bauer, C. Vieu: “Photoluminescence of CdZnSe/ZnSe quantum well structures fabricated by reactive ion etching”, 7th International Conference on II-VI Compounds and Devices, Edinburgh, UK 1995.
2. J.H. Li, V. Holy, G. Bauer, M. Hohnisch, H.-J. Herzog, F. Schäffler: “Strain relaxation and misfit dislocations in compositionally graded Si1-xGex layers on Si (001)”, E-MRS Strasbourg 1995.
3. C. Pichler, G. Springholz, G. Bauer: “A comparison of experimental resolution for critical thickness determination by UHV-STM, x-ray diffraction and in situ RHEED”, International Conference on Semiconductor Heteroepitaxy, Montpellier, France 1995.
4. G. Springholz, N. Frank, G. Bauer: “Surface modifications in strained-layer heteroepitaxy studied by UHV-scanning tunneling microscopy”, 7th International Conference on Modulated semiconductor Structures, Madrid, Spain, July 10 – 14, 1995.
5. S. Ferreira, H. Sitter, R. Krump, W. Faschinger, G. Brunthaler: “Room temperature blue electroluminescence from the ZnMgCdSe quaternary system”, 7th International Conference on II-VI Compounds and Devices, Edinburgh, August 13 – 18, 1995.
6. G. Brunthaler, H. Straub, W. Faschinger, G. Bauer: “Herstellung von II-VI Quantendrähten mit optischer Emission im blauen Spektralbereich”, Seminar Grundlagen und Technologie elektronischer Bauelemente, 5. – 8.4.1995, Großarl, Österreich.
7. F. Geist, H. Pascher, G. Springholz, G. Bauer: “Band and exchange parameters of Pb1-xEuxTe”, 7th International Conference on Narrow Gap Semiconductors, Santa Fe, New Mexico, Jan. 8 – 12, 1995.
8. H. Mariette, C. Gourgon, L.S. Dang, J. Cibert, C. Vieu, G. Brunthaler, H. Straub, W. Faschinger, N. Pelekanos, W.W. Rühle: “Fabrication and optical properties of CdTe/CdZnTe quantum wires and dots processed by nanolithography”, International Conference on Semiconductor Heterostructures, Montpellier 1995.

9. G. Springholz, G. Bauer: “Study of misfit-dislocation formation in strained-layer heteroepitaxy using UHV-scanning tunneling microscopy”, 7th International Conference on Modulated Semiconductor Structures, Madrid, Spain, July 10 – 14, 1995.
10. G. Springholz, G. Bauer: “A scanning tunnelling microscopy study of surface modifications induced by misfit dislocation formation in strained layer heteroepitaxy”, Intenational Conference on the Formation of Semiconductor Interfaces, Princeton, USA, 1995.
11. G. Springholz: “Surface deformation induced by local strain fields of misfit dislocations studied by UHV-scanning tunnelling microscopy”, Workshop on Molecular Beam Epitaxy, Max-Planck-Institut für Festkörperforschung, Stuttgart, 8. – 11. Okt. 1995.
12. E. Wirthl, H. Straub, M. Schmid, H. Sitter, G. Brunthaler, P. Bauer: “AES-analysis of plasma-etched ZnSe”, 7th International Conference on II-VI Compounds and Devices, Edinburgh, UK 1995.
13. G. Springholz, G. Bauer: “A scanning tunnelling microscopy study of surface modifications induced by misfit dislocation formation in strained layer heteroepitaxy”, Intenational Conference on the Formation of Semiconductor Interfaces, Princeton, USA 1995.
14. G. Springholz: “Surface deformation induced by local strain fields of misfit dislocations studied by UHV-scanning tunnelling microscopy”, Workshop on Molecular Beam Epitaxy, Max-Planck-Institut für Festkörperforschung, Stuttgart, 8. – 11. Okt. 1995.
15. E. Wirthl, H. Straub, M. Schmid, H. Sitter, G. Brunthaler, P. Bauer: “AES-analysis of plasma-etched ZnSe”, 7th International Conference on II-VI Compounds and Devices, Edinburgh, UK 1995.
16. W. Heiss, E. Gornik, C.R. Pidgeon, B.N. Murdin, C.J.G.M. Langerak, M. Helm, H. Hertle, F. Schäffler: “Intersubband lifetimes in Si/SiGe and GaAs/AlGaAs quantum wells”, 7th International Conference on Modulated Semiconductor Structures, Madrid, Spain, July 1995.
17. A.A. Darhuber, G. Bauer, P.D. Wang, Y.P. Song, C.M. Sotomayor Torres, M.C. Holland: “Elastic strains in GaAs/AlAs quantum dots studied by high-resolution x-ray diffraction”, 7th International Conference on Modulated semiconductor Structures, Madrid, Spain, July 10 – 14, 1995.
18. W. Faschinger: “Doping and Compensation in Wide Gap II-VI Semiconductors”, International Conference on Semiconductor Heteroepitaxy, Montpellier 1995.
19. H. Straub, G. Brunthaler, W. Faschinger, G. Bauer, C. Gourgon, LeSi Dang, H. Mariette, C. Vieu: “Photoluminescence of CdZnSe quantum well wire structures fabricated by reactive ion etching”; 7th International Conference on II-VI Compounds and Devices, Edinburgh, August 13 – 18, 1995.
20. E. Wirthl, M. Schmid, D. Stifter, H. Sitter, P. Bauer: “Auger Investigations on II-VI Ternary and Mulitnary Compounds”, 10th Int. Conf. on Ternary and Multinary Compounds, Stuttgart 1995.

21. E. Wirthl, H. Straub, H. Sitter, G. Brunthaler, M. Schmid, D. Stifter, P. Bauer: “AES Investigations on Plasma-etched II-VI Binary Compounds”, Int. Symposium on Blue Laser and Light Emitting Diodes, Chiba, Japan 1996.
22. E. Wirthl, H. Sitter, P. Bauer: “Auger-Elektronenspektroskopie an II-VI-Verbindungshalbleitern”, Fortbildungsseminar der GMe in Großarl

Doctor’s Theses

1. G. Stöger, Quantum interference effects, hot electrons and metal insulator transition in Si/SiGe heterostructures and superlattices, Universität Linz, 1995.
2. E. Wirthl, Quantitative Auger-Analyse an binären und ternären II-VI Verbindungshalbleitern, Universität Linz, 1995.

Habilitations

1. Wolfgang Faschinger, Molekularstrahlepitaxie von II-VI Verbindungen mit großer Energielücke, Universität Linz, 1995.

Cooperations

1. Walter Schottky Institut, TU München, Garching
2. Nanoelectronics Research Center, Glasgow, Scotland
3. Institut für Festkörperelektronik, TU Wien
4. Experimentalphysik, Universität Bayreuth, Deutschland
5. Institute of Physics, Polish Academy of Sciences, Warsaw
6. Department of Physics, Heriot Watt University, Edinburgh, Scotland
7. ESRF, Grenoble, France
8. CEA-CNRS Grenoble, France
9. NIST-Reactor Radiation Division, Gaithersburg, MD, USA
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11. Department of Physics, Massachusetts Institute of Technology, Cambridge, MA, USA
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13. University of Warwick, Coventry, England
14. Fraunhofer Institut, Freiburg, Deutschland
15. IBM Watson Research Center, Yorktown Heights, USA
16. Daimler Benz Laboratorien Ulm, Deutschland
17. Fachbereich Physik, Universität Paderborn, Deutschland

Si/$Si_{1-x}Ge_x$ and Si/$Si_{1-y}C_y$ Heterostructures and Superlattices: X-Ray Diffractometry, Electron Beam Lithography, and Luminescence

G. Bauer, G. Brunthaler, A.A. Darhuber, W. Faschinger, Th. Fromherz, M. Helm, P. Kruck, Ch. Penn, F. Schäffler, J. Stangl, H. Straub, St. Zerlauth

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The molecular beam epitaxy of Si/SiGe, Si/$Si_{1-y}C_y$, and SiGe/$Si_{1-y}C_y$ structures is described. The epilayers, heterostructures and superlattices are characterized by high resolution x-ray diffraction using rocking curves, reciprocal space mapping and x-ray reflectivity. In particular it is shown that the strain relaxation mechanism proceeds in the SiC layers via the formation of β-SiC precipitates in contrast to Si/SiGe where misfit dislocations relief the misfit strain. First attempts for a modulation doping of Si/$Si_{1-y}C_y$ heterostructures are described, for realizing high mobility two dimensional electron gases. The luminescence from multi-quantum well structures with electrons confined in the $Si_{1-y}C_y$ wells was observed and analyzed. In addition, the fabrication and the performance characteristics of Si/SiGe MQW intersubband detectors are described.

1. Structural Characterization of MBE Grown Si/$Si_{1-x}C_x$ Multiquantum Well Structures by High Resolution X-Ray Diffraction

Si-based heterostructures offer interesting possibilities for high frequency devices based on Si technology. There has been an increasing interest in such devices and several companies have recently announced the production of Si/SiGe heterobipolar transistors [1].

The MBE growth of $Si_{1-x}C_x$ epilayers has recently attracted considerable attention, offering an alternative and addition to the so far much more studied Si/SiGe heterostructure system [2]. Since the lattice constant of these alloys is smaller than that of Si, the epilayers are under biaxial tensile strain, which leads to a conduction band alignment according to which the electrons will be confined to the $Si_{1-x}C_x$ layers. Thus, a two dimensional electron gas can be realized in principle within a pseudomorphically grown epilayer. In Si/SiGe heterostructures, such a 2D electron channel can only be realized by depositing a Si layer on top of a relaxed SiGe buffer layer. The necessary relaxation of the SiGe buffer is caused by misfit dislocations and the accompanying threading dislocations penetrate through the active 2D channel to the surface, and are thus unavoidable. This disadvantage is circumvented in Si/SiC heterostructures, at the expense that the 2D electrons are confined in the $Si_{1-x}C_x$ layer where they suffer from alloy scattering.

However, the solubility of carbon in silicon is only $3.5x10^{17}$ atoms/cm^3 in thermodynamic equilibrium. Non-equilibrium techniques like plasma enhanced chemical vapor, deposition molecular beam epitaxy (MBE) and solid phase epitaxy allow the growth of $Si_{1-x}C_x$ epilayers with carbon contents of a few percent (up to about 4%) [3]. We have grown such layers using MBE, where the chamber was equipped with three electron beam evaporators, for Si, Ge, and C. The beam fluxes were monitored and controlled with a quadrupole mass spectrometer, the Si substrate temperatures were varied between 700 °C and 450 °C.

We have investigated the structural quality of such heterostructures, multiquantum wells and superlattices by using several x-ray techniques: (i) high resolution x-ray diffraction, (ii) reciprocal space mapping, (iii) specular x-ray reflectivity measurements and (iv) reciprocal space maps around the origin (000), measuring diffusely scattered radiation. The purpose of these investigations was to assess the strain status of the epilayers, to determine the layer thicknesses and the carbon contents, and to establish whether the deposited epilayers were pseudomorphic or not with respect to the (001) Si substrate. In Fig. 1, rocking curves of two pseudomorphic SiC/SiGe superlattices are shown. The reflectivity measurements yielded information on the $Si/Si_{1-x}C_x$ interface roughness as well as the correlation properties within the growth plane and perpendicular to it.

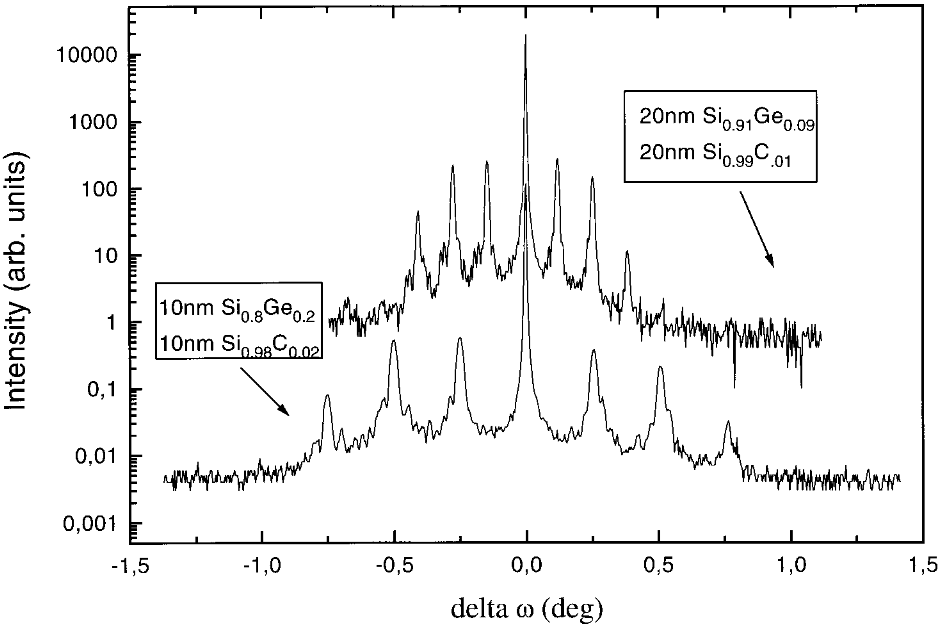

Fig. 1: X-Ray rocking curves of two SiC/SiGe superlattices on (001) Si, which show strain compensation for the parameters (SiGe, SiC layer thicknesses and C and Ge contents as chosen). Number of periods: 10

The main results are the following:

With increasing epilayer thickness and/or with increasing carbon content, the relaxation of the $Si_{1-x}C_x$ epilayers occurs through the formation of β–SiC precipitates and not through the formation of misfit dislocation as in the case of Si/SiGe heterostructures.

The epilayers stay pseudomorphic even after the formation of $Si_{1-x}C_x$ has occurred as can be determined without any ambiguity from reciprocal space maps around oblique (224) reciprocal lattice points. Apparently, the excess carbon that cannot be accommodated as a diluted alloy forms these precipitates, which have a size from about 2 to 6 nm (as determined by transmission electron microscopy).

The interface roughness of Si/Si$_{1-x}$C$_x$ heterostructures with C contents of about 1 – 2 % is quite similar to that of Si/SiGe heterostructures as has been determined recently by high reflectivity measurements using synchrotron radiation at the Optics Beam Line of the ESRF, Grenoble. (A carbon content of about 1% causes the same absolute amount of biaxial strain as a Ge content of 9%.) In Fig. 2 data on the diffuse scattering are shown, by measuring ω-scans in the reciprocal lattice around (000) through the 1st, 2nd and 3rd satellite maximum. Fits to the experimental data as shown yield an interface roughness of about 4Å.

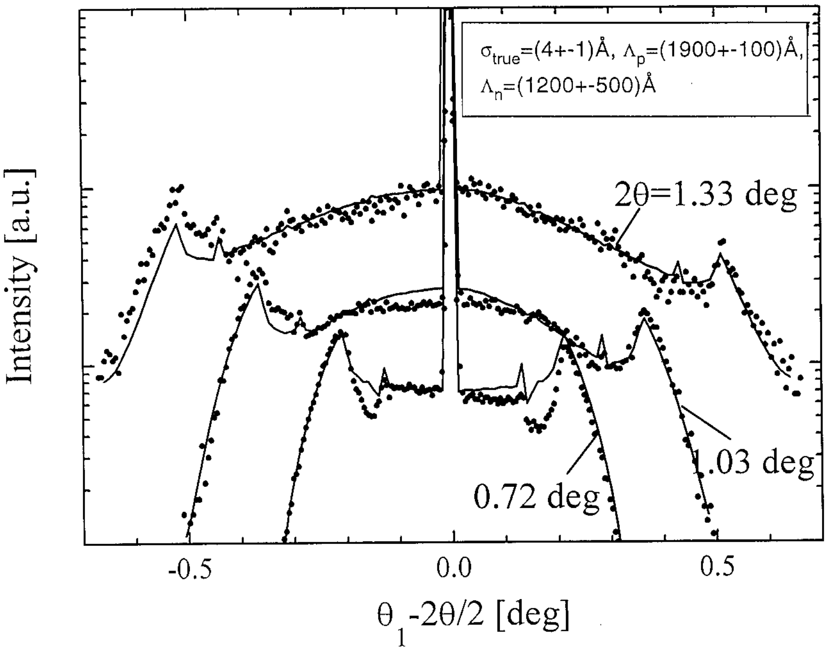

Fig. 2: Determination of interface roughness of SiGe/SiC superlattices from ω-scans in the reciprocal lattice.

We have also investigated the thermal stability of such heterostructures by thermal annealing experiments at temperatures in the range from 800° to 950°C. The thermal treatment causes also the formation of β-SiC precipitates, whereas the remaining carbon stays substitutionally on Si sites in the lattice. Thus the annealed Si$_{1-x}$C$_x$ epilayer stays pseudomorphic, but annealing reduces its carbon content at the expense of precipitate formation. Even at these elevated temperatures used for the annealing experiments no evidence for misfit dislocation formation was found within the accuracy of the x-ray mapping methods.

For the use of Si/Si$_{1-x}$C$_x$ heterostructures the findings about the interface roughness are encouraging for future devices. The annealing experiments show that the thermal stability of the silicon-carbon alloys is comparable to that of SiGe alloy layers, with the main difference that no misfit dislocation formation occurs.

2. Si/SiGe Quantum Well Infrared Photodetectors

There is a strong need for infrared detectors operating in the two atmospheric windows at 3 – 5 µm and 8 – 12 µm which are based on silicon and are thus compatible with existing Si electronics. Presently silicide (PtSi and IrSi) detectors are employed for imaging arrays, whereas HgCdTe is used for high-sensitivity single-element applications. Quantum well infrared photodetectors (QWIPs), which are based on intersubband transitions in quantum wells, are promising alternatives which ultimately could replace both of the above. Up to now, most of the related research has concentrated on GaAs/ AlGaAs quantum wells [4]. In the present report we describe the fabrication and performance of QWIPs based on Si/SiGe quantum wells [5].

The detector structures consist of 10 $Si_{0.65}Ge_{0.35}/Si$ quantum wells with a thickness of 25 Å, separated by 300 Å Si barriers and are grown pseudomorphically on a Si (001) substrate. The quantum wells were doped p-type to 1.2 x 10^{12} cm^{-2} per well. The active region is enclosed by two heavily p-doped contact layers. The quantum well thickness is such that the first excited heavy-hole state is near the top of the quantum wells, so that the absorption of an infrared photon leads to a photocurrent.

The samples were characterized by polarization dependent infrared absorption spectroscopy, which allowed clear assignment of the active transitions [6]. The cut-off wavelength of the present structure is at 1200 cm^{-1} (8 µm) for p-polarized and at 1400 cm^{-1} (7 µm) for s-polarized radiation. s-polarized absorption, which is equivalent to normal-incidence absorption, is only possible due to the band mixing present in the valence band. This is a significant advantage when compared, e.g., to n-GaAs QWIPs, where normal-incidence detection is not possible without special coupling schemes. In our device the photoresponse between 3 µm and 7 µm peaks at a wavelength of 5 µm and is actually higher in s-polarization than in p-polarization.

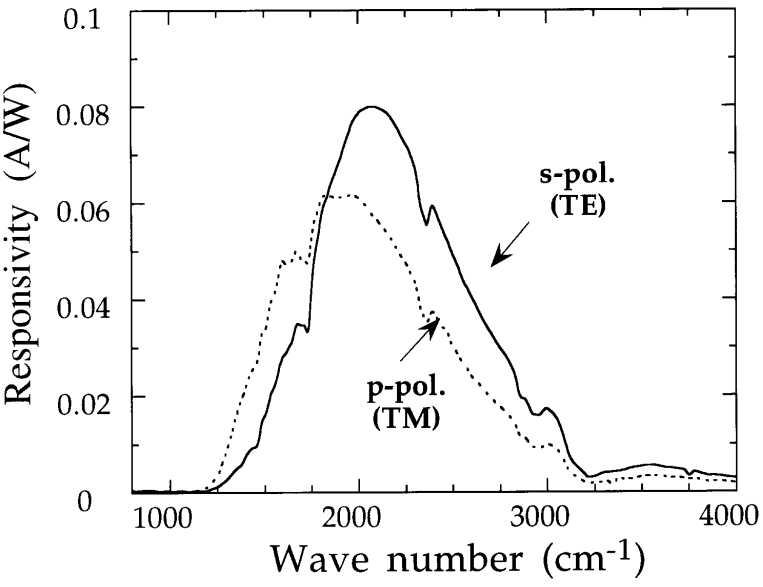

Fig. 3: Spectral dependence of the photoresponse measured in s- (solid line) and p- (broken line) polarization.

Detector elements of 100 – 400 μm diameter were fabricated by photolithography, reactive ion etching and metal evaporation/lift-off techniques. The spectral dependence of the responsivity for both orthogonal polarization directions is shown in Fig. 3. Figure 4 shows the dependence of the normal-incidence responsivity on the bias voltage, V. At V = -3.5 V, we measure a normal-incidence current responsivity as high as 80 mA/W.

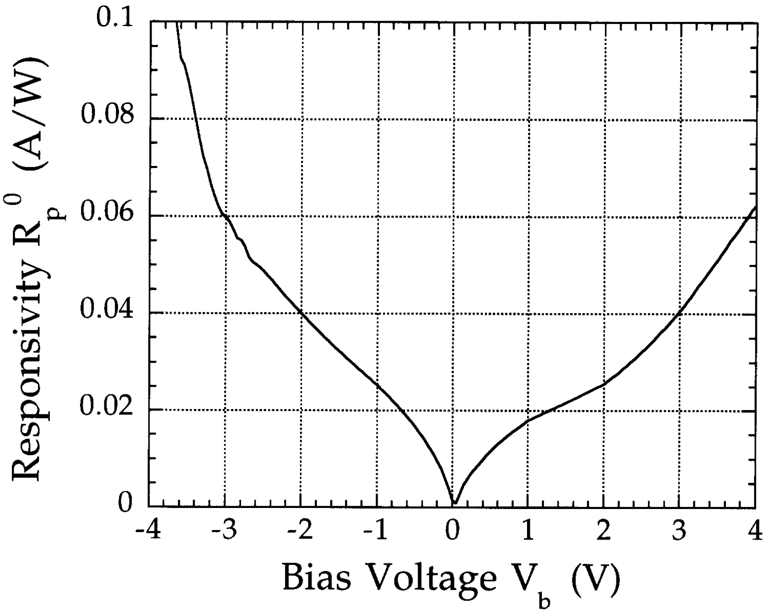

Fig. 4: Bias dependence of the peak responsivity.

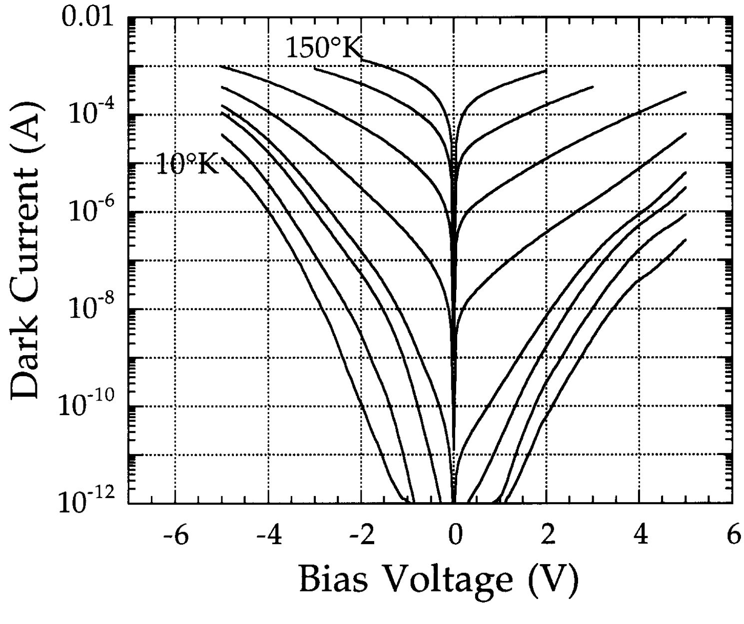

Fig. 5: Dark-current–voltage characteristics of a 200 μm mesa device for temperatures between T = 10 K and 150 K, in steps of 20 K.

In Fig. 5, the dark-current–voltage characteristics of a 200 μm device are shown for temperatures between T = 10 K and 150 K, in steps of 20 K. If the dark current divided by the temperature is plotted versus the inverse temperature, an activation energy can be extracted. Such an evaluation is presented in Fig. 6. At V = 1 V, an activation energy of 154 meV results, which is consistent with the energy difference between the Fermi level and the top of the barriers in the present structure. At higher bias, the activation energy decreases due to the effective lowering of the barriers (not shown). The low dark current gives rise to BLIP (background limited infrared performance) operation at T = 80 K for a bias of 1 V and even higher BLIP temperatures at lower bias. Noise measurements for evaluation of the detectivity, D*, are currently performed.

To summarize, we have shown that high-performance normal-incidence QWIPs can be fabricated from Si/SiGe. Such detectors can be designed for different peak wavelength over a wide range and are more sensitive than silicide detectors.

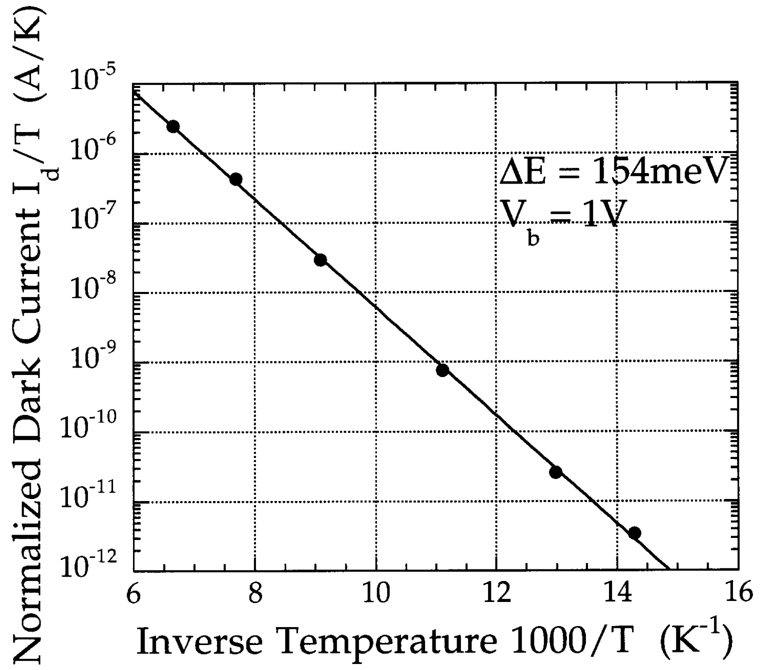

Fig. 6: Evaluation of the activation energy from the dark current at 1 V bias voltage.

3. Photoluminescence from Si/$Si_{1-x}Ge_x$ and Si/$Si_{1-y}C_y$ Heterostructures

As described in the proposal, a facility for photoluminescence measurements in the near infrared has been set up in Linz. The Si based heterostructures are excited with Ar-ion laser radiation, and the samples are placed in a variable temperature insert in a He cryostat. The luminescence light is collected and analyzed with a grating monochromator and detected with a North Coast Ge detector. A wavelength range from 0.8 μm to 1.7 μm can be covered with this system.

The luminescence studies contribute essentially to the characterization of the MBE grown materials, in particular the luminescence lines and their efficiency yield information on the amount of defects present.

The luminescence from Si/SiGe quantum wells grown pseudomorphically on (001) Si has been well described in the literature. A series of such MQW's with the following parameters 10 x (51.3 Å SiGe$_{0.23}$ / 69Å Si), 10 x (68Å SiGe$_{0.31}$ / 61Å Si), 10 x (30.8 Å SiGe$_{0.23}$ / 69 Å Si) has been measured and is shown in Fig. 7. The spectra are dominated in the SiGe QW-part by the no-phonon line (NP) and the Si-Si TO phonon replica line. These structures shift with decreasing quantum well width to higher energies. Furthermore, at about 1.1 eV a series of luminescence lines appears which are due to radiative band edge recombination in the Si layers (TO phonon replicas of free excitons and bound excitons due to boron impurities). At 1.15 eV the no-phonon band edge recombination lines of Si appear.

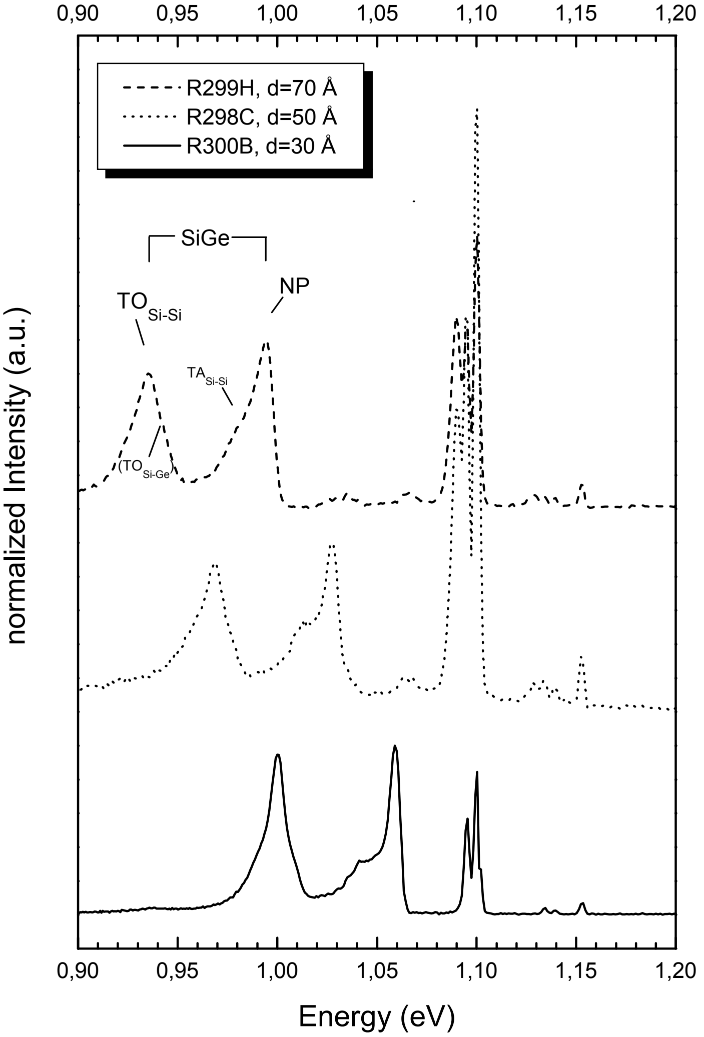

Fig. 7: Measurements on SiGe MQWs, normalized to the SiGe-NP signal. The samples have different quantum well widths, one can clearly see the increase of the confinement-energy with decreasing well width.

Recently, Eberl et al. [7] have concluded from luminescence studies on a series of Si/$Si_{1-y}C_y$ multi-quantum wells that this system has a type I band alignment, which would make these heterostructures extremely interesting for optoelectronic applications. However, there is still a controversy about the interpretation of these data regarding conclusive evidence for a type I band alignment.

We have recently performed preliminary investigations on the luminescence from our MBE grown $Si_{1-y}C_y$ epilayers, on Si/$Si_{1-y}C_y$ quantum wells and multiquantum well structures. In Fig. 8, the luminescence vs. energy is shown for a Si/$Si_{1-y}C_y$ multi-quantum well (MQW) sample with a carbon content in the wells of 1.5%, a well width of 50 Å, a Si spacer width of 150 Å (10 periods). In the photoluminescence spectra a no-phonon line and a TO phonon replica from the $Si_{1-y}C_y$ quantum wells can be seen at about 1.04 and 0.98 eV. The lines at higher energies are due to electron-hole droplets (1.08 eV), the TO-phonon replica of a bound exciton line at 1.092 eV and finally the no-phonon bound exciton line of Si at 1.15 eV. This sample was grown at about 450°C.

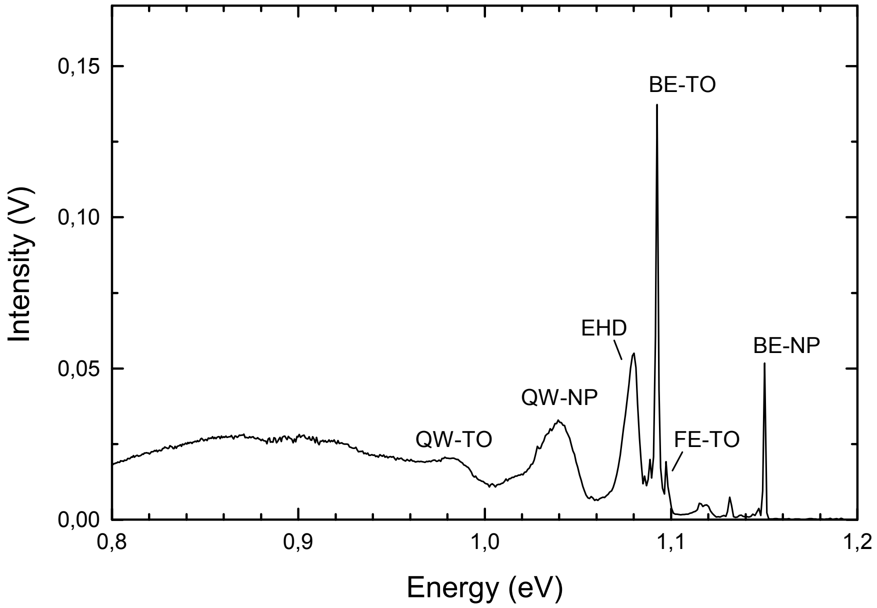

Fig. 8: Photoluminescence spectrum from a Si/$Si_{1-y}C_y$ MQW.

In order to grow strain compensated structures on the (001) Si substrates, a MQW structure with alternating $Si_{1-x}Ge_x$ and $Si_{1-y}C_y$ layers can be grown. Luminescence data from such a MQW with $Si_{1-x}Ge_x$ (x = 9.15%) layer thicknesses of 87 Å and $Si_{1-y}C_y$ (y = 1.37%) of 87 Å are shown in Fig. 9. The luminescence efficiency is smaller than for Si/$Si_{1-y}C_y$ quantum wells, however a transition at 1.115 eV and its TO replica at 1.055 eV are attributed to QW luminescence. All other lines originate from Si.

The rather weak luminescence from the QW regions in the $Si_{1-x}Ge_x$/$Si_{1-y}C_y$ MQW's is most probably not an intrinsic property of the strain compensated Si based heterostructures but reflects rather insufficient material quality. In particular, the fact that free exciton lines are absent and only bound exciton lines (due to Sb or P) can be seen indicates rather high unintended impurity concentrations. Modifications of the e-beam evaporators scheduled for the next two months and additional pumping of the growth chamber by a newly commissioned turbo pump are expected to greatly improve the background contaminations in the MBE apparatus.

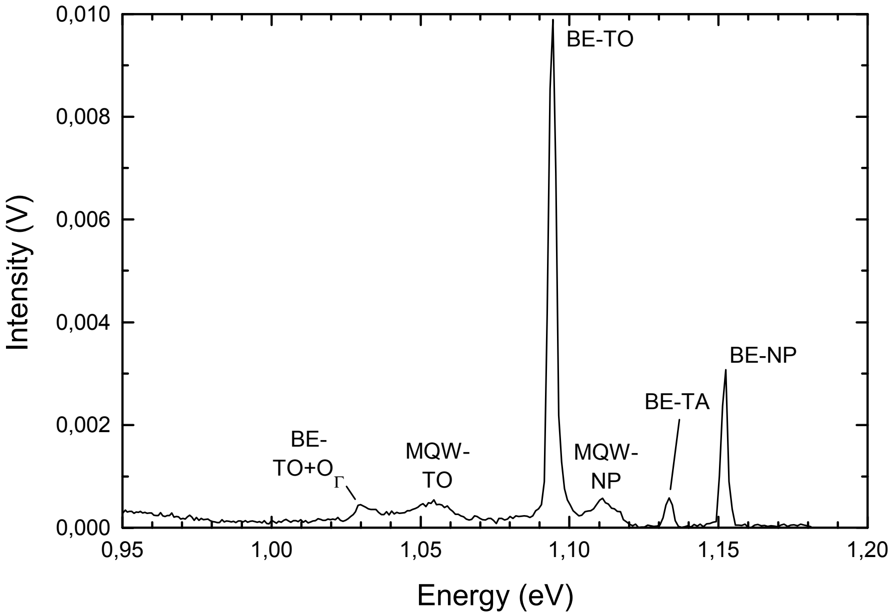

Fig. 9: Photoluminescence spectrum from a strain-compensated $Si_{1-x}Ge_x/Si_{1-y}C_y$ MQW.

4. Conclusion

Si /SiGe and Si/SiC heterostructures have been grown by MBE and characterized with respect to their structural, electronic, and optical properties. The structural characteristics of pseudomorphic Si/SiC heterostructures are quite similar to those of Si/SiGe, in particular with respect to the interface roughness. First experimental data on modulation doping of Si/SiC structures have been obtained. An electron mobility enhancement with respect to that of bulk Si has been observed in SiC channels, however, mobilities are still influenced by background residual impurities. Interband luminescence in Si/SiC quantum wells was observed as well.

Intersubband quantum well detectors (Si/SiGe MQW’s) for the mid-infrared region were fabricated and characterized with respect to their detector characteristics.

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Project Information

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Kruck	Peter	dissertation	
Penn	Christian	dissertation	
Stangl	Julian	dissertation	
Straub	Hubert	dissertation	50% GMe funding
Zerlauth	Stefan	dissertation	

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16. T. Fromherz, P. Kruck, M. Helm, G. Bauer, J.F. Nützel, G. Abstreiter: "Polarization dependence of intersubband absorption and photoconductivity in p-type SiGe quantum wells", Superlattices and Microstructures, submitted.

Presentations

Invited Talks

1. T. Fromherz, P. Kruck, M. Helm, G. Bauer, J.F. Nützel, G. Abstreiter: "Polarization dependence of intersubband absorption and photoconductivity in p-type SiGe quantum wells", International Conference on Intersubband Transitions in Quantum Wells: Physics and Applications, Oct. 23 – 26, 1995, Kibbutz Ginosar (Sea of Galilee), Israel.
2. M. Helm: "Infrarotspektroskopie von Löchern in Si/SiGe Quantum Wells / Intersubbandrelaxation in GaAs/AlGaAs Quantum Wells", Universität Marburg, 28.11.1995.
3. G. Bauer, J.H. Li, E. Koppensteiner: "X-ray reciprocal space mapping of Si/SiGe heterostructures", European Materials Research Society, Strasbourg, France, 22. – 26. Mai 1995.
4. T. Fromherz, J.H. Li, P. Kruck, M. Helm, G. Bauer: "Intersubband spectroscopy on Si/SiGe multi quantum wells and their structural characterization", Heterostructures *de semiconducteurs IV-VI*, Orsay, 26. – 27. Okt. 1995.

Poster Presentations

1. T. Dietl, J. Jaroszynski, M. Sawicki, P. Glod, J. Wrobel, G. Stöger, G. Brunthaler, G. Bauer, F. Schäffler: "Electron localisation in Sb-doped Si/SiGe superlattices", XXIV International School on the Physics of Semiconducting Compounds, Jaszowiecz, Poland 1995.
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Doctor’s Theses

1. G. Stöger, Quantum interference effects, hot electrons and metal insulator transition in Si/SiGe heterostructures and superlattices, Universität Linz, 1995.

Habilitations

1. W. Faschinger, Molekularstrahlepitaxie von II-VI-Verbindungen mit großer Energielücke, Universität Linz, 1995.

Cooperations

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Doping Problems in Semiconductors

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We present two examples of current investigations of point defects in semiconductors: (i) the characterization of Er centers in Si and their properties as a source of 1.5 µm luminescence, and (ii) problems arising in the doping of large gap II-VI compounds. We show that the luminescence yield of Er in Si can be improved by hydrostatic pressure, and we explain this in terms of energy transfer via defect recombination. Nitrogen in II-VI compounds is shown to be an effective acceptor as needed for light emitters from such materials.

1. Introduction

The controlled introduction of point defects with well-known structural, electronic and thermodynamic properties is the most important tool for the achievement of specific properties and thus for the fabrication of semiconductor devices. In spite of 50 years of intense research on the properties of point defects in semiconductors there is still a number of barely understood problems. Two of such problems are investigated here.

The first one concerns erbium as a dopant in silicon. The rare earth element erbium has an incompletely filled inner 4f shell that is very well shielded by the outer 5th and 6th shell. The crystal rather acts as a weak perturbation and the radiative internal transitions within the 4f shell produce almost atom-like spectra with the main transition occurring at 1.54 µm, independent of the host crystal [1 – 3]. The latter manifests itself only by its crystal field, which, together with other nearby defects and impurities, causes subtle characteristic splittings of the main transition. Nevertheless, owing to the long radiative life time of about one millisecond and the weak perturbation, the line widths are extremely narrow (typically less than 0.1 cm^{-1}) and the splittings are well resolvable.

The wave length of the main transition, 1.54 µm, makes Si:Er an interesting candidate for a Si-based integrable light source for optical communication via silica fibers, which have their minimum damping right at that wave length. Problems arise, however, from the temperature induced quenching of the luminescence yield, which occurs well below room temperature already. Co-doping with light elements like C, N, F, and, most efficiently, O, was found to improve the efficiency dramatically but still not sufficiently for room temperature applications. In this work, we show another way of improving the efficiency by application of hydrostatic pressure. We attribute this effect to the change in the energy transfer rate from the Si crystal to the 4f shell of the Er, whereby we consider the role of additional oxygen as co-activator in the Er luminescence.

In part 3 of this report we describe our efforts and successes in the attempt to dope large gap II-VI compounds also highly p-type. The latter is a necessary requirement for laser structures built from such materials with the goal of achieving short wave length emission.

2. Erbium in Silicon

The originally rather weak PL yield has been substantially improved over the years by co-doping with light elements and optimized annealing procedures, without gaining too much insight in the underlying physical mechanisms [2]. In particular, the question, how the energy is transferred from the host crystal to the 4f shell of Er, which produces this PL, is only tentatively solved.

Most authors assume that defects are involved in this process. In a first step, the exciting photon is absorbed and generates an exciton that can transport part of the excitation energy over macroscopic distances, much wider than the Er-containing surface layer that is produced either by ion implantation or molecular beam epitaxy. (These techniques are preferred since they produce a state far from thermal equilibrium and thus they allow to overcome the limited solubility of Er.) Then these excitons are trapped at or close to an Er containing defect located close to the surface. As a next step, the de-excitation or recombination of the exciton leads to a non-radiative transfer of the necessary energy for the intra-4f transition from the J = 15/2 ground state to the first excited, the J = 13/2 state. Obviously, different Er configurations have different efficiency in this transfer process, which allows to optimize the PL yield by “breeding” particularly suitable Er complexes by co-implantation and short time annealing procedures [3].

The energy released by the “supplying” defect state should be at least close to the intra 4f excitation energy. A difference in energy can be accommodated by local phonons or other low energy excitations. The latter process works better at elevated temperature which causes, however, also a quenching of the PL yield due to a “backtransfer” process which is envisioned as just opposite to the excitation process: under thermal excitation, the exciton bound at the supplier defect can be released again and dissipated elsewhere.

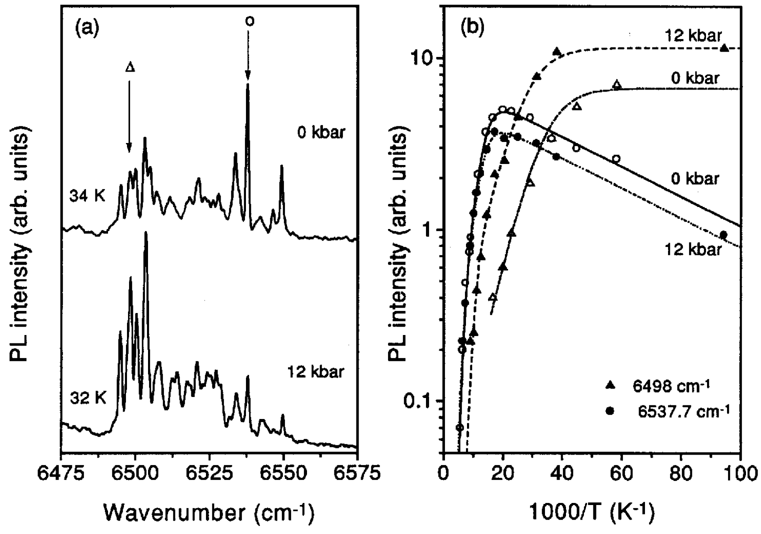

Fig. 1: (a) Photoluminescence of Si:Er, O without and with a hydrostatic pressure of 12 kbar. (b) Arrhenius plot of the luminescence intensity of two lines marked in Fig. 1a (circle and triangle, respectively) with and without pressure.

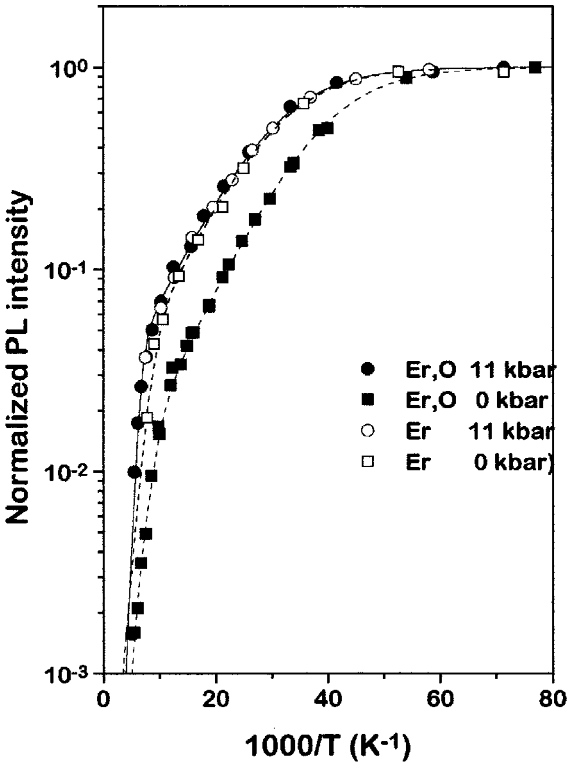

Fig. 2: Arrhenius plot of the luminescence intensity of Si:Er, O (full symbols) as compared to that of a sample without additional O implantation.

In order to test such a model, we have performed a study of Er in Si under hydrostatic pressure. High resolution Fourier spectroscopy allows us to distinguish different centers as reviewed elsewhere [3] and to determine their PL yield individually up to temperatures of well above 200 K. The sample is put into a pressure cell employing a piston and benzene as pressure transmitting medium up to a pressure of 20 kbar. The cell is attached to a cold finger cryostat and cooled to temperatures down to 10 K.

In Fig. 1 (a), two PL spectra of Si:Er, O are shown for 0 and 12 kbar, respectively. It is clearly seen that pressure affects different lines that belong to different centers individually: some lines increase strongly, some decrease and others seem to be unaffected. The dependence of the PL intensity for the two lines indicated in Fig. 1 (a) by arrows on temperature is given in Fig. 1 (b) for the two pressures of 0 and 12 kbars each.

This type of behavior is observed only in samples with additional oxygen implantation as shown in Fig. 2: here the normalized intensity of the same cubic center is shown with and without pressure, with and without additional oxygen. Only after oxygen implantation the beneficial effect of the hydrostatic pressure is observed.

We may conclude from these findings that apparently oxygen provides an additional path for the energy transfer from the Si crystal to the Erbium 4f shell. This additional transfer mechanism depends obviously strongly on pressure. In the case of the cubic Er center and one of the centers ascribed earlier to an Er-intrinsic defect complex named “D1” the pressure causes an increase in intensity by almost an order of magnitude in an intermediate temperature regime (140 K > T > 25 K).

In an earlier paper [3] we have considered energy transfer via bound excitons which yields expressions of the type:

$$I(\mathrm{T}) = I(0)\left(1 + \frac{\mathrm{e}_{\mathrm{BE}}}{\mathrm{n}_{\mathrm{FE}}\mathrm{c}_{\mathrm{BE}}(1+\beta\tau)}\exp(-\mathrm{E}_{\mathrm{BE}}/\mathrm{kT})\right)^{-1}$$

where e_{BE}, E_{BE}, c_{BE} stand for the emission rate, the binding energy and the capture rate of excitons, b for the transfer coefficient and t for the Er radiative life time. Fitting such expressions (two separate ones for the regimes T < 100 K and T > 120 K) to the observed temperature dependence under pressure shows that in the intermediate temperature regime the activation energy is independent of pressure but the prefactor, which contains the coupling coefficient b, is strongly affected. In order to explain this behavior we propose that in the case of the additional transfer mediated by oxygen excitons trapped at oxygen centers excite first an oxygen-related deep level, which, in turn, transfers its excitation energy to the 4f shell of Er.

The effect of pressure is to shift the oxygen level relative to the 4f excitation energy. This mechanism explains the strong pressure dependence of b, which, in the spirit of perturbation theory, is described in terms of matrix elements and energy difference denominators. The latter may account for the observed strong influence of hydrostatic pressure on the PL yield, whereas the activation energy for quenching remains unchanged. This activation energy corresponds in our picture to the detachment energy of the bound exciton. Bound excitons are rather extended states, and these are well known to exhibit rather small pressure coefficients.

The observation of the strong influence of pressure on the PL yield thus suggests a new mechanism for the energy transfer and thus it also explains the beneficial role of oxygen-co-doping on the luminescence yield of Erbium in Si. This mechanism suggests also new possibilities to improve the efficiency of Si:Er based light emitting devices.

3. Doping of II-VI Compounds

The successful fabrication of the first blue-green laserdiodes in 1991 caused a breakthrough in the technology of the II-VI compound semiconductors with large energy gap. Lasers emitting in the blue range are needed, for example, for optical data storage at higher density than present. The main problem, namely the p-type doping of ZnSe, was solved using activated nitrogen as an acceptor.

Contemporary laser structures contain in the active region a so-called quantum well consisting of ZnCdSe with about 20% CdTe, corresponding to an energy gap of 2.54 eV at low temperatures. In order to extend the wave length further to the blue range an energy gap of 2.65 eV is needed for the active region. This requirement implies, however, that the gap of the cladding layers, consisting of ZnMgSe, should exceed 3 eV in order to provide the necessary optical and electrical confinement. The hole concentration then is limited, however, to less than 4×10^{16} cm^{-3} for a gap of 3.05 eV. This low value would lead to an enormous increase in the threshold voltage, which would further enhance degradation. The main task therefore was to find a material with both a large energy gap and higher saturation carrier concentration.

New doping techniques in molecular beam epitaxy based on plasma-activated N_2 gave carrier concentrations for p-type material orders of magnitude higher than previously obtained doping levels. Another milestone was the incorporation of magnesium into the family of II-VI compounds. In that way the energy gap and the lattice constant can be chosen separately in the quaternary compound.

In the framework of the research project supported by the GMe, the material system ZnMgSeTe was investigated and first electroluminescent devices were fabricated based on that quaternary compound. The epitaxial layers were grown in an MBE chamber equipped with effusion cells for Cd, Zn, Mg, Se, Te, and additional chlorine and nitrogen sources for n- and p-type doping. The most important results obtained in this field are the following:

1. It could be shown that the short period ZnSe/ZnTe superlattices could be doped p-type. Even for very low Te content, carrier concentrations up to 10^{19} cm^{-3} were achieved resulting in mastering the ever lasting contact problems to p-type material. Even the addition of 15% Mg, which opens the gap to the blue spectral range, had no influence on the high dopability. Using the so-called amphoteric native defect model, the doping limits could be explained and predicted for other II-VI compounds. This model was previously developed for III-V materials and described the dopability as a function of the conduction- and valence-band edge position relative to a universal energy level for all materials of this class.
2. Using the results described above diodes were grown consisting essentially of a ZnMgSe n-part and a ZnMgSe/ZnMgTe p-part. The concentration of Mg and Te in the n- and p-part were chosen to fulfill the condition of a common lattice constant and to obtain at the same time a maximal dopability. Electron and hole confinement could be achieved by varying the Mg and Te content in the active zone of the light emitting diode.

The first diode, realized in this material system, emitted in the green spectral range and showed electrical properties comparable with LEDs fabricated by Sony in 1994. With a forward bias of 6 V a current density of 500 A/cm^2 is obtained, which is clearly above the threshold current for laser emission. By using a ZnMgCdSe multi-quantum-well structure, the wavelength of the emitted light could be shifted into the deep blue spectral range.

Besides the excellent electrical characteristics of our LEDs there are some drawbacks in the linewidth of the emitted light, which made laser activity impossible so far.

One of the main reasons for that was the fact that our LEDs were grown on GaAs substrates and 2.5 μm thick buffer layers of ZnMgSe. That means that the whole structure contains much lattice mismatch causing dislocations at interfaces and as a consequence, it broadens the linewidth of the optical emission.

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A 60 GHz MMIC-Compatible TED-Oscillator

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Experimental results achieved with planar GaAs transferred electron oscillators at V-band frequencies are reported in this contribution. The active devices are MESFET-like structures with a Schottky-gate controlling the electron injection into the drift region. The electron injection is adjusted to a level yielding a frequency independent negative differential resistance, which is exploited for millimeter-wave power generation. The highest measured CW output power and efficiency are 8 mW and 1.6 % at 59.5 GHz, respectively. These results are comparable to those obtained with transistor oscillators which are much more difficult to fabricate due to their extremely small dimensions in the 0.1 μm range.

1. Introduction

Millimeter-wave MMIC´s have potential of being extensively used in future industrial and communication systems. In these systems one of the key elements is the oscillator capable of producing enough output power at these high frequencies. For power levels above 10 dBm at millimeter-wave frequencies mostly two-terminal devices such as Gunn or IMPATT diodes are used. The power levels achieved with transistor oscillators are lower than those of two-terminal devices but transistor amplifiers can be used for boosting up the power levels and they are in general much better suited for monolithic integration. Their disadvantage is the highly sophisticated technology needed to fabricate these millimeter-wave transistors.

A device much easier to fabricate is the so called **F**ield **E**ffect **C**ontrolled **T**ransferred **E**lectron **D**evice (FECTED) which combines the simplicity of two-terminal devices with the ability of being integrated with transistors and diodes. The FECTED is basically a planar Gunn-diode with an injection limiting cathode contact [1]. Due to the limited electron injection of the cathode the transit-time limitation is removed which makes the device especially well suited for millimeter-wave power generation. The main advantage, however, is the relaxed geometry of the device so that easy fabrication is possible. Very impressive results have been obtained at 35 GHz [2]. We now report new results achieved with identical devices operated at V-band frequencies.

2. Device Structure

Figure 1 shows a cross sectional view of a typical device. It consists of an 0.8 μm thick MOCVD-grown n-doped GaAs channel layer with a doping level of about $4*10^{16}$ cm^{-3}, an alloyed Ni-Au-Ge ohmic source contact, a Cr-Au-Schottky drain contact and a Schottky gate. A Schottky drain contact instead of an ohmic one has been used in order

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[1] Member, IEEE

[2] Senior Member, IEEE

to keep the electric field there low thereby minimizing breakdown effects [3]. The overlapping Schottky gate is separated from the source contact by a chemical vapor deposited SiO_2 layer with a thickness of 500 nm connecting the gate to ground RF-wise. The device width is 200 µm and the thickness of the semi-insulating substrate is 150 µm. The device as well as the circuit layout (Fig. 2) has been defined by electron beam lithography.

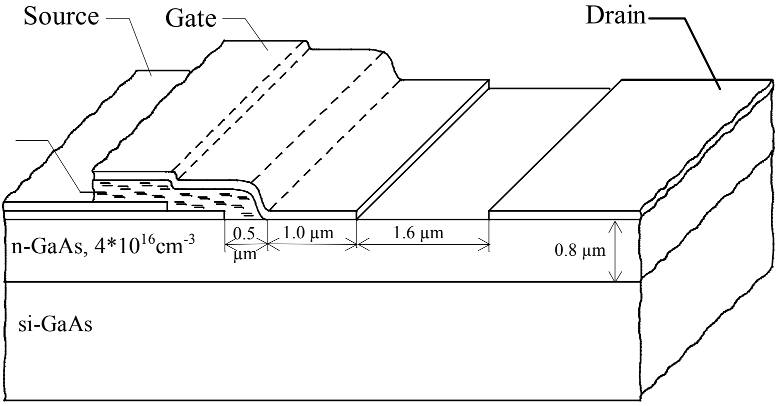

Fig. 1: Cross-sectional view of the FECTED

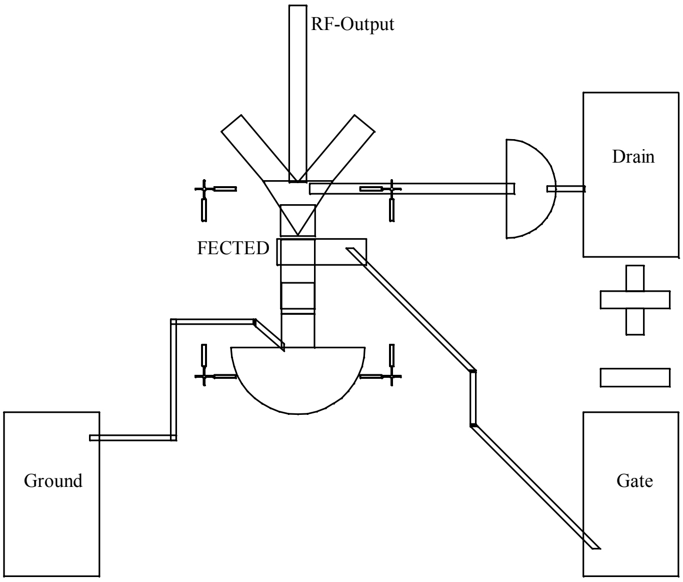

Fig. 2: Layout of the circuitry of the 60 GHz oscillator

3. Results

At 59.5 GHz an output power of 8 mW with an efficiency of 1.6 % has been obtained. The output power was corrected for the losses in the waveguide-to-microstrip transition and the measurement setup. Drain voltage and current were 7.5 V and 66 mA, respectively. The measured phase noise was about -78 dBc/Hz @ 1 MHz off carrier. A useful modulation range of about 1 GHz was obtained by simply changing the negative gate bias voltage. The highest frequency obtained with this design was 63.8 GHz with an associated power level of 1.76 mW and an efficiency of 0.43 %. Although these results have been achieved with circuits designed without any extensive simulations or CAD tools, they are nevertheless comparable to those achieved with transistor oscillators [4], [5].We therefore believe that improved performance should be obtainable by introducing more rigorous modeling and better testing equipment. Also, the use of a composite anode contact that combines a short stripe of a Schottky metal with an ohmic contact should lead to further improvement of performance [3].

4. Conclusion

Planar, monolithically integrated transferred electron oscillators have been fabricated for operation at V-band frequencies. The active device is a planar Gunn-diode with an injection limiting cathode contact that exhibits a broad band negative differential resistance, which is used for millimeter wave power generation. This device, which is called FECTED (**F**ield **E**ffect **C**ontrolled **T**ransferred **E**lectron **D**evice), is easy to manufacture and has a simple circuitry because it is a two-terminal device. The best result obtained with this type of oscillator is 8 mW at 59.5 GHz with an efficiency of 1.6 %. It is believed that further optimizations by means of better modeling and testing could result in higher power levels as well as in better efficiency.

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ASIC Design with Austrian Universities

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After giving a short survey of the project aims of UNICHIP and its development over the last years, selected activities are presented which have been completed in the last year. Besides covering new methods in teaching the design of user programmable logic devices, results of a long year research project on a multiple redundant field bus are described. The last part includes industry related projects. In the past year several analogue and digital ASIC design projects have been accomplished in cooperation with Austrian SMEs.

1. Introduction

The UNICHIP project was originally proposed in 1987 by the *Institut für Allgemeine Elektrotechnik und Elektronik* at the Vienna University of Technology. Since its very beginning this national activity was focused on three main topics in the area of the design of digital and analogue integrated circuits. Firstly, undergraduate education had to be intensified by means of offering the students access to state of the art hard- and software design tools together with the possibility to actually manufacture selected designs. Secondly, effective accomplishment of research and advanced development projects should be made feasible. Finally, the Austrian industry — mainly Small and Medium sized Enterprises (SMEs) — should be supported in using new technologies and design methodologies.

All of these aims required continuous investments in design hardware and Engineering Design Automation (EDA) software tools. Additionally, a measurement lab had to be installed enabling the verification on both digital and analogue behavior of integrated circuits that have been fabricated in the scope of UNICHIP.

The GMe has funded UNICHIP throughout the past years so we were able to set up and operate a ASIC design facility and thereby achieve every one goal of UNICHIP at least to a certain extent within the first years. The participation in the ESPRIT project *Teaching VLSI Design Skills* (EUROCHIP) and later on in EUROPRACTICE turned out to be a major breakthrough for UNICHIP. Both of these projects were launched by the European community to accomplish similar goals as UNICHIP but on a pan-European level. Several services are available such as very cheap access to both a variety of EDA tools and to IC prototype manufacturing facilities. Education and academic research are showing great success and have been pushed to an advanced level comparable to other European universities. In the recent past the SME support activities — by far the most difficult task — have been successful.

The remainder of the report will cover all three aspects of UNICHIP be means of short descriptions of selected projects.

2. Teaching UPLDs

2.1 Motivation and Background

UPLDs became an eminent factor in industry because of growing available complexity and pin numbers. They offer the advantage of system integration and miniaturization at small volumes. The migration to, for example, a gate array for high volumes is easier to achieve since some parts of the gate array design may be done automatically using special software tools for converting the UPLD design.

The goal of this new course is to teach practical knowledge about the structure, technology, and the area of application of UPLDs. The students gain personal experience by designing selected small circuits and transferring them from one design system or UPLD structure to another and comparing the results.

2.2 Aims

The course showed a comprehensive overview about all relevant UPLD-device families and their design tools. Not only were technical aspects like structure, speed, and complexity discussed but also economic criteria like availability, support, the structure of costs, and the important industrial aspects like problems with device programming (time, verification, long term stability) and second source were shown. Numerous software and UPLD distributors and manufacturers made test systems available for this course. This engagement enabled an objective comparison of different architectures and software tools.

The fundamentals of UPLDs were taught in five lectures at the beginning of the course. After that each student had to implement some small sample circuits on different architectures with different software tools. It was the intention of the selected examples to show which UPLD family is suitable for a special circuit structure or which software fits for a special design method. The students had to comment, interpret, and compare the obtained results.

It was the new approach of this course to teach UPLD knowledge not only by means of one special family with a selected design system but to present all available architectures and all relevant design systems. This wide approach together with solid fundamentals enables the students to make good use of their knowledge even in four or five years. This is very important due to the fast changes of technology in the UPLD area.

The following UPLD families were taught:

- XILINX — XC3000 Series, XC4000 Series, XEPLD (Hiper) Series
- Altera — MAX5000 Series, MAX7000 Series, EPLD Series
- Actel, TI — ACT1 Series, ACT2 Series
- Concurrent Logic — CLI Series

The following CAE-design systems were available:

- Log/IC for DOS, VAX/VMS, UNIX — Isdata
- MAXPLUS II for MS-Windows — Altera
- Migrate — Migration Technology
- Numerous Version of Workview for different UPLD families
- XACT — XILINX
- ALS for Actel — Actel
- IDS — Concurrent Logic

2.3 Results

24 students were registered for the CAE course “Design of User Programmable Logic Devices”. 20 of them have successfully finished their works. It was the key work of the examples to implement small designs on different architectures with a minimum of assistance. Therefore, they had to document not only their implementation of the simple example, which is quite boring, but their experiences and a critical comparison of the results with different tools and architectures.

3. PCC — A Pattern Classification Coprocessor

The aim of this project was to speed up a time consuming pattern matching algorithm by implementing it in hardware. The algorithm and system design have been accomplished by our industrial partner. Referring to several years of experience in developing complex UPLDs (User Programmable Logic Devices), the authors were put in charge of designing of a Pattern Classification Subsystem containing hardware accelerators. Besides of a complete specification of the interface circuitry, the PCC was defined as follows: Given a matrix **M** of size $i * j$ and a vector **X** of size j, the Manhattan distance between every row of **M** and **X** is calculated. The resulting vector is weighted by adding an offset vector and finally the minimal component of this sum is generated and written to the output port of the subsystem together with the corresponding row of **M**.

Adding all operations necessary to compute the Minimal Weighted Manhattan Distance (MWM) and taking the time constraints into account resulted in a CPU capable of performing some 260 MOPS. Expressed in another way, this leads to a necessary instruction cycle time of less than 4 ns. The first version of the PCC included the Manhattan distance calculation unit for 64 components per vector. The PCC was implemented using a XILINX FPGA (XC-4010) which was the only device available comprising the required resources such as 20 MHz system clock frequency, 16 bit adders with less than 50 ns delay, more than 700 flip flops, and 64 Byte on chip SRAM. Figure 1 shows a flow chart of the algorithm as implemented.

The System was implemented as a full sized PC-AT ISA Bus compatible board with a DSP as an on-board host CPU for the PCC. The PCC Subsystem is a successful implementation of an algorithm in hardware using one high density FPGA to its very extent. Compared to a software version of this algorithm running on a PC we gained computation speed of two orders of magnitude.

The XILINX FPGA has been replaced by a mask programmed version of the device recently, thus reducing the production costs of the complete system.

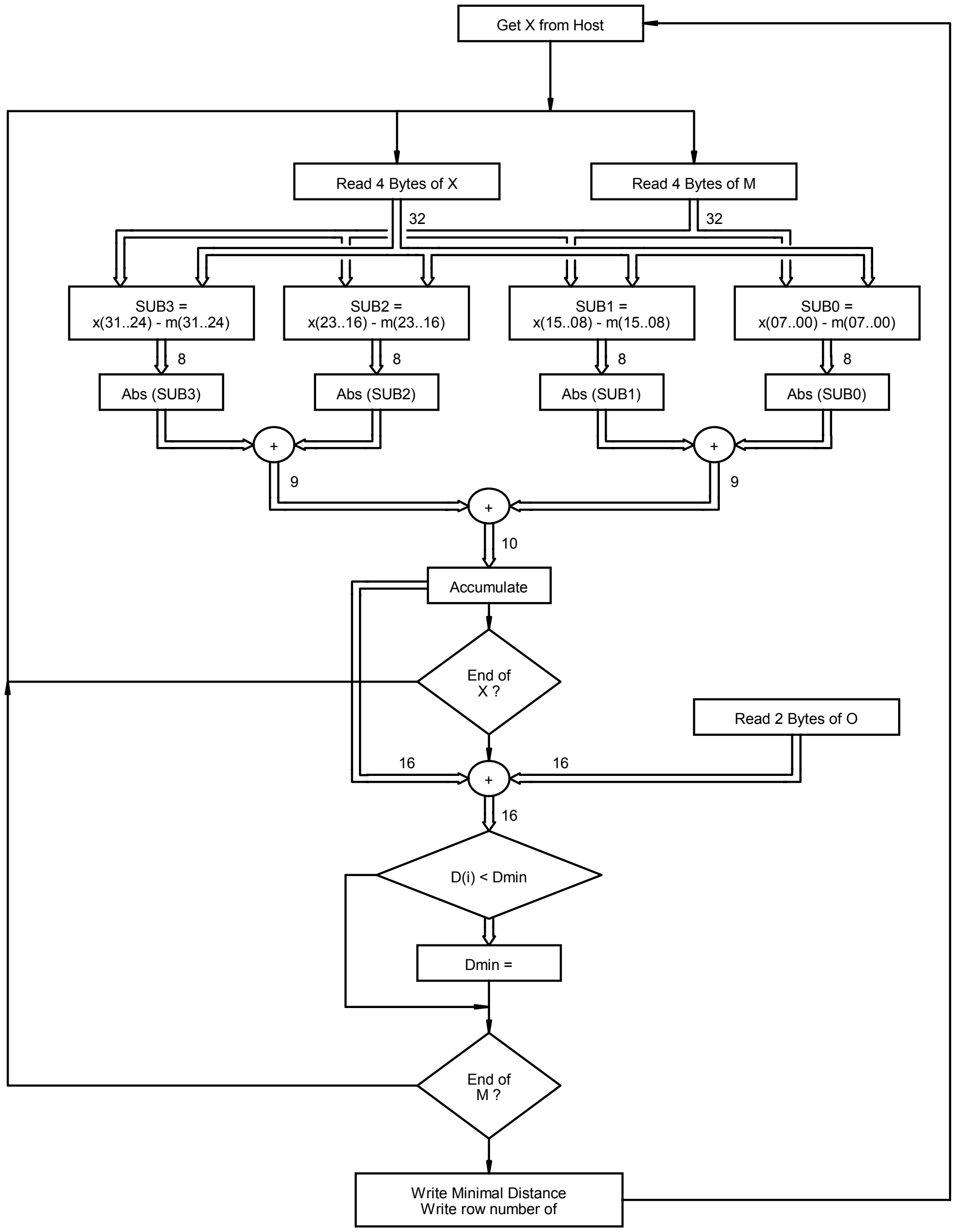

Fig. 1: Block diagram of the PCC implementation

4. XR-III, a Fault Tolerant Field Bus

The transmission line is the most sensitive part of a field bus. Not only do electromagnetic disturbances cause transmission errors, a failure of the transmission medium consequently means the failure of at least parts of the whole communication system. Moreover, repairing a broken cable is far more difficult than the exchange of other system components that are easily accessible. The use of redundant transmission lines is a possible solution, yet most of the existing field bus systems provide no means to facilitate the implementation of fault tolerance.

In contrast, the XR-III field bus makes use of two additional, active redundant cables, which ensures fault tolerance without any supplementary hardware as well as optimal performance. It features a serial master-slave structure suited for sensor-actuator applications, up to 256 nodes connected to a ring, 10 MHz data rate, and identical single-chip-controllers both for master and slave. The transmission medium is left to the choice of the user, fiber optic links are possible as well as coax or twisted pair cables with or without coupling transformers.

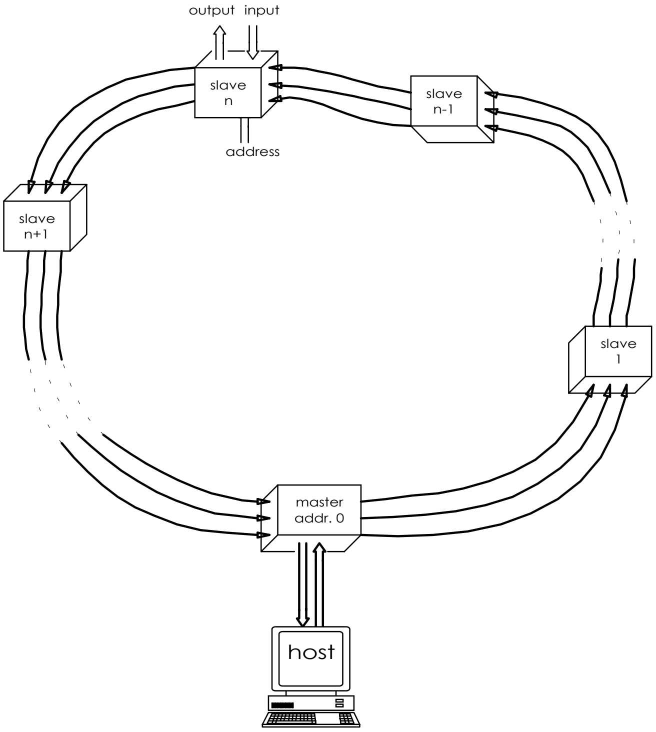

Fig. 2: XR-III structure

Data integrity is obtained basically by a CRC used for detection and correction of transmission errors and improved further using the active redundancy. This means that the data is transmitted simultaneously over all three lines and the receiver compares the information coming in on all lines and finally decides by a majority vote what has actually or more likely been sent. This active redundancy also prevents the loss of data in case of a cable failure.

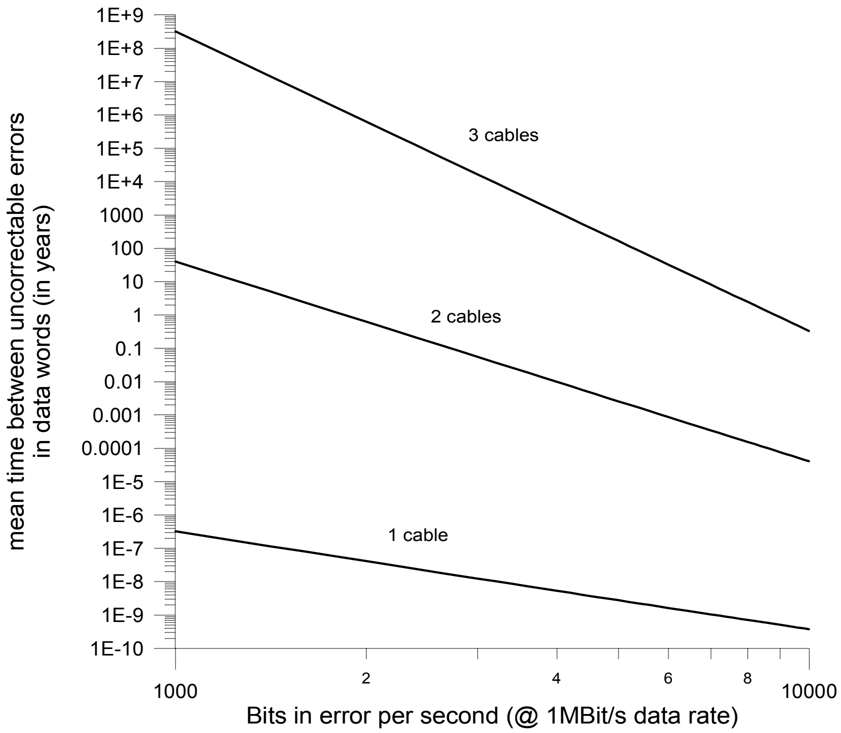

Fig. 3: Performance comparison using 1, 2, or 3 transmission lines

The first step towards realization of the concept was the design of a prototype using FPGAs. To ease implementation, a number of functions were omitted, and the design concentrated on the innovative and essential features of the concept. This way, the concept of active redundancy could be proved to be fully functional in praxis. Subsequently, a hardware description of the ASIC completed in the scope of a diploma thesis as a starting point for the production of a standard cell IC including the complete functionality of the XR-III protocol.

5. Ion Beam Control Subsystem

This project was initiated by the Viennese firm IMS who were looking for a Transputer based control hardware for their ion beam lithography machine. The Transputer architecture was selected mostly because of its ability to support distributed real time process control and the availability of high speed serial links. The latter were of particular importance since the whole subsystem was to be operated at a high dc potential (some 100 000 V), which demanded optically isolated data connections to the main computer. As the electrical environment was expected to be very harsh, great care had to be taken concerning EMC and ESD.

The complete subsystem consists of three double Euro printed circuit boards devoted to three distinct tasks. One comprises the Transputer itself, the electro-optical converters for two links that are used to communicate with the outside world, a state-of-the-art UART to interface with high end measurement equipment such as high resolution digital multimeters, two PS2 sockets for up to 8 MByte DRAM SIMs, and 32 optically isolated digital IOs. The connection to the other boards is given through the reserved signals of an off-the-shelf VME-bus backplane.

The second is a twelve-channel DA board for controlling the so-called multipoles that regulate the ion beam. Each channel is made up of a 16-bit DAC followed by an analogue amplifier. An on-board SRAM stores the last values written to the DACs to allow readback and serves as additional external storage facility for the Transputer. Because of the high density of components and to meet the EMC requirements, the board had to be entirely hand-routed. Two of these boards may be cascaded in a master-slave-configuration with a single central voltage reference.

Finally, the third board is used to control two power supplies. It comprises two 16-bit ADCs and DACs, respectively, with a 5 bit base address offset so that up to 32 boards can be used simultaneously under the control of one single Transputer main board.

All of these boards have been manufactured with four layers (two signal, ground, power supply), to save production costs, the power supply layer being split between the analogue and digital supply voltages. For address decoding and several control problems, numerous programmable logic devices have been employed.

6. Analogue Head Set Transceiver

The Viennese company Frequentis who are producing flight control equipment needed to replace their discrete analogue amplifiers for the headsets of the flight controllers with a single ASIC. Driving forces for this decision were not only the reduction of printed circuit board space along with the enhancement of functionality, but also the demand for in-house standardization.

The ASIC comprises two independent modules, each for one headset. The voice-band signals coming from a standard stereo codec are amplified and delivered directly to the headphones. The microphone signal, on the other hand, is amplified and level-shifted for processing by the codec. To monitor whether a headset is attached and to allow a system test, an analogue loopback is provided where the sum of the earphone signals is fed back into the microphone path.

The ASIC had to be realized in a combined full-custom and cell-array design style. Some macro cells could be taken from design libraries provided by the manufacturer, others had to be designed from scratch on a transistor basis. The particular challenge was the design of an off-chip driver capable of delivering 10 $\mathrm{mW_{eff}}$ to loads ranging from 150 to 600 Ohms. For the sake of low power consumption, the supply voltage had been restricted to 5 V, which left hardly a voltage margin for the output swing and required the buffer stage to be laid out in fully differential configuration. As the whole subsystem needs to be compliant to the ESD rules set up by CEE, large suppresser diodes are required to protect the board, resulting in extremely high capacitive loads varying from 0.5 to 3 nF.

A first prototype has been manufactured by way of the MPW service of EUROCHIP by MIETEC-ALCATEL. Owing chiefly to changes in the performance requirements, a redesign had been necessary for series production. This entirely new design, which also needs only half the area of the prototype, is now being manufactured by AMS. The prototypes have been verified successfully in January 1996.

7. 4-Channel Full Duplex G.726 ADPCM CODEC

In cooperation with SEMCOTEC — an Austrian SME company located in Vienna — we designed a four channel full duplex ADPCM codec that is fully compatible with ITU (CCITT) standard G.726. The ADPCM codec supports all four bit rates defined within the ITU standard and is pin compatible to the well-known SIERRA SC11362 device.

Starting from the ITU standard G.726, a simulation model of the ADPCM encoder and decoder was written in VHDL and was verified using the test vectors supplied by the ITU. We used this ADPCM simulation model as a golden model for writing a synthesizeable VHDL description of the quad full duplex ADPCM codec.

The parallel functional description of the behavior of the ADPCM was further modified to serialize some functions in order to share hardware resources, thus reducing the required area. Eliminating all parallel events would have resulted in a DSP-like general purpose ALU which in turn would have meant an overhead for implementing features like jumps and a higher system frequency. In order to stay compatible to the SIERRA ADPCM processor SC11362 we had to trade carefully area vice frequency. This optimization task was done manually since architecture synthesizers like CATHEDRAL-II produced insufficient results. In order to reduce the power consumption of the device we used a (synchronous) gated clock design methodology. The VHDL simulation and synthesis were done using the SYNOPSYS tools.

The quad channel full duplex ADPCM codec has been manufactured by National Semiconductors using a standard 0.8 μm CMOS process. Tests of prototypes were successful.

8. System Integration of A Digital Audio Processor System Using Logic Synthesis

A year ago, a customized DSP called DAP (Digital Audio Processor) was developed in cooperation with the Austrian company AKG for processing digital audio data to simulate a realistic and natural sound impression, which is achieved by special deep FIR algorithms. The audio processing system was developed by AKG for usage in a professional digital audio environment like recording studios. It comprises a microcontroller, fixed memory, a DAC, a fast static RAM, some glue logic, and finally the ASIC specially designed for this purpose.

We extended the idea of this audio processing system to applications in the area of consumer electronics. For this purpose we had to adapt the concept of the DAP in order to meet the special requirements of the high volume consumer market. We implemented all functions into one chip excluding only the digital-to-analogue conversion and the storage of coefficient data. The goal of this work was to prove the capability of the system integration to reduce dramatically the overall system cost. Beyond these more economic reasons we wanted to gain more detailed experience in using logic synthesis through this industrial design task.

In order to obtain an easily transferable design we decided to use the hardware description language VERILOG for functional design input together with the logic synthesis tool SYNOPSYS. Placement and routing were accomplished using the CADENCE software. The design work was carried out as a diploma thesis.

We showed that using system integration offers a large number of benefits. The overall system cost may be reduced by a large factor. The usage of VERILOG based functional design entry combined with synthesis using SYNOPSYS showed not only good results but also a speed-up of the design entry task and the capability of fast switching from one ASIC technology to another. A great productivity enhancement is further to be expected for designs of larger complexity than this.

The whole design task took about six months. The design has been finished successfully within the scope of the diploma thesis and is currently a refinement work is being completed to make this part suitable for the needs of AKG.

Project Information

Project Manager

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Project Group

Last Name	First Name	Status	Remarks
Cadek	Gerhard	dissertation	
Kausel	Wilfried	dissertation	
Kirsch	Rainer	student / dissertation	
Kowarsch	Eduard	student	50% GMe funding
Sauter	Thilo	dissertation	
Schreier	Roland	dissertation	
Thorwartl	Peter	student	50% GMe funding

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14. R. Metchev, J.E. Parra-Diaz, G.R. Cadek, and R. Schreier: “ASIC-Entwurf eines Netzwerkdruckpuffers”, Austro-Chip’94, 122 – 129.
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Cooperations

1. AKG-Acoustics
2. SEMCOTEC Vienna
3. Philips Dictation Systems
4. IMS Ionen Mikrofabrikations Systeme
5. Frequentis Nachrichtentechnik
6. Institut für Computertechnik, TU Wien, Prof. D. Dietrich
7. Institut für Technische Informatik, Prof. Grünbacher
8. Institut für Elektronik, TU Graz, Prof. Leopold
9. Institut für Angewandte Informationsverarbeitung, Prof. Posch
10. Institut für Systemwissenschaften, Universität Linz, Prof. R. Hagelauer

UNICHIP Graz —
Design of Integrated Circuits

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To satisfy the growing demand for engineers trained in the design of integrated circuits (ICs), the Department of Electronics offers several academic courses to cover this topic. In order to establish fundamental knowledge on design flow, verification, and test of ICs, also some research projects are carried out at the Department. The main area in IC design is the wide topic of mixed signal ASICs in CMOS or BiCMOS technology. In the following chapters there will be an introduction to the facilities and the courses at the Department of Electronics. Furthermore some IC-projects of the year 1995 are presented.

1. Introduction

A main part of the 1995 activity at the Department of Electronics in UNICHIP was training the students in the field of IC design. The Department offers five courses to cover the following topics:

- Basic IC-technology (fabrication, design-flow, silicon-technology)
- Fundamentals of MOS transistors
- Use of CAD tools (analogue and digital simulation, layout, standard-cell design, etc.)
- Analogue and digital circuit design
- Testing integrated circuits

In order to get a deeper understanding of the problems encountered with analogue integrated circuit design, two special courses at the EPFL in Lausanne/Switzerland were attended by members of the project team. The participation on some international conferences helps to establish good contact to the scientific community [3].

The AUSTROCHIP ‘95 Workshop in Graz was organized by the project team.

1.1 Academic Courses

The following table shows the titles and some related information on all courses related to IC design offered at the Department of Electronics.

There were 10 diploma theses finished in 1995. Some of them where carried out in close cooperation with the three major enterprises in Austria dealing with IC design and manufacturing (AMS, Siemens-EZM and MIKRON).

title of the course	type	hours/term	participants/year
Integrierte Schaltungen 1	VO	30	80
Integrierte Schaltungen 2	VO	30	45
Integrierte Schaltungen 2	UE	30	45
Testen Integrierter Schaltungen	LU	45	36
Elektronikprojekt	PR	90	10

Table 1: Courses dealing with IC-design

1.2 Facilities

1.2.1 Hardware

We are using the following hardware components in our courses as well as for research projects:

- 10 SUN-SPARC Stations
- 6 PCs
- Versatec-Electrostatic Plotter
- Micromanipulation Tool with Laser-Cutter
- Various IEEE-488 based measurement instruments (Logic Analyzer, etc.)

1.2.2 Software

We are using the following software-tools in our courses and for research projects:

- V8.2 Design Framework; Mentor Graphics
- GDT Tools; Mentor Graphics
- HSPICE; Meta Soft
- PSPICE; PC-based simulation for smaller projects
- XACT; Xilinx tools for FPGA-development using Mentor Graphics front-end
- HP-VEE; PC-based test-program-generation for IEEE-488 bus system

2. Experimental

In many courses there is a practical aspect that leads to some implementation and fabrication of chips by means of MPW (Multi-Project-Wafer) runs.

2.1 Student Projects

2.1.1 Universal I²C-Bus Module

The I^2C-bus is widely used in microcontroller applications. This student project was done by two persons. It started with schematic entry followed by simulation using M-Models in LSim and ended with a standard-cell layout for a 1.2µm CMOS-process. This layout is part of the ELEVE-chip, which is currently on the way to fabrication.

2.1.2 Development of a Transimpedance Amplifier in a 1.2µm CMOS-Technology

In this project a transimpedance amplifier circuit of a given topology was brought from simulation to layout. The circuit will be part of the ELEVE-chip.

2.1.3 CMOS and BiCMOS Input Amplifier for Piezoresistive Sensors

Two input amplifiers for piezoresistive sensors used for measurement of the velocity of sound in fluids were developed in this project. One was based on a mere use of MOS transistors. In the second circuit also bipolar-transistors were used. The layout was created by means of SDL (Schematic-Driven-Layout) using device generators. The circuits will be part of a test-chip in BiCMOS technology, which is intended to be in the factory in the middle of spring 1996.

2.1.4 Power-MOS Transistors of Various Layout Styles

An N-MOS and a P-MOS transistor were designed using various layout styles. The target was to reach an on-resistance of less than 10 ohms. Both transistors are part of the ELEVE-chip for evaluation on the workbench.

2.1.5 Development of a Static RAM Using Generator Tools

A 1kx8 static RAM was developed using a generator tool from Mentor Graphics. The layout was done for a 1.2 µm CMOS-process.

2.1.6 Circuits for Evaluation of Charge-Injection Effects in Analogue Switches

To be able to cancel charge-injection in analogue switches often so called dummy-switches are used. This project was done to simulate this effect and to do a layout to proof the obtained results. Three different switches were layouted and are part of the ELEVE-chip.

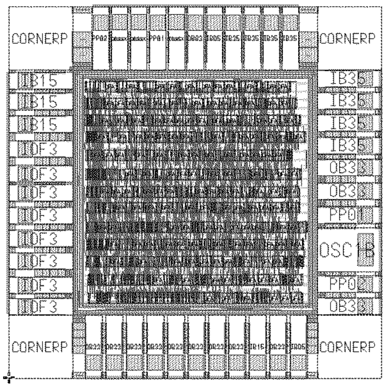
2.1.7 Evaluation of Former IC-Projects

The projects of the latest test-chip (EXPLORER [1]) were evaluated. The results for the various designs were as we expected them to be. They match the results from simulation very well.

2.2 Research Projects

2.2.1 ENDOR; a Chip for a Handheld Density-Meter

To minimize size and power consumption of a handheld, battery-powered density-meter an ASIC (ENDOR) was developed. It consists of some peripheral logic for a microcontroller and a unit for quantizing and coding in a charge-balance A/D-converter and a periodic signal. The microcontroller communicates via bus signals and registers with the ASIC.



process	1,2µm CMOS
transistor count	app. 8.000
area	2,5*2,5 mm^2
time for development	app. 6 months
package-type	PLCC-44

Fig. 1: Layout and technical data for the ENDOR-chip

2.2.2 Device Generators for Bipolar, NMOS, and PMOS Transistors

To speed up the analogue ASIC design it is necessary to use Schematic Driven Layout to offer consistency and ease of modification. As the devices in analogue integrated circuits are not part of a library they have to be generated according to properties attached to the element in the schematic representation of the circuit. In this project the following device generators for a BiCMOS process of AMS and the design environment of Mentor Graphics were developed:

- Bipolar NPN transistors of various styles
- N-MOS transistors of various styles
- P-MOS transistors of various styles
- Capacitors and resistors of various styles and different layers [2]

Figure 2 shows two layouts for transistors created by means of device-generators.

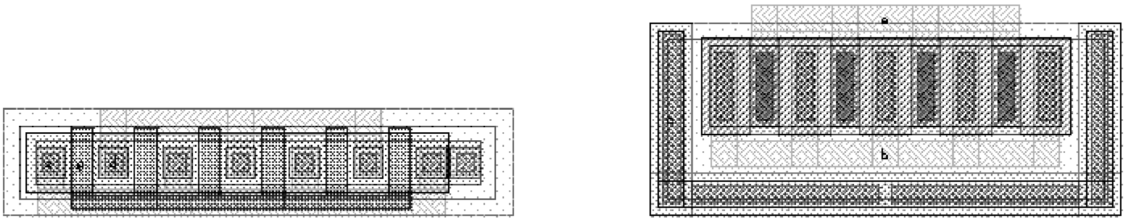


Fig. 2: Layout of an MOS- (left) and a bipolar-transistor (right)

In this project we had a close cooperation with AMS with the aim to incorporate these device-generators in the support-tool for customers.

2.2.3 Building Blocks in SC-Technique for Use in High Resolution A/D-Converters

In this project the building blocks (SC-integrator, sampled comparator, etc.) for high resolution A/D-converters will be developed using SC-technique. The project is not finished by now.

3. Conclusion

The design of integrated circuits from the idea to the chip is the main goal for the project reported. To train the students in this field there are some academic courses offered. Some student projects were realized on a test-chip to evaluate the simulation and the layout. There are also some research projects that are all together in the field of mixed-signal ASICs for sensor applications.

At the Department of Electronics there is a close cooperation to some firms mainly situated in Graz. Many students take the opportunity to do their thesis in one of them.

Although there are some contacts to small and medium sized enterprises the overall situation of technology transfer in the field of integrated circuit design is not as it should be.

Acknowledgments

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4. P. Söser: “Über die Entwicklung anwendungsspezifischer integrierter Schaltungen”, Herbsttagung der Studiengruppe für Elektronische Instrumentierung, Graz, 2.10.1995.

Cooperations

1. Institut für Angewandte Informationsverarbeitung und Kommunikationstechnologie; TU Graz, Prof. Dr. R. Posch
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Microsensors

Integrated Microsensors Implemented in Microsystems

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The aim of the project was the realization of a microflow system with implemented thermosensors. High sensitive thin-film temperature sensor arrays based on a-Ge were already realized and exhibited high sensitivity combined with high spatial and time resolution. Entering the field of microsystem technology and silicon micromachining, a new generation of flow sensors could be realized based on the principle of heat anemometry. Simulations of thermal heat flow yield an optimized structure able to measure gas and liquid flow with high dynamic range and high time resolution. Devices for measuring the liquid in an implantable microvalve and gas in an air intake of a combustion engine were accomplished.

1. Introduction

The aim of the project was the realization of a microflow system with implemented thermosensors. High sensitive thin-film temperature sensor arrays based on amorphous Germanium (a-Ge) were already realized and exhibited a high temperature resolution of 0.1 mK combined with a high spatial and a high time resolution of milliseconds [1]. For flow measurements, the principle of hot wire anemometry was modified. An a-Ge element acts as a heater and as a thermistor simultaneously. The cooling of the element, which is inserted in a flow stream, is the measured value and reflects the flow in an indirect way. This effect can also be used for measuring the blood flow in tissue and is called the method of heat clearance [2].

By using arrays of thermistor elements, a heating element passes heat into the flow, and the downstream thermistor will be additionally heated compared to an upstream sensor. In such a way the flow direction can be easily detected.

To enhance the sensitivity of a flow sensor, a thermal insulation from the substrate is favorable. An easy way to accomplish this task is the use of silicon micromachining by wet anisotropic etching. The use of silicon micromachined parts as essential elements of the construction of thermal flow meters results in reduced size, shorter response time and often less power consumption compared with classic flow rate meters [3, 4]. The use of a-Ge thermistors in combination with silicon micromachining increases the sensitivity and can further reduce the necessary thermal power and the disturbance of fluid temperature.

A flow channel can be formed in a silicon substrate, and a thermistor is placed on a silicon nitride bridge. An array of bridges crossing the silicon micromachined flow channel

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forms the base of the flow sensor. Each thermistor device consists of a vacuum-evaporated a-Ge resistor passivated by PECVD SiN_x [5]. The SiN_x acts as a mechanical support, as chemical insulation, and as a mask for the silicon etching.

A prototype device consisted of six thermistors and one thermistor/heating element [6]. Figure 1 shows the layout of the device.

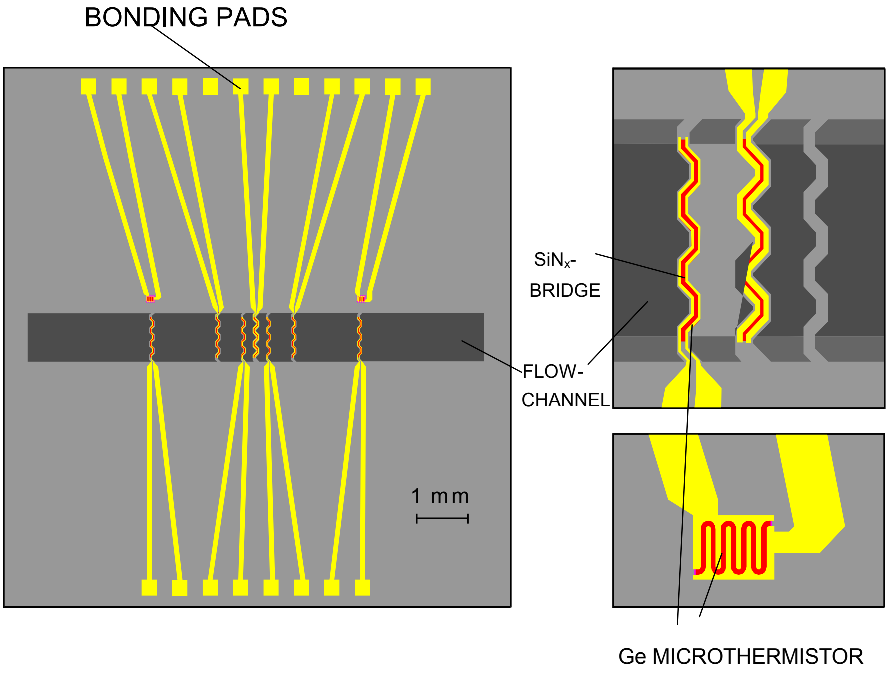

Fig. 1: Layout of a micromachined thermistor sensor array

Such a device was mounted on a conventionally formed upper part made from PMMA to form a flow channel. The cross section is shown in Fig. 2.

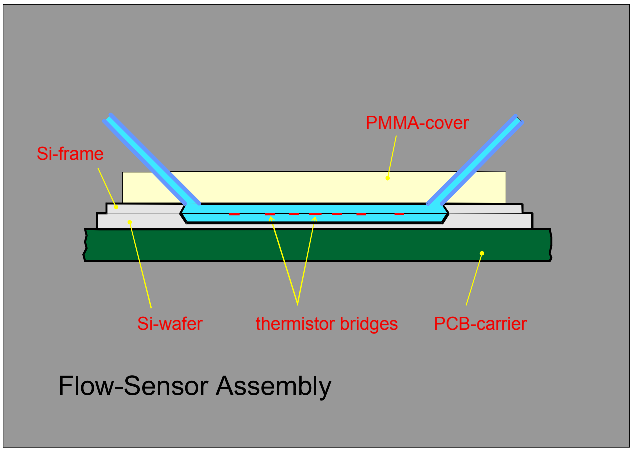

Fig. 2: Cross section of the thermistor array integrated on a micromachined silicon substrate.

Such a device is able to measure the flow of liquids from 1 ml/h to 4 l/h, and of gases from 10 sccm to 3000 sccm. However, an optimization of the flow sensor device is highly recommended for special applications.

Two typical examples are given showing different applications measuring gases and liquids. These two tasks exhibit inherent problems, and therefore two different structures and measuring systems had to be developed. First, a flow sensor for combustion engines is presented, and second, a device for measuring liquids in an implantable microvalve.

2. Experimental

2.1 Gas Flow Sensor

The air intake rate of a combustion engine is one of the key parameters needed for the combustion process optimization. Knowledge of this parameter is essential if one tries to minimize both the engine's fuel consumption and the pollution of the environment. This rate should be known for each intake stroke. For the development of such engines, high resolution monitoring of the time function of air velocity during the stroke is also desirable. The suction strokes of the engine cause a discontinuous flow of air in the induction pipe. Depending on the number of revolutions per minute and the geometry of the suction pipe, the air flow can change from simple pulsations to an oscillating flow with large amplitudes. To investigate the dynamic behavior of a suction system, a useful flow sensor must offer quick response, high sensitivity, recognition of flow direction, and a wide dynamic range. Miniaturized thermal anemometers, based on thin film Ge thermistors, show a good compromise of the mentioned characteristics. The sensitivity of the thermistor could be greatly enhanced by mounting it on a micromachined thin membrane. Due to miniaturization, a faster response to flow changes can be achieved. Flow direction could be detected using two temperature sensors placed symmetrically to a thin film platinum resistor that represents the hot wire. A cross-section of the proposed sensor structure is depicted in Fig. 3. An array of those miniaturized flow sensors can be used to average spatial variation of the flow velocity field according to turbulent flow.

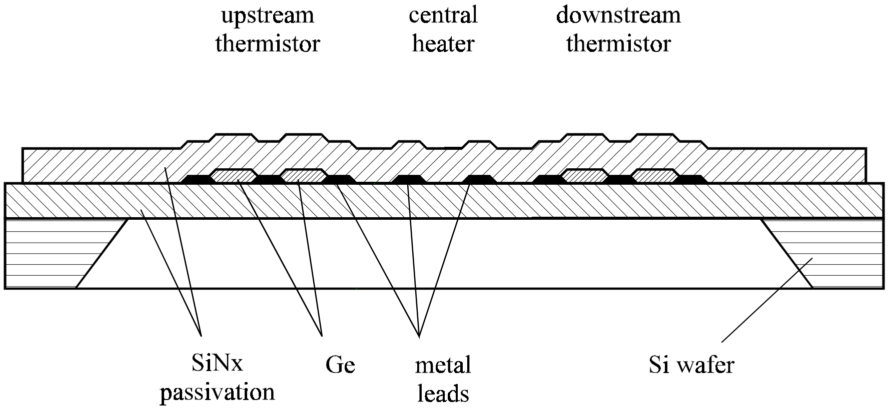

Fig. 3: Schematic cross section of the modeled flow sensor.

FE calculations were done using the ANSYS software package in order to simulate the thermal behavior and the flow dependence of the temperature field. Figure 4 depicts the temperature changes following a stepwise change of the flow velocity field. The time response and the sensitivity of the modeled structure both meet the requirements of the application. Our calculations have shown that the sensor response is determined essentially by the boundary layer of the flow. The supplied heat does not penetrate very deeply into the flowing medium, since the relevant dimensions of the sensor are smaller than or comparable to the boundary layer thickness. Fluctuations, which are typical for a turbulent flow, will be averaged very efficiently by this arrangement.

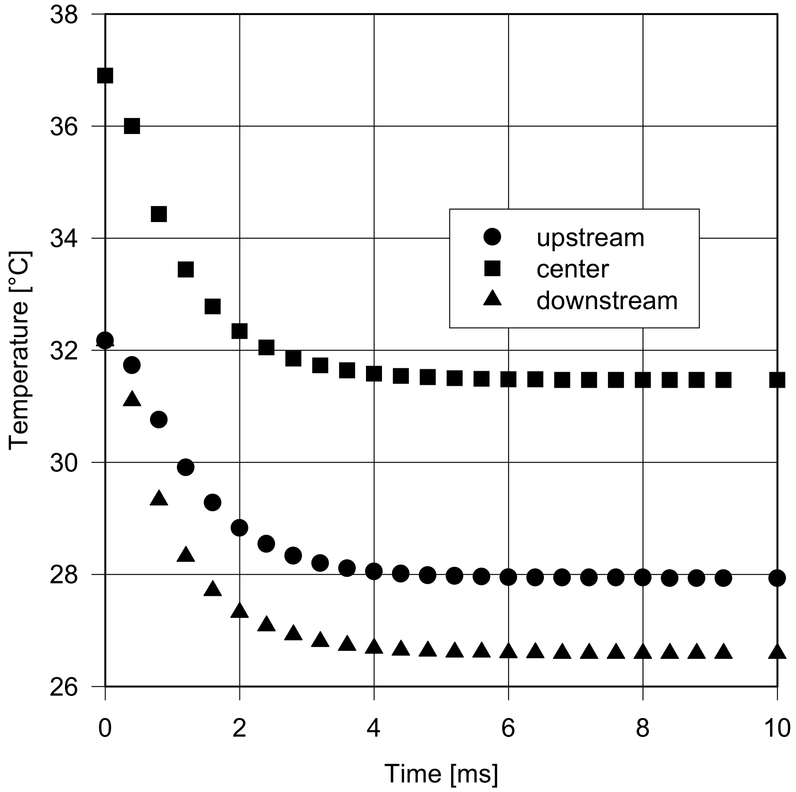

Fig. 4: Calculated time dependence of temperature following a step change of flow velocity.

2.2 Flow Sensors for Liquids

This project is a contribution to the development of a miniaturized all silicon device for the aid of patients suffering from hydrocephalus. This device should measure the intracranial pressure and automatically open a shunt for excessive liquor cerebrospinalis if required. A micro machined valve and a miniaturized flow sensor are the key parts of this device. The valve, developed by IMT Dresden, opens if the differential pressure rises above the allowed limit. The flow sensor serves for continuous monitoring as well as control functions.

The flow sensor should not hinder the free flow of liquor. Therefore we developed a micro machined Si structure which on the one hand ensures good thermal parameters for the detection of flow and on the other hand provides the desired flow channel dimensions. The outline of the flow sensor was designed to fit perfectly into the micro flow channel concept of the device. Only a very low value for the overtemperature of the flowing medium is acceptable for this application. Ge thin film thermistors offer the possibility to build very sensitive flow sensors based on the hot-wire anemometer principle. They need only slightly elevated temperatures to generate a reliable readout. We used a two-dimensional model of the sensor geometry for FE calculations of the temperature fields to simulate the flow response.

Operation safety considerations led to a design consisting of two flow sensing sites (Fig. 5). Further requirements are the recognition of the flow direction and the compensation of changes in the ambient temperature. Thus a total of six thermistors and two thin film platinum resistors for the heat generation were integrated on the sensor chip. The sensor was realized using the mask alignment equipment of the MISZ that is capable for mask adjustment related to structures on the backside of the wafer.

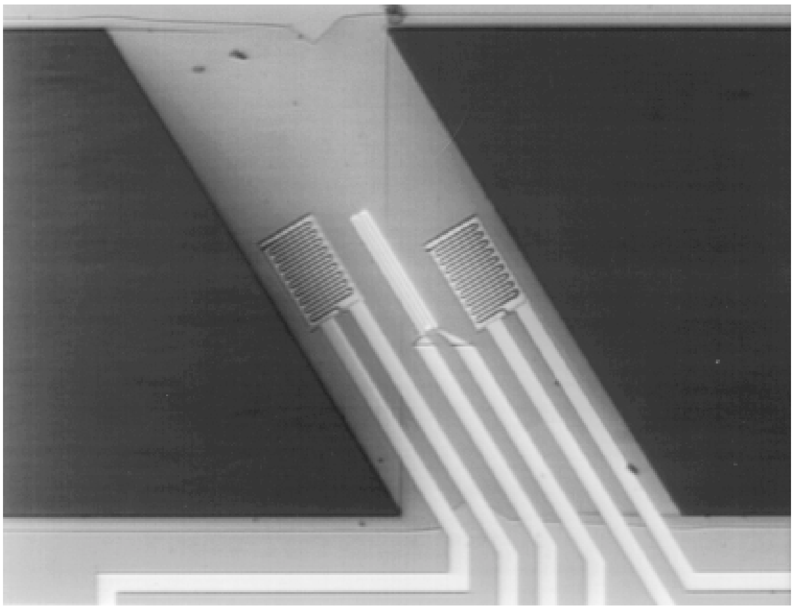

Fig. 5: A thermal flow sensor placed on a SiN_x microbridge. Flow channel width measures 1 mm. A thin film platinum resistor of 750 Ω is located in the mid of two thin film Ge thermistors with a resistance of 56 kΩ.

The flow sensor is integrated in a micromachined microvalve which can be implanted into the scull.

First samples of the sensor chip are currently under investigation at IMT Dresden and in our laboratories at the TU Vienna. It is planned to implement similar sensors in automated drug delivery devices.

3. Conclusion

The presented flow sensor arrangements are characterized by using thin film amorphous Germanium thermistor arrays and metal heating elements that are mounted in the center plane of a micromachined flow channel. Due to the insulation of the thermistors with SiN_x, the flow sensor can be used for flow sensing of gases as well as liquids. The flow dependence of the thermal conductivity was investigated by FE analysis, which is an important fact to optimize the structure due to the different applications and measuring principles.

It seems possible to design a flow sensor for a wide range of applications to match the desired dynamic range and time resolution in gases as well as in liquids.

The combination of high sensitive planar thin-film thermistors with micromachining opens the possibility to produce flow sensor devices for medical applications, process engineering and chemical engineering.

The future aim is the development of a complete analytical laboratory on chip with different integrated sensors to perform physical-chemical analysis simultaneously and directly on the measuring site.

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Biacovsky	Dalibor	dissertation	
Steurer	Johannes	assistant professor	partially GMe funded
Glatz	Ronald	technician	

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10. A. Steinschaden, Detection of HIV-antibodies by impedance spectroscopy, in preparation.

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Other Projects

Microstructure Lithography

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This project comprises three separate activities, each of which is partly related to the discontinued GMe focal-point activity on Ion Projection Lithography (IPL). The first activity made use of the GMe's ALPHA ion projector as an illumination unit for Masked Ion Beam Lithography (MIBL). The second activity involved experiments for the development of a three-level resist process that permits the indirect structuring of thick resist layers by ion beam exposure. Finally, the processes that are otherwise used for the preparation of field emitter displays were applied to the preparation of a micro-mechanical device, namely, of a dust collector for space experiments.

1. Introduction

The ALPHA ion projector, which has been developed by the Viennese company IMS and has been bought by the GMe in the late eighties, has successfully been used in the past years to demonstrate the feasibility of Ion Projection Lithography (IPL). Due to wear and aging of crucial parts of this machine, a continued operation would have required considerable repairs and investments, and did therefore not appear feasible. Consequently, the GMe decided in 1995 to sell the ALPHA ion projector back to IMS, who were entitled in the agreement to dismantle the machine.

During the past years, the focus of the attention of IMS has shifted from demagnifying IPL to 1 : 1 Masked Ion Beam Lithography (MIBL) due to the greater simplicity of the required set-up. Currently, IMS is constructing a dedicated MIBL module (access to which will be available for the GMe under the selling agreement); for first MIBL experiments, the ALPHA ion projector was used as an illumination unit during the last months of its operation.

One of the key applications of MIBL will be the preparation of emitter tips for field emitter displays where sub-micrometer structures are required over a large area. All technological processes that permit to prepare those tips require relatively thick resist layers, into which structures with a high aspect ratio have to be transferred. The energy of an ion beam is not sufficient to expose these layers over their entire thickness; a multi-level process is therefore required for structure transfer.

With a similar technique, although with electron beam rather than ion beam exposure, special microstructured surfaces for an ESA space experiment were produced for the Austrian Research Center Seibersdorf. These surfaces will be used during the RO-

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SETTA Mission to collect dust emitted from a comet; the dust particles will be imaged and classified by means of an atomic force microscope (AFM).

2. Masked Ion Beam Lithography for Proximity Printing

Optical and x-ray proximity printing systems are resolution limited by diffraction and beam dispersion. Parallel dispersion free ion beam systems are therefore ideal to transfer stencil mask patterns onto all sorts of non-ideal substrates. Figure 1 shows the schematics of a 1:1 MIBL system. Hydrogen or Helium ion beams are extracted from a suitable ion source and ExB mass separation unit. Using a proper electrostatic lens system, a parallel broad ion beam can be obtained. Ion beam induced mask heating effects can be compensated by radiation cooling using a cold tube that surrounds the mask exposure station. The virtual source size can be as small as 10 µm and, implementing proper electrostatic systems, the divergence of the ion beam illuminating a point in the stencil mask can be as low as 30 µrad. Thus, there is a penumbrial blur of only 30 nm for a gap of 1 mm between stencil mask and substrate.

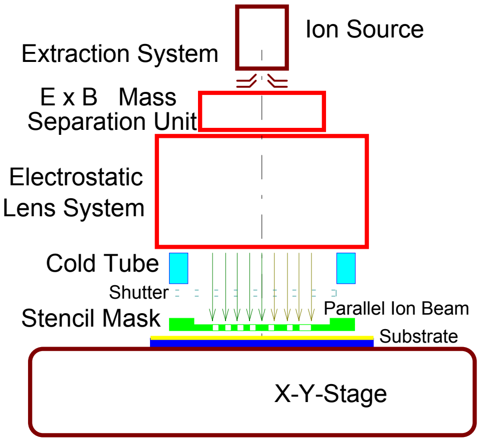

Fig. 1: Schematics of Masked Ion Beam Lithography (MIBL) stepper [1].

A feasibility study was performed with the GMe’ ALPHA ion projector operated in the MIBL (Masked Ion Beam Lithography) mode with ≈10x10 mm^2 exposure field (Fig. 2).

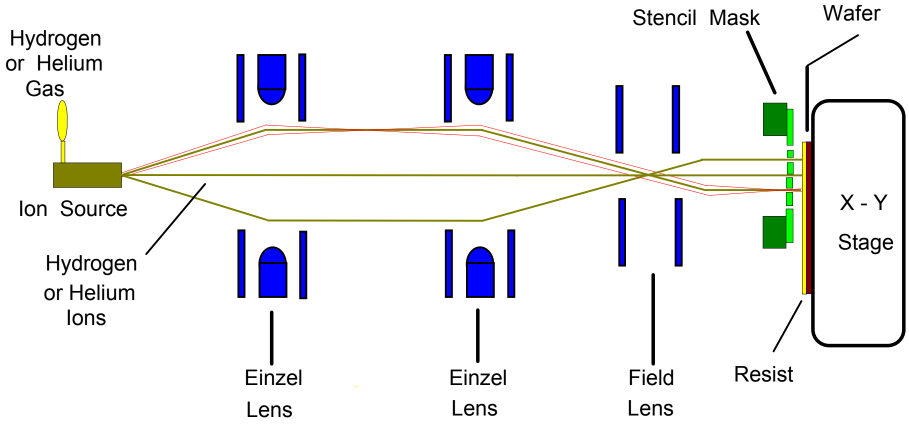

Fig. 2. ALPHA ion projector of the GMe as used in the MIBL mode [1].

Structures as small as 0.2 µm in diameter could be transferred even with a gap of 1 mm between stencil mask and substrate. The widening of resist lines with 10% increase in dose was evaluated to be 14 nm for a 2800 µm gap and 4 nm for a 300 µm gap. This excellent exposure latitude favorably compares with synchrotron based X-Ray lithography, where a widening of 20 nm with 10% overexposure has been reported for a 40 µm gap, and 10 nm for 10 µm gap.

Promising applications of the MIBL technique include the fabrication of flat panel displays based on vacuum electronics (field emitter displays), surface acoustic wave and micro-optic devices and — in combination with reactive ion etching — the fabrication of micro electro-mechanical systems (MEMS).

3. Pattern Transfer from Ni Stencil Masks onto Thick Resist

The goal of this investigation was the preparation of circularly shaped openings with a diameter of about 0.8 µm in OCG 6512 resist with a thickness of 1.2 µm. These structures are needed for the production of field emitter displays. The energy of the 55 keV H^+ ion beam produced by the ALPHA ion projector was not sufficient to expose the resist over its entire thickness. Therefore, a three-level process had to be developed: A 30 nm thick titanium layer was evaporated on the 1.2 µm thick OCG 6512 resist spun on the substrate. The titanium layer was coated with 250 nm of ion sensitive resist AZ PF 514. The 55 keV H^+ ions could fully expose this thin resist film through a galvanic overgrown Ni mask with openings down to 0.5 µm. After the exposure, the resist was wet chemically developed in undiluted AZ 518 developer. Next, the titanium layer was opened by microwave assisted reactive plasma etching with SF_6. Finally, the bottom OCG 6512 resist was plasma etched in a mixture of oxygen and CF_4. Both plasma etching processes were carried out in the Technics ECR 4000 RIE unit specially built for the TU Vienna. Figure 3 shows the relatively steep slopes in the bottom resist after the etching procedure. In order to assess the local etching rate within a hole, the etching was intentionally stopped before it reached the substrate.

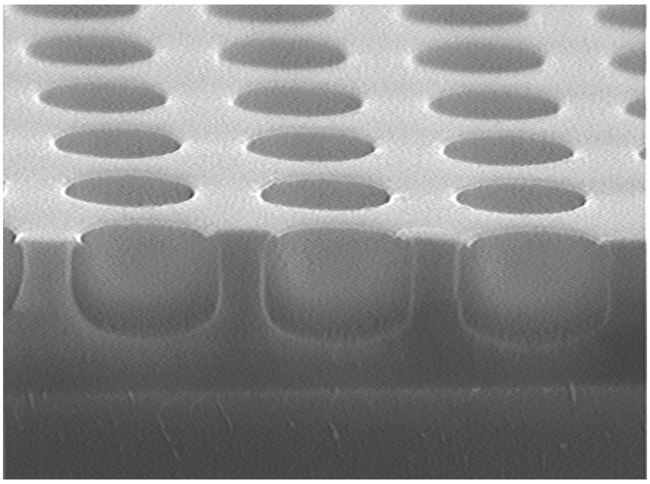

Fig. 3: Cross-section of the three-level resist after partial RIE etching of the OCG 6512.

4. Microstructures for Space Applications

For a space experiment, surfaces are required that can collect small dust particles (50 – 500 nm diameter) with high efficiency and without damage to the particles. These surfaces must convert the kinetic energy of the incoming dust particles by inelastic processes in order to avoid reflection of the particles. Free-standing columns of 0.3 µm diameter and 1.5 µm height were produced by means of electron beam lithography (Fig. 4). An impinging particle may break a number of these columns, thereby incurring an inelastic energy loss ΔE per column:

$$\Delta E = \frac{3\pi}{32} \cdot \frac{B^2 r^2 l}{M}$$

where B and M are fracture stress and modulus of the column material respectively; r and l are radius and length of the columns, respectively. The properties of these "collector surfaces" can be tailored to the particular requirements by variation of the column dimensions. By ion etching the structures of Fig. 4 into the Si substrate material it was possible to produce arrays of free-standing cones whose fracture energy is considerably lower than that of the resist columns.

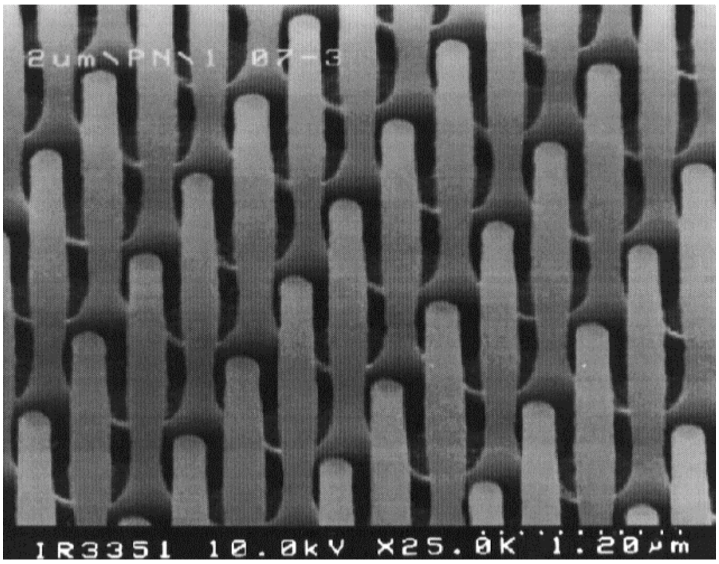

Fig. 4: Micro-columns in resist material.

Acknowledgments

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Surface Analysis for Microelectronics

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This paper demonstrates applications of surface analysis techniques for the investigation and characterization of materials and production processes. SIMS depth profile measurements of implanted erbium in silicon demonstrate that high precision measurements of low concentrations are necessary to assist implantation and simulation groups. Measurements of potassium profiles in fullerene films were done to investigate diffusion processes in order to optimize material properties.

1. Introduction

Surface analysis techniques play an important role for supporting material development and process optimization. One of the most common techniques is the Secondary Ion Mass Spectrometry (SIMS). This is due to the high detection power of the method, the fact that all elements are detectable and the possibility of registering two- and three-dimensional distributions of trace elements.

To support various investigations in the field of microelectronics, the performance of analytical methods has to be increased. The actual questions of the technology demand a permanent development of the precision of measurements, especially at very low concentrations. The supervision of the implantation process stability by measurements of depth profiles for erbium demonstrates the support of optimizing production processes. Investigation of the implanted potassium distribution in C_{60} fullerenes supplies information for the development of new materials.

2. Experimental

The ion implantation of 2 MV erbium in silicon was performed at room temperature with doses of $3{,}13 \times 10^{13}$ and $8{,}13 \times 10^{13}$ cm^{-2}. To determine the diffusion coefficient of erbium in silicon, one series of the samples was tempered at 900° C for 30 min in nitrogen.

The films of chromatographically purified C_{60} were prepared on silicon substrates by vacuum deposition. Ion implantation of 30 keV $^{39}K^+$ was performed at 300 °C in a vacuum better than 10^{-4} Pa. The depth profiles were measured using 5.5 keV O_2^+ primary ions.

3. Conclusion

The SIMS depth profiles of implanted erbium in silicon show no broadening of the erbium implantation profiles during the temperature treatment. The maximum concentration of erbium was about 2×10^{18} atoms per cm^3, the profiles were Gaussian like. The detection limit was lower than 1x10^{15} atoms per cm^3. This indicates that there is no significant diffusion of erbium at a temperature of 900° C.

Figure 1 shows the depth profile of $^{39}K^+$ for samples implanted with 30 keV K^0 at room temperature (1x10^{16} cm^{-2}) and at 300 °C (1, 3, 5 and 10x10^{16} cm^{-2}). For room temperature implantation, the experimental profile is Gaussian-like with a weak diffusion induced tail at greater depths. At 300 °C implantation temperature a peak appears in the tail region at about 100 nm, and the K-concentration within the theoretical ion range is strongly reduced. An increase of the dose leads to a subsequent increase of the peak at about 100 nm and to a slight shift of its maximum into the depth. However, with increasing dose the K concentration in this region tends to saturate at a value of about 2x10^{21} cm^{-3}. A certain amount of K diffuses out to the surface, but the diffusion into the depth is more pronounced. In all samples more than 70% of the implanted atoms are found underneath a 70 nm surface layer. Raman spectra indicate that there is a passivating a-C surface layer and the accumulation of K is at the a-C/C_{60} interface. These structures may have useful applications for the new Tc superconducting devices on the basis of fullerenes which can be handled on air [1, 2].

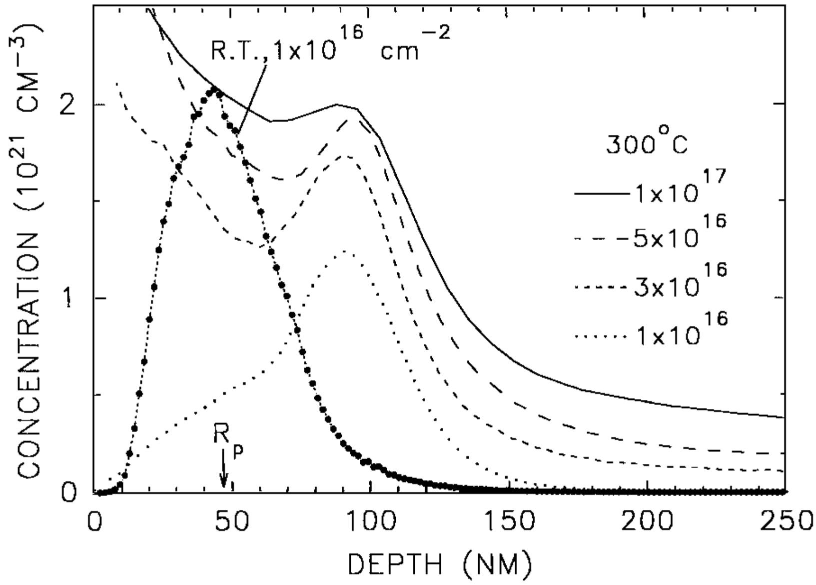

Fig. 1: SIMS potassium profiles for C_{60} films implanted with 30 keV K^+ at room temperature (1x10^{16}) and at 300 °C (1, 3, 5 and 10x10^{16} cm^{-2}).

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Brunner	Christian	dissertation	

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Scanning Probe Microscopy of Small Semiconductor Structures: A Structural Study of Polycrystalline Silicon

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The surface topography and structure of low-pressure chemical vapor deposited silicon films on thermal oxide grown on (100)-silicon substrates have been investigated on a nanometer scale by scanning force microscopy, tunneling barrier height imaging (TBI) and constant current scanning tunneling microscopy (STM). As a result we have found that surface topography and roughness are mainly determined by the deposition process. Films deposited at 620°C show a columnar structure represented by hillocks with lateral dimensions between 50 and 150 nm and surface roughness between 7 and 14 nm. Doping by high temperature diffusion and subsequent annealing causes a complete recrystallization of the film, leading to lateral grain sizes between 200 and 600 nm.

1. Introduction

Thin films of polycrystalline silicon prepared by chemical vapor deposition (CVD) are used in different applications in today's integrated circuit device technology. In addition to its use as gate electrodes of metal-oxide-semiconductor (MOS) devices and interconnections in VLSI circuits, polysilicon is being used as high-value load resistor in static RAMs, floating gates in electrically alterable ROMs (EEPROMs) and transistor emitters in bipolar technology.

Atomic force microscopy (AFM) and scanning tunneling microscopy are powerful tools for real-space surface imaging with high 3D resolution. Atomic resolution of surface structures can be achieved in a variety of fields such as biology, electrochemistry, and semiconductor materials. Additional information about electrical properties of conducting materials can be obtained in applying STM-related modulation techniques as differential conductance measurements and tunneling barrier height imaging (TBI). TBI in the case of semiconductors is very sensitive to local dopant variation induced changes of the band structure.

In the present work we report on structure and surface roughness investigations of polysilicon produced by LPCVD followed by high temperature diffusion doping, performed by contact AFM and STM measurements under ambient and high vacuum conditions. The samples have been taken from production-line test wafers, produced by high-volume equipment.

2. Experimental

2.1 The STM/AFM System

The measurements have been performed using a commercial UHV AFM/STM, with a 5 µm range tube-scanner driving the sample. Scanner calibration at atomic resolution has been performed by the manufacturer and proved by the authors for higher scan ranges using flat lithographic gratings.

The STM measurements have been performed using electrochemically etched PtIr tips with a 15° interior angle and a 50 nm radius of curvature. Commercially available silicon nitride cantilevers characterized by a 35° interior angle and 20 nm radius of curvature have been used for the contact-AFM measurements. Force calibration for individual cantilevers has been obtained by measuring force-distance curves.

2.2 Sample Preparation

The polycrystalline layers have been deposited by thermal decomposition of undiluted silane in a high-volume production LPCVD reactor at 620 °C onto (100) n-type silicon wafers covered with 100 nm of thermally grown silicon dioxide. Deposition at this temperature is known to produce a well-defined columnar structure that allows easy dopant diffusion along the grain boundaries and therefore is selected for intermediately doped layers in MOS gate electrode and interconnect applications. Ex-situ phosphorus doping has been applied to some of the wafers by gaseous predeposition using a $POCl_3$ source at 970 °C (sheet resistance 10 Ω/square) and 900 °C (15 Ω/square), followed by deglazing in buffered oxide etch (BOE). Additional selective silicon oxide etching has been applied by dipping the samples in 40% HF acid for 30 seconds.

2.3 As-Grown Layer

The low conductivity of the as-grown layer has restricted our measurements to contact-AFM. Images of the film deposited at 620 °C exhibit a fine polycrystalline structure (Fig. 1) typical for LPCVD films deposited above the amorphous-polycrystalline transition temperature [1]. The lateral dimension of the columnar crystallites represented by the bright regions of the topograph in Fig. 1 varies between 50 and 150 nm. Corrugation and surface roughness are determined by height differences of the individual crystallites and depend on the selected position on the sample. The films show a significant increase of an order of magnitude in surface roughness compared to the substrate and layers deposited under amorphous growth conditions.

2.4 Phosphorus Doped Layers

The contact-AFM picture of a layer phosphorus doped at 900 °C shows hillocks comparable in size and shape to the as-grown film in Fig. 1, but no evidence for larger size structures one might expect from the recrystallization caused by the high-temperature doping procedure. In Fig. 2, the topographic data have been numerically differentiated with respect to the lateral coordinates to enhance short-scale corrugation and have been convoluted with the topographic data. This synthetic image results in a contrast enhancement of grain boundaries and makes a well-defined lateral equiaxed structure observable. Typical lateral dimensions of the grains are 200 nm, but ranging up to 400 nm.

In layers phosphorus doped at 970°C the differentiated topograph reveals larger grain sizes up to about 600 nm.

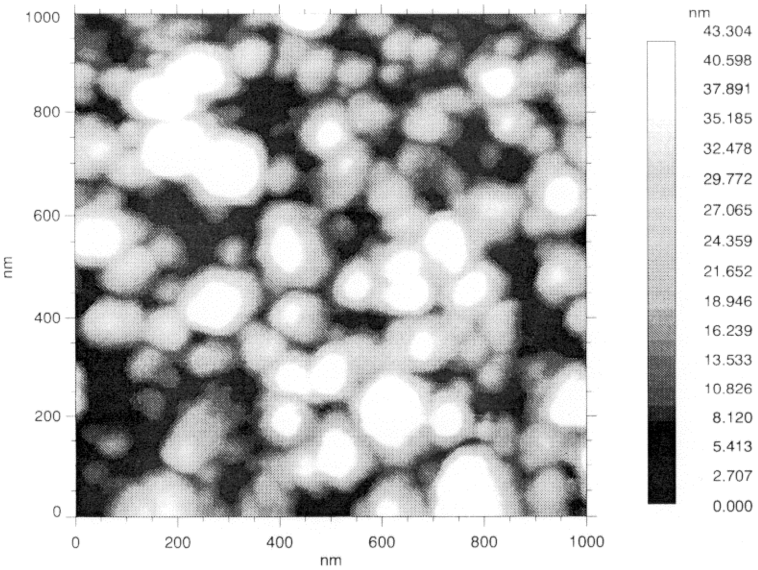

Fig. 1: Contact-AFM image of the as-grown layer

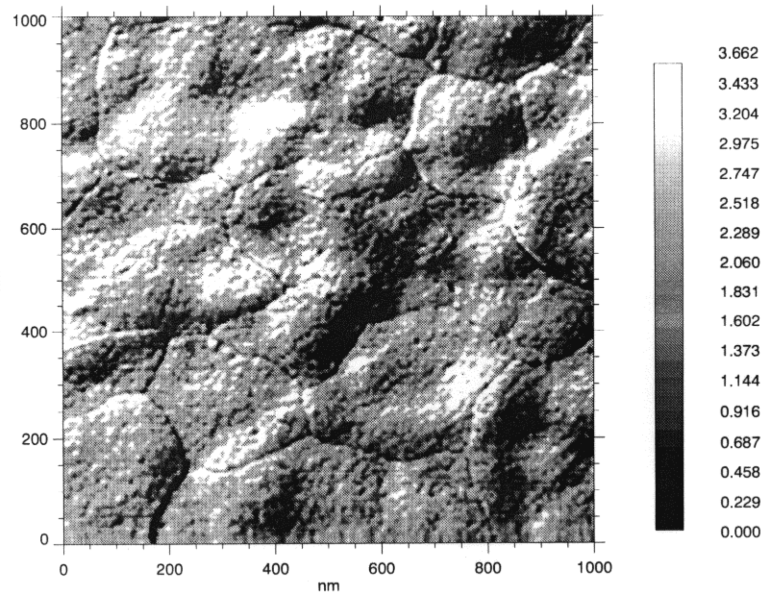

Fig. 2: Differentiated and convoluted contact-AFM image of a doped layer, showing grain boundaries

2.5 Surface Roughness Evaluation

All the measurements have been performed by contact AFM using the same silicon nitride tip. At least 20 images of 1x1 μm^2 have been acquired on several positions. Areas have been chosen randomly on each sample. Roughness values have been calculated from each image using standard software which fits a plane to the entire image, determines the deviation of each image point from this plane and calculates the arithmetic roughness R_a and root-mean-square R_{rms}. The values of the roughness are largest in the as-grown layers (R_{rms}= 13.7 nm), smaller in those doped at 970°C (8.6 nm) and 900°C (7.5 nm).

3. Conclusions

The scanning probe techniques applied in this work have proven to be superior to other techniques for surface topography and roughness determinations. It has been shown that both are essentially determined by the deposition process. Large grains anticipated to occur during the doping process at 900 – 970 °C, clearly become observable by differentiating and convoluting contact-AFM topographic data.

Acknowledgments

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Pirker	H.	technician	10% GMe
Pleschinger	A.	dissertation	

Publications in Reviewed Journals

1. A. Pleschinger, J. Lutz, F. Kuchar: "Polycristalline silicon characterization by scanning probe microscopy", *Appl. Phys. Lett.* (submitted)

Presentations

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