Internal Characterization of IGBTs Using the Backside Laserprobing Technique

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This work presents the time-resolved measurement of charge carrier concentration and temperature profiles in IGBTs by Backside Laserprobing. Calibrated numerical device simulation is employed for investigating the effects of the sample preparation on the device under test and for supporting the interpretation of the experimental results.

1. Introduction

The high operating temperature due to extensive heat dissipation has become a severe and critical issue in the optimization of modern power semiconductor devices as the blocking voltage and forward current are steadily increasing [1]. Time-resolved measurements of carrier concentration and temperature during dynamic device operation provide valuable information for the verification and calibration of the electrothermal models [2] implemented in device simulation tools. In this paper we present the thermal characterization of Insulated Gate Bipolar Transistors (IGBTs) during transient switching under shorted load conditions.

The interpretation of the results is supported by calibrated numerical device simulation. Moreover, the relevance of effects on the measurement results introduced by the sample preparation are studied by multi-cell simulation.

2. Backside Laserprobing

The Backside Laserprobing technique makes use of the dependence of the refractive index of silicon on temperature (thermo-optical effect [3]) and on carrier concentration (plasma-optical effect [4]). The modulation of the refractive index is measured by detecting the phase shift of an infrared laser beam ($\lambda = 1.3\mu m$). The laser beam propagates in vertical direction and is reflected at the top metallization layer (as illustrated in Fig. 1). Thereby, its phase is shifted by

$$\varphi(t) = 2 \cdot \frac{2\pi}{\lambda} \cdot \int_0^L \left(\frac{\partial n_{Si}}{\partial T} \Delta T(z,t) + \frac{\partial n_{Si}}{\partial n} \Delta n(z,t) + \frac{\partial n_{Si}}{\partial p} \Delta p(z,t) \right) dz, \tag{1}$$

where $\partial n_{Si}/\partial T$ is the temperature coefficient of the refractive index, $\partial n_{Si}/\partial n$ and $\partial n_{Si}/\partial p$ describe the dependence of the refractive index on the concentration of electrons and holes, respectively. ΔT, Δn and Δp are the changes of the temperature and the electron and hole density, respectively. L is the thickness of the substrate. Note that the influence of the temperature increase and the increase of the charge carrier density on the refractive index are opposite in sign.

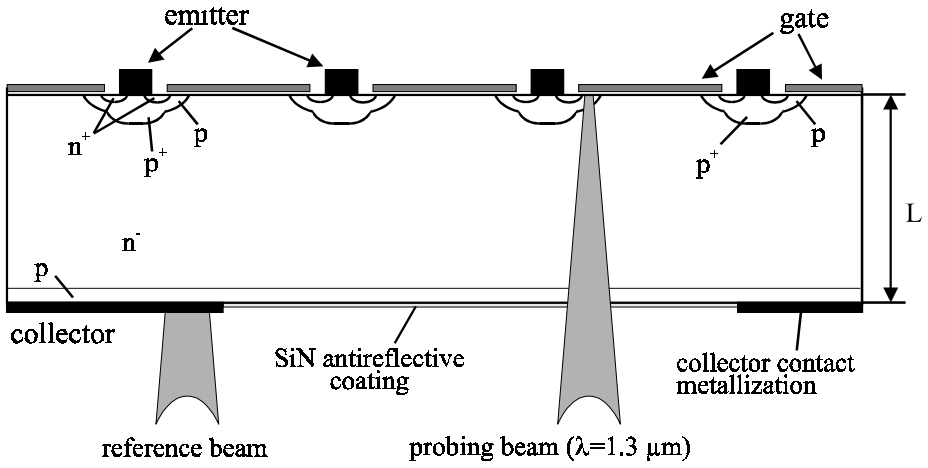


Fig. 1: Cross section view of an IGBT with probing and reference laser beam. The probing beam can be placed at different positions within the window area.

To detect the phase change we use a modified version of a heterodyne laserprober setup [5] outlined in Fig. 2. A probe and a reference beam with slightly shifted wavelengths are positioned inside and outside the device active area, respectively, as shown in Fig. 1. The lateral resolution is determined by the laser beam spot size of approximately 3 µm. The beams reflected from the device surface metallization interfere on the detector yielding a signal of the form $\sin(2\Delta\omega t+\varphi(t))$, where $\varphi(t)$ is the phase evolution according to Eq.1. The beat frequency $2\Delta\omega=2(\omega_1-\omega_2)$ determines the lateral distance of the two laser beams within the device structure and their wavelength shift. The phase signal $\varphi(t)$ is obtained from the time domain analysis of the detector signal.

The measurement technique requires to etch a window of 70 µm x 70 µm in size in the collector contact metallization. This window opening is done by a photolithographically structured etching in a two step process using HNO_3 and HF acids. Thereby, the contact metallization, which consists of a few different layers, can be removed without etching the silicon. To suppress multiple reflections within the silicon substrate (Fabry-Perot-interference), the window area is coated with an antireflective layer of Si_3N_4 by a PECVD deposition process.

The devices used in this study are vertical IGBTs with 1200 V blocking voltage. The schematics of the cross section is given in Fig. 1. The devices are operated under shorted load conditions with U_{CE} up to 500 V. Thus, operating conditions with high power dissipation as they typically occur in industrial applications can be investigated.

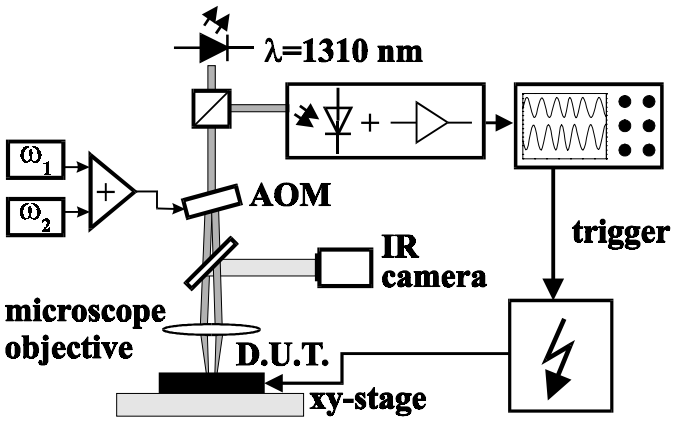


Fig. 2: Experimental setup of the Backside Laserprobing technique.

3. Numerical Modeling

For the quantitative evaluation of the experimental results, the device performance is simulated using a self-consistent electrothermal extension of the drift-diffusion model, as it is implemented in the general-purpose device simulator DESSIS^{ISE} [6]. The electrothermal models for the transport parameters have been calibrated with reference to the forward characteristics and the internal carrier concentration and temperature profile, which have been determined by Internal Laser Deflection measurements [2].

By simulating several IGBT cells, the effect of the window in the collector metallization on the device behavior is investigated. A current crowding causes a local increase of the carrier concentration at the edges of the window. Due to this current crowding the MOS structures, which can be seen through the window, feature a higher power dissipation. The resulting inhomogeneity of the lateral temperature profile is about 15% at the topside, whereas the temperature rise at the bottom due to the window preparation is negligible (see Fig.3).

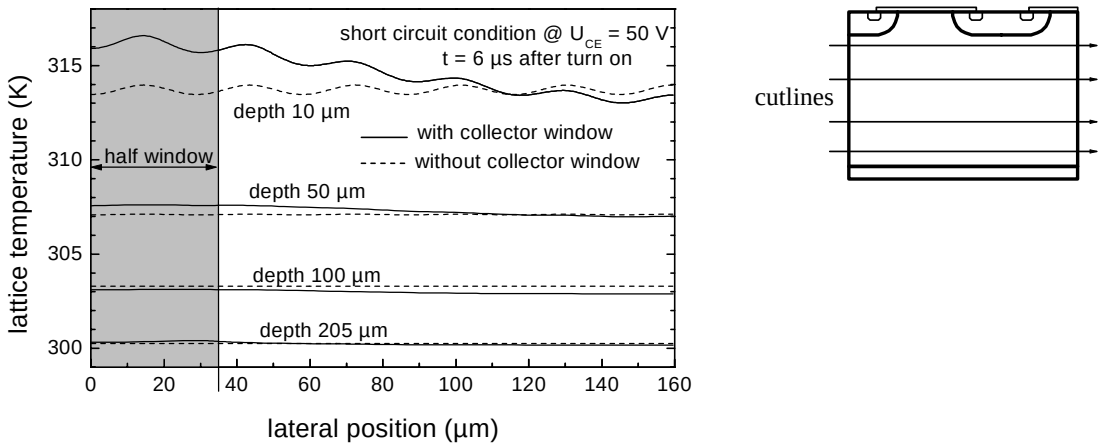
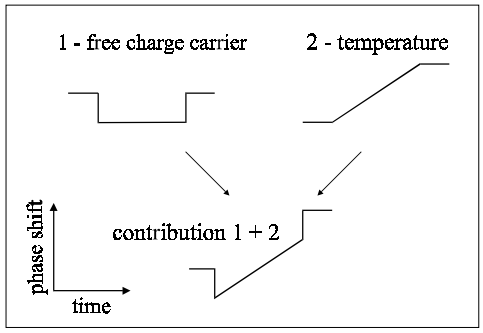


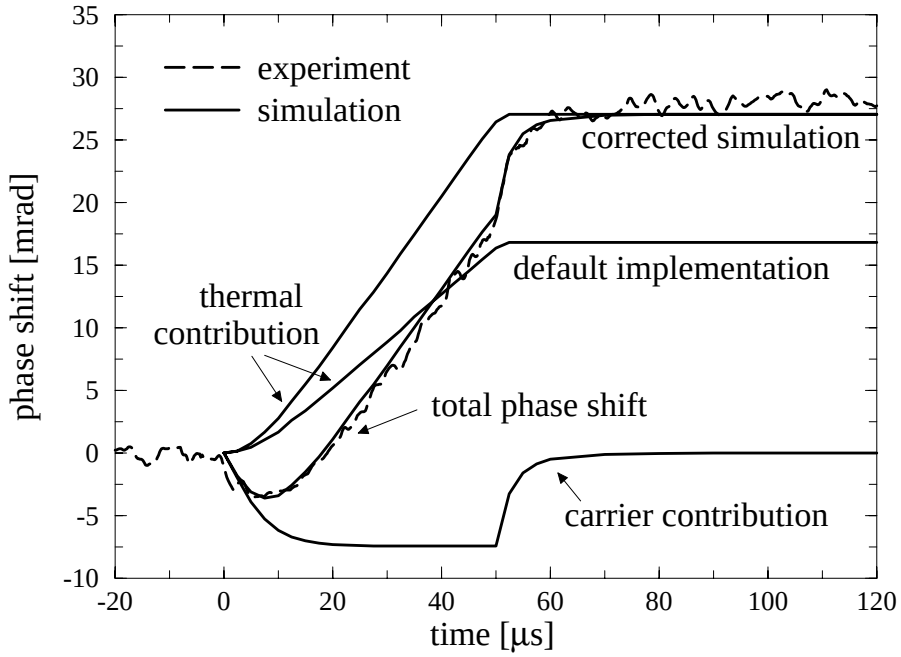
Fig. 3: Lateral temperature profiles at different depths of the prepared IGBT device (short circuit operation at U_{CE} = 50 V). Due to symmetry only one half of the structure is simulated. Thus, the center of the window is located at the lateral position of 0 µm. The schematics on the right hand side shows the 4 cutlines.

4. Experimental Results

In order to investigate the contribution of the carrier concentration on the phase shift signal, the device is investigated at low power dissipation (U_{CE} biased at 2 V). The measured phase shift for a pulse duration of $\tau = 50\ \mu s$ is shown in Fig. 4. The contributions of carrier concentration and temperature are of the same order of magnitude. When the pulse duration is increased, the contribution of the carrier concentration does not change, as the current remains unaffected. The contribution due to the temperature increase, however, changes according to the varying power dissipation.

(a)





(b)

Fig. 4: Phase shift at low power dissipation under short circuit condition ($U_{CE} = 2$ V, pulse duration $\tau = 50\ \mu s$). (a) Schematics of charge carrier and temperature contribution to the total phase shift. (b) Comparison of measured and simulated phase shift. The default implementation of the device simulator does not take into account the Peltier heating at the semiconductor/metal interface of the collector contact [7]. Adding this extra heat source yields the correct thermal contribution.

In the case of short circuit operation at high collector emitter voltages the thermal contribution becomes dominant. The phase change due to a change of the charge carrier density can be neglected. Therefore, the phase shift $\varphi(t)$ is a measure of the integral of the temperature change along the beam path.

The IGBTs are designed to withstand shorted load conditions for 10µs. According to this specification gate pulses of 15 V height and length of 10 µs are applied. The power dissipation is controlled by varying the collector emitter voltage U_{CE} between 50 and 500 V. The current is nearly independent of the applied voltage as it is confined by the MOS-structure of the IGBT. For different voltages U_{CE} the measured phase shift is shown in Fig. 5. The constant power dissipation during a current pulse causes a linear rise of the phase shift. A small increase of the phase shift is observed after pulse turn-off for about 40 µs. This is due to heat conduction from the edge of the window to the center of the window [8]. After this short time effect the cooling of the device is visible on a time scale of several 100 µs.

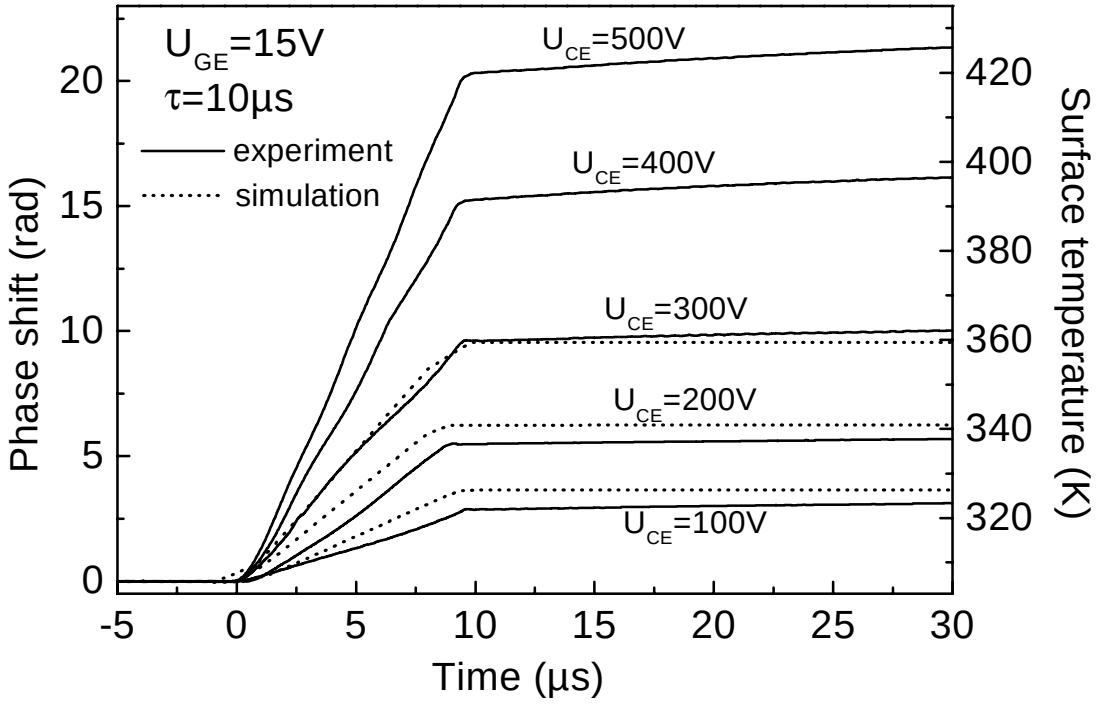


Fig. 5: Phase shift for short circuit operation at high collector emitter voltages U_{CE} with a pulse duration of 10µs. The surface temperature is calculated assuming a linear vertical temperature distribution.

The vertical temperature profile (in direction of the beam propagation) during the current pulse is dominated by the power dissipation in the channel region. Therefore, a linear decrease of the lattice temperature with increasing depth can be assumed. Thus, the phase shift can be interpreted as a measure for the maximum temperature in the device during the heating pulse (cf. scaling on the right hand side in Fig. 5). A temperature increase of $\Delta T = 120$ K is obtained at $U_{CE} = 500$ V at the end of the heating pulse. This temperature is far below the critical values assumed for latch-up, thus verifying safe operation at short circuit bias.

5. Conclusion

The internal transient behavior of vertical IGBTs under short circuit conditions has been studied by employing the Backside Laserprobing technique. Charge and temperature induced phase signals are analyzed in order to determine the temperature variation in the surface region. The influence of the preparation of the samples has been investigated by accurate numerical simulations, which have shown to be indispensable for the correct interpretation of the experimental results.

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