GaAs VCSELs with Dielectric Si_3N_4/SiO_2 Mirrors

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We present a procedure to fabricate GaAs based VCSELs utilizing Si_3N_4/SiO_2 Bragg mirrors. Current injection into the active region is defined by selective wet oxidation of AlAs. A CW threshold current of 800 µA is measured at 20 °C for a device with 5 µm square oxide aperture. The fabrication process presented here is suitable for integration of VCSELs and RCPDs.

1. Introduction

While the development of GaAs vertical-cavity lasers (VCSELs) is mainly driven by the need for optical data link products for short-haul communication, other possible applications such as laser printing and optical processing are being discussed. The field of application could be extended by developing the VCSEL technology further to include greater functionality, e.g. by integration of a resonant-cavity photodetector (RCPD).

Integration of VCSELs and RCPDs requires a technology allowing to simultaneously optimize the performance of the VCSELs and the RCPDs, whose bandwidth and responsivity are determined by the reflectivity of the incoupling mirror [1]. The need for integrating cavities with different Q factors (i.e. high Q for VCSELs and lower, adjustable Q for RCPDs) is difficult to fulfill with standard VCSEL technology using all-epitaxially grown cavities. Our approach is to use Si_3N_4/SiO_2 Bragg mirrors as top reflectors, allowing the Q factors of the RCPD cavity to be adjusted at will.

2. Sample Preparation

The VCSEL structure is an organometallic chemical vapor deposition (OMCVD) grown diode structure with a 30-periods AlGaAs/AlAs Bragg mirror stack on the substrate side. The 7λ/4-cavity contains three GaAs quantum wells separated by $Al_{0.2}Ga_{0.8}As$ barriers. $Al_{0.5}Ga_{0.5}As$ spacer layers are added on both sides to achieve efficient carrier confinement. The cavity is completed by a 30 nm AlAs oxidation layer embedded in $Al_{0.9}Ga_{0.1}As$, followed by 112 nm $Al_{0.2}Ga_{0.8}As$ and a 10 nm highly p-doped GaAs cap layer to obtain ohmic contacts and homogenous current spreading into the active region.

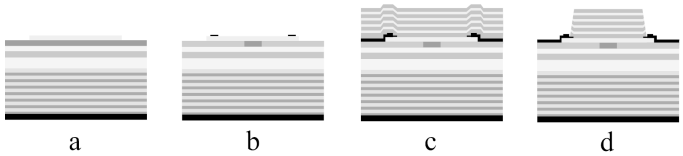

Fig. 1: Cross-sectional view of an oxidized GaAs VCSEL with Si_3N_4/ SiO_2 top mirror.

A broad area Sn/Au contact is deposited at the backside of the substrate and annealed at 380 °C. The top layers are etched to form shallow square mesas exposing the AlAs oxidation layer (Fig. 1a) which is subsequently oxidized in a furnace set at 520 °C (Fig. 1b). *In situ* optical monitoring is used to stop the oxidation process. Electrical contact is made to the p-type GaAs surface using Cr/Au metallization (Fig. 1c). The top Bragg mirror is deposited by plasma enhanced chemical vapor deposition (PECVD) and consists of 16 pairs Si_3N_4/ SiO_2 (Fig. 1c). It has already been shown that these mirrors meet the demands on reflectivity for use in VCSELs [2]. A two-step etching process is used to pattern the top mirror (Fig. 1d): the first step, Ar-ion etching, is stopped approximately 50 nm above the metallization, the remaining dielectric is then removed in a reactive ion etch process which exposes the extended contacts of the devices.

RCPDs with an area of 50 µm square were integrated beside the VCSELs, but have not been investigated so far. Tuning the RCPDs to the desired bandwidth and responsivity can be accomplished by removing excessive mirror pairs in a further etch step.

3. Performance of the VCSELs

Figure 2 shows the CW-output characteristics of a VCSEL with a 5 µm square oxide aperture at room temperature. Threshold current (800 µA) is comparable to that of all-epitaxial devices [3], but due to the high drive voltage, wallplug efficiency does not exceed 7.4 %.

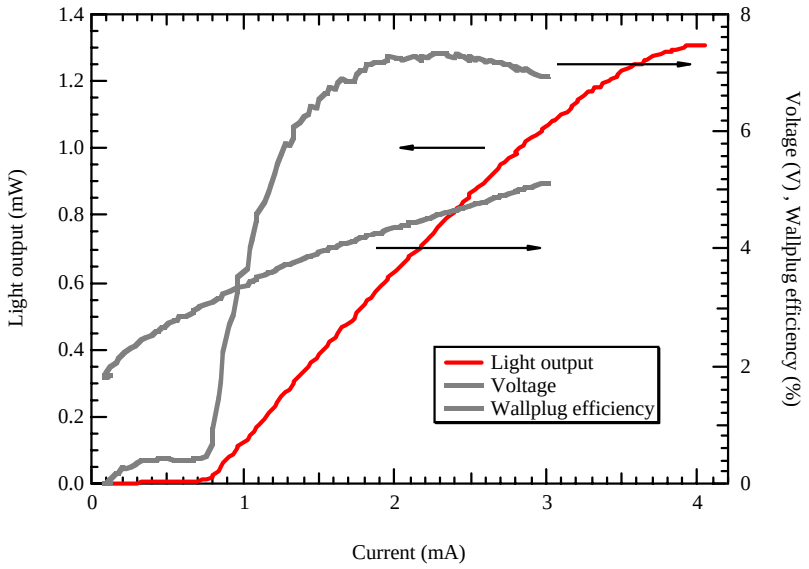

Fig. 2: Output characteristics of a 5 µm square GaAs VCSEL.

Because of the lateral current injection into the active zone, a high differential resistance is expected to be inherent in these devices [4], but we believe that the extremely high value of 920 Ω is partially caused by the technology used to fabricate the samples: we noticed that the GaAs cap layer was visibly attacked by an unplanned HCl dip which had become necessary to improve the sticking properties of the photoresist on the sample. The removal of the cap layer could well account for the poor conductive properties of the diode. A numerical simulation of the cavity shows that the resonance wavelength

is blue shifted by approximately 6 nm if the cap layer is missing. This is in good agreement with the observed laser wavelength of 843.5 nm as opposed to the design wavelength of 850 nm.

In Fig. 3, optical output characteristics for CW operation are shown for various temperatures. Despite the mismatch between resonance wavelength and spectral gain maximum, lasing action continues up to an operating temperature of 90 °C, threshold current increases from 750 µA at –10 °C to 2 mA at 90 °C.

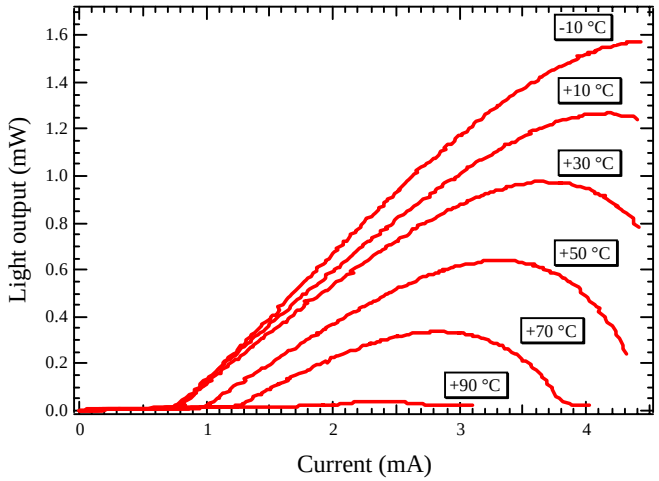

Fig. 3: Light output versus current of a 5 µm square GaAs VCSEL at different temperatures.

Due to the smaller temperature coefficients of the refractive index of Si_3N_4 and SiO_2 as compared to the GaAs/AlAs material system, the lasing wavelength of our VCSELs shows a smaller temperature dependence (Fig 4) than all-epitaxial devices [3], [4]. The spectral shift of the emission wavelength is 0.045 nm/K. The shift due to dissipated power is evaluated to 0.092 nm/mW, resulting in a thermal resistance of 2.04 K/mW.

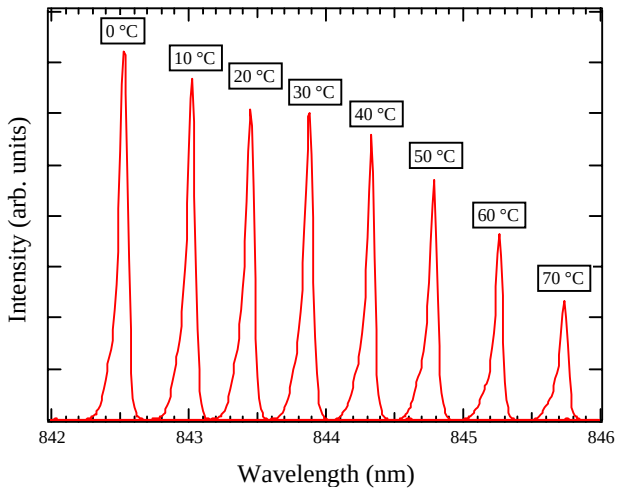

Fig. 4: Temperature dependence of the emission wavelength of a 5 µm square VCSEL. The linewidth is resolution limited.

We further investigated the influence of the oxide aperture on the transverse lasing mode. Fig. 5 shows the nearfield patterns of 7 and 5 µm VCSELs. The strong index guiding of the oxide aperture causes the 7 µm devices to lase in the TEM_{11}-mode. Aperture sizes of 5 µm or smaller are required to maintain lasing in the fundamental TEM_{00}-mode throughout the observed pumping range.

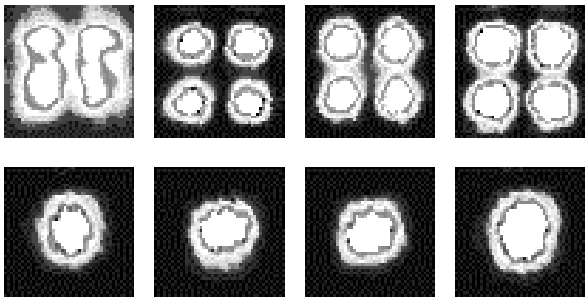

Fig. 5: Nearfield patterns of a 7 µm (top) and 5 µm (bottom) square oxide aperture VCSEL at different pumping levels. (1.5 mA, 2 mA, 3 mA and 4 mA (from left to right).

4. Conclusion

We described the fabrication of GaAs based VCSELs incorporating PECVD deposited Si_3N_4/SiO_2 top Bragg mirrors. This process is suitable for the integration of VCSELs and RCPDs. In CW operation at 20 °C threshold currents of 800 µA and wallplug efficiencies of 7.4 % were achieved in devices with 5 µm oxide aperture. Maximum light output power is 1.3 mW. Both the temperature coefficient of the emission wavelength (0.045 nm/K) and the thermal resistance (2.04 K/mW) are significantly smaller than in all-epitaxial devices.

Acknowledgements

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