GMe

Gesellschaft für Mikroelektronik

The Society for Microelectronics

Annual Report

1998

Vienna, April 1999

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c/o Technische Universität Wien Institut für Angewandte Elektronik und Quantenelektronik Gußhausstraße 27-29/359, A-1040 Wien

Vienna, April 1999

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The Society for Microelectronics (GMe — Gesellschaft für Mikroelektronik)

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1. Goals of the Society for Microelectronics

The Society for Microelectronics (GMe) was founded in 1985 with the aim to "support microelectronics technology and its applications" in Austria. The GMe defines its tasks as follows:

- Support of university-based "high-tech" research in the areas of microelectronics, semiconductor technology, sensors, and opto-electronics;
- Operation of research facilities;
- Support and consulting for industry, in particular, for small and medium enterprises, within the area of microelectronics.

The central task of the GMe is to provide an internationally competitive *infra-structure* in the area of microelectronics technology. The GMe allocates funds to maintain research projects in the fields of semiconductor technology, sensors, opto-electronics, and ASIC design. Thus the infra-structure support generates a base for research projects that are funded by other funding agencies.

2. Activities of the Society

The present focal point activities of the GMe are:

- Operation of university-based laboratories for microelectronics technology;
- Design of application specific integrated circuits (ASICs) —TMOe.

The GMe currently supports mainly the first focal point activity but also coordinates the Austria-wide activities of the TMOe program.

The main task of the GMe in the area of microelectronics technology is the operation of the cleanroom laboratories in Vienna and Linz. The GMe has coordinated the construction of the Microstructure Center (MISZ — Mikrostrukturzentrum) in Vienna; the funds were supplied by the Austrian Federal Ministry of Science and Research. The GMe now finances a significant part of the operation costs for the cleanroom laboratories in Vienna and Linz.

2.1 Microelectronics Technology — Cleanroom Vienna

The following university institutes receive support within this focal point activity:

- TU Wien:
 - Institut für Festkörperelektronik
 - Institut für Allgemeine Elektrotechnik und Elektronik

2.2 Microelectronics Technology — Cleanroom Linz

The following university institutes receive support within this focal point activity:

- Johannes Kepler Universität Linz:
 - Institut für Halbleiterphysik
 - Institut für Experimentalphysik
 - Institut für Mikroelektronik

3. Other Activities of the Society

One of the declared tasks of the GMe is to provide information on current Austrian academic activities in the field of microelectronics to industry, in particular to Austrian small- and medium enterprises (SMEs). This will improve the transfer of "know-how" between Austrian universities and industry. As an example, the GMe supplied editorial articles to an Austrian publishing house that targets its magazines on the management and technical staff of Austrian industrial enterprises. The articles presented some of those projects supported by the GMe that had a direct impact on Austrian industry.

To enhance the distribution of the results of the research work done with GMe support, the GMe has put the contents of its previous annual reports — 1995 through 1997 — on its Web server; this will also happen for this report. Although we did not explicitly advertise on a larger scale the existence of this server and its contents, it has apparently been fairly well accepted by the international community. Access statistics show an average access of 3 counts per day; however, an amazingly large percentage of these accesses — close to 50 per cent — originates from net domains outside Austria. About one quarter of the visitors of the GMe's web site visited it more than once. The GMe Web server is available under the URL:

http://www.iaee.tuwien.ac.at/gme/

Finally, the GMe prepared and carried out the biennial seminar "Aktuelle Entwicklungen der Mikroelektronik" in Bad Hofgastein, Salzburg, which took place in March 1999. The predecessor of this seminar has first been held in 1977 in Großarl; since 1987, the GMe contributes financial support, and since 1993, the Society acts as its main organizer. The seminar presented thirteen invited lectures given by international experts, and 25 oral and poster contributions which resulted from work supported by the GMe. The program of this seminar is included in the appendix of this report. For the first time, greater emphasis was put into making the seminar more attractive to an industrial audience, thus intending an enhanced knowledge transfer between universities and industry.

4. The Annual Report for 1998 of the Society for Microelectronics

The GMe is currently supporting the microelectronics technology activities of the cleanroom laboratories in Vienna and Linz.

All projects described in this report were carried out in the cleanrooms in Vienna and Linz, respectively. They are *not* specific projects of the GMe but were funded by a variety of other sources. They all have in common that they use the infra-structure provided by the GMe. It would therefore not have been possible to carry out these projects without the support by the GMe.

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Microelectronics Technology — Cleanroom Vienna

Cleanroom Vienna

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We report on the main activities in the cleanroom of the MISZ (microstructure center). The cleanroom of the MISZ was opened 1993; during 1994, most of the equipment for the production of semiconductor devices was installed. Since 1995, state of the art growth of III–V compounds as well as the production of patterned masks used in lithography is done on a regular basis. In spring 1998 state of the art Silicon processing has been added as an additional material system. This activity is starting up and may need further support to mature. A short description of projects with a high content of technological input in our institute is given.

One of the main research areas of this institution is the preparation and characterization of III–V devices. Therefore the MISZ, namely the fke, maintains several collaborations with national and international research institutions and companies by providing them with epitaxial layers (III–V compounds). A second main research topic is the production of micron and sub-micron devices down to nanometer scale. Patterned masks for optical lithography are provided to different institutions.

1. Introduction

Since 1995, the cleanroom of the MISZ is running on a regular basis. Main research areas are the state of the art growth of III-V compounds and the production of patterned masks. Testing of the cleanroom quality and adjustment (laminar air flow, filters, cooling, humidity...) if necessary is done periodically.

The cleanroom contains all major components for semiconductor device processing (both on silicon and GaAs basis) and is equipped with a conventional photolithography including a mask fabrication facility, e-beam lithography for nm structures, evaporation chambers, an ion milling chamber, and a plasma etching and plasma deposition chamber in master-slave configuration.

In 1998, the following additional equipment was installed :

- an RF sputtering chamber for deposition of metals and dielectric materials;
- a focussed ion beam ("FIB") writer;
- an additional wet bench was installed for chemical processes.

The RF sputtering chamber is mainly used for the deposition of dielectric mirrors, which are necessary for the fabrication of surface emitting lasers.

The FIB writer is currently the ultimate tool in nanofabrication technology. This machine is basically a scanning ion microscope (similar to a scanning electron microscope) with the additional abilities to deposit arbitrary metal structures in the deep sub- μ m regime and to etch holes in predefined deep sub- μ m geometries.

In the following chapters, the main research activities making use of the cleanroom itself or using samples grown, structured and tested in the MISZ are described. These activities are not the only projects running in the MISZ, but are intended to show a representative overview on basic research as well as applied projects using the existing equipment. For a more general overview the added project information, specially the attached publication list from the last year, may give some insides on the broad range of activities.

Project Information

Project Manager

Dr. Gottfried STRASSER

Institut für Festkörperelektronik, Technische Universität Wien

Project Group

Last Name	First Name	Status	Remarks
Bertagnolli	Emmerich	Full Prof.	
Boxleitner	Winfried	Post Doc	
Bratschitsch	Rudolf	dissertation	
Finger	Norman	dissertation	
Fuchshuber	Michael	student	
Fürböck	Christoph	dissertation	
Gianordoli	Stefan	dissertation	
Gornik	Erich	Full Prof.	
Haider	Manfred	student	
Heer	Rudolf	dissertation	
Hirner	Heimo	student	
Hobler	Gerhard	Assistant Prof.	
Hoffmann	Rainer	student	
Hvozdara	Lubos	dissertation	
Kast	Michael	student	
Kellermann	Peer Oliver	dissertation	
Kersting	Roland	Post Doc	
Kröll	Peter	technician	
Lampacher	Peter	student	
Langmann	Gottfried	technician	
Litzenberger	Martin	dissertation	
Lugstein	Alois	assistant	
Maier	Thomas	dissertation	
Pacher	Christoph	dissertation	
Patz	Sybille	student	
Ploner	Guido	dissertation	
Pogany	Dionyz	guest scientist	
Prinzinger	Johannes	technician	

Last Name	First Name	Status	Remarks
Rakoczy	Doris	dissertation	
Rauch	Christoph	dissertation	
Riegler	Erich	technician	
Schenold	Helmut	technician	
Schrenk	Werner	dissertation	
Smola	Winfried	student	
Smoliner	Jürgen	Assistant Prof.	
Stöckl	Herbert	technician	
Strasser	Gottfried	Assistant Prof.	
Thaller	Edwin	student	
Ulrich	Jochen	dissertation	
Unterrainer	Karl	Assistant Prof.	
Wanzenböck	Heinz	assistant	
Zobl	Reinhard	dissertation	

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GaAs VCSELs with Dielectric Si₃N₄/SiO₂ Mirrors

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We present a procedure to fabricate GaAs based VCSELs utilizing Si₃N₄/SiO₂ Bragg mirrors. Current injection into the active region is defined by selective wet oxidation of AlAs. A CW threshold current of 800 μ A is measured at 20 °C for a device with 5 μ m square oxide aperture. The fabrication process presented here is suitable for integration of VCSELs and RCPDs.

1. Introduction

While the development of GaAs vertical-cavity lasers (VCSELs) is mainly driven by the need for optical data link products for short-haul communication, other possible applications such as laser printing and optical processing are being discussed. The field of application could be extended by developing the VCSEL technology further to include greater functionality, e.g. by integration of a resonant-cavity photodetector (RCPD).

Integration of VCSELs and RCPDs requires a technology allowing to simultaneously optimize the performance of the VCSELs and the RCPDs, whose bandwidth and responsivity are determined by the reflectivity of the incoupling mirror [1]. The need for integrating cavities with different Q factors (i.e. high Q for VCSELs and lower, adjustable Q for RCPDs) is difficult to fulfill with standard VCSEL technology using allepitaxially grown cavities. Our approach is to use Si_3N_4/SiO_2 Bragg mirrors as top reflectors, allowing the Q factors of the RCPD cavity to be adjusted at will.

2. Sample Preparation

The VCSEL structure is an organometallic chemical vapor deposition (OMCVD) grown diode structure with a 30-periods AlGaAs/AlAs Bragg mirror stack on the substrate side. The $7\lambda/4$ -cavity contains three GaAs quantum wells separated by Al_{0.2}Ga_{0.8}As barriers. Al_{0.5}Ga_{0.5}As spacer layers are added on both sides to achieve efficient carrier confinement. The cavity is completed by a 30 nm AlAs oxidation layer embedded in Al_{0.9}Ga_{0.1}As, followed by 112 nm Al_{0.2}Ga_{0.8}As and a 10 nm highly p-doped GaAs cap layer to obtain ohmic contacts and homogenous current spreading into the active region.



Fig. 1: Cross-sectional view of an oxidized GaAs VCSEL with Si₃N₄/ SiO₂ top mirror.

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A broad area Sn/Au contact is deposited at the backside of the substrate and annealed at 380 °C. The top layers are etched to form shallow square mesas exposing the AlAs oxidation layer (Fig. 1a) which is subsequently oxidized in a furnace set at 520 °C (Fig. 1b). *In situ* optical monitoring is used to stop the oxidation process. Electrical contact is made to the p-type GaAs surface using Cr/Au metallization (Fig. 1c). The top Bragg mirror is deposited by plasma enhanced chemical vapor deposition (PECVD) and consists of 16 pairs Si₃N₄/SiO₂ (Fig. 1c). It has already been shown that these mirrors meet the demands on reflectivity for use in VCSELs [2]. A two-step etching process is used to pattern the top mirror (Fig. 1d): the first step, Ar-ion etching, is stopped approximately 50 nm above the metallization, the remaining dielectric is then removed in a reactive ion etch process which exposes the extended contacts of the devices.

RCPDs with an area of 50 μ m square were integrated beside the VCSELs, but have not been investigated so far. Tuning the RCPDs to the desired bandwidth and responsivity can be accomplished by removing excessive mirror pairs in a further etch step.

3. Performance of the VCSELs

Figure 2 shows the CW-output characteristics of a VCSEL with a 5 μ m square oxide aperture at room temperature. Threshold current (800 μ A) is comparable to that of all-epitaxial devices [3], but due to the high drive voltage, wallplug efficiency does not exceed 7.4 %.



Fig. 2: Output characteristics of a 5 µm square GaAs VCSEL.

Because of the lateral current injection into the active zone, a high differential resistance is expected to be inherent in these devices [4], but we believe that the extremely high value of 920 Ω is partially caused by the technology used to fabricate the samples: we noticed that the GaAs cap layer was visibly attacked by an unplanned HCl dip which had become necessary to improve the sticking properties of the photoresist on the sample. The removal of the cap layer could well account for the poor conductive properties of the diode. A numerical simulation of the cavity shows that the resonance wavelength is blue shifted by approximately 6 nm if the cap layer is missing. This is in good agreement with the observed laser wavelength of 843.5 nm as opposed to the design wavelength of 850 nm.

In Fig. 3, optical output characteristics for CW operation are shown for various temperatures. Despite the mismatch between resonance wavelength and spectral gain maximum, lasing action continues up to an operating temperature of 90 °C, threshold current increases from 750 μ A at -10 °C to 2 mA at 90 °C.



Fig. 3: Light output versus current of a 5 µm square GaAs VCSEL at different temperatures.

Due to the smaller temperature coefficients of the refractive index of Si_3N_4 and SiO_2 as compared to the GaAs/AlAs material system, the lasing wavelength of our VCSELs shows a smaller temperature dependence (Fig 4) than all-epitaxial devices [3], [4]. The spectral shift of the emission wavelength is 0.045 nm/K. The shift due to dissipated power is evaluated to 0.092 nm/mW, resulting in a thermal resistance of 2.04 K/mW.



Fig. 4: Temperature dependence of the emission wavelength of a 5 µm square VCSEL. The linewidth is resolution limited.

We further investigated the influence of the oxide aperture on the transverse lasing mode. Fig. 5 shows the nearfield patterns of 7 and 5 μ m VCSELs. The strong index guiding of the oxide aperture causes the 7 μ m devices to lase in the TEM₁₁-mode. Aperture sizes of 5 μ m or smaller are required to maintain lasing in the fundamental TEM₀₀-mode throughout the observed pumping range.



Fig. 5: Nearfield patterns of a 7 μm (top) and 5 μm (bottom) square oxide aperture VCSEL at different pumping levels. (1.5 mA, 2 mA, 3 mA and 4 mA (from left to right).

4. Conclusion

We described the fabrication of GaAs based VCSELs incorporating PECVD deposited Si_3N_4/SiO_2 top Bragg mirrors. This process is suitable for the integration of VCSELs and RCPDs. In CW operation at 20 °C threshold currents of 800 µA and wallplug efficiencies of 7.4 % were achieved in devices with 5 µm oxide aperture. Maximum light output power is 1.3 mW. Both the temperature coefficient of the emission wavelength (0.045 nm/K) and the thermal resistance (2.04 K/mW) are significantly smaller than in all-epitaxial devices.

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GaAs/AlGaAs/InGaAs Bandgap Lasers — From DH Lasers to VCSELs

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Starting from the growth of double hetero (DH) semiconductor bandgap lasers, in the material system AlGaAs/GaAs we are now optimizing laser devices such as a twin waveguide laser and a laser interferometer based on vertical cavity surface emitting lasers (VCSEL).

1. MBE

MBE (molecular beam epitaxy) technique allows the epitaxial growth of different compounds. One of the model materials for optoelectronics are epitaxial layers of III-V semiconductors, mainly GaAs and related compounds. The controlled growth of single crystalline layers on an atomic scale makes it possible to design new materials with optimized electrical and optical characteristics. A solid source MBE system (MOD GEN II) is used for the growth of AlGaAs/GaAs semiconductor lasers and InGaAs quantum well lasers; thus, this machine is further equipped with an indium cell. As doping materials we use silicon for n-doping and carbon for p-doping.

2. Lasers

We started laser growth with double hetero (DH) GaAs/AlGaAs laser structures. This material was characterized by processing broad area lasers and measuring their electrical and optical properties. The threshold current density and differential efficiency are comparable to lasers processed from industrial grown materials [1].





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As a next step, ridge lasers were processed out of DH material. The ridge forms a lateral optical waveguide, which allows the realization of single mode lasers, where in addition a longitudinal mode control is needed. A simple model for calculating the lateral optical waveguide is the effective index model. The difference of the effective transverse refractive index and the width of the ridge determines how many lateral waveguide modes are possible and the divergence of the facet emission in lateral direction. Based on the ridge laser design we started to manufacture "single mode lasers" by incorporating a longitudinal mode control via a 4th order dfb (distributed feed back) grating. The reason for choosing a 4th order grating (period 515 nm) at this time was the established holographic grating definition with our HeCd laser setup for this grating period. The measured lasers showed a drift in the emission wavelength of about 0.05 nm/K, as can be seen in Fig. 1 (linewidth limited by the used spectrometer) due to change of the refractive index with temperature, which is in good agreement with literature [2].

As a next step, InGaAs SQW (single quantum well) lasers with separate confinement layers were grown. Strained InGaAs QWs show higher peak material gain than unstrained QWs or bulk material. The lattice mismatch between GaAs and InGaAs determines the so-called critical thickness for InGaAs layers on GaAs. Layers thinner than the critical thickness can be grown without relaxation effects. There are different models for calculating the critical thickness, e.g. by Matthews and Blakeslee or People and Bean [3]. One difficulty in the growth of strained InGaAs layers on GaAs is the calibration of In content and growth rate with RHEED (reflected high energy electron diffraction) measurements, originating from the lattice mismatch of the two materials. Additionally, optical problems remain in InGaAs QW lasers due to the large antiguiding effect and the nonlinear gain behavior at high current densities. E.g. the current density for narrow gain guided lasers increases dramatically for widths below 20 µm [3]. Therefore, a relatively strong index guiding is needed for narrow lasers. The grown SQW material was characterized with broad area lasers and showed threshold densities comparable to state of the art lasers [4], [5]. Ridge lasers with widths from 2 µm to 6 µm show kink-free light output (fig. 2) up to current densities of 5 times threshold density (limited by the setup) and the measured far field pattern indicates that only one lateral mode exists.



Fig. 2: Emitted power versus injected current of an InGaAs SQW laser (ridge width $4 \mu m$).

Currently we are working on two laser projects, a twin waveguide laser and a laser interferometer.

2.1 Twin waveguide laser

The goal of this project is the realization of a grating coupled twin waveguide laser, where the two waveguides are the active laser waveguide and a passive waveguide formed by Au/SiO/SiN. The waveguide are coupled via a surface relief grating atop of the semiconductor (Fig. 3). These lasers allow postprocessing wavelength adjustment and high side mode suppression [6].



Fig. 3: Twin waveguide laser schematic.



Fig. 4: SEM picture of 190 nm period grating etched into GaAs (photoresist removed)

The use of diluted photoresist (thickness 50 nm) allows us to produce grating periods as small as 180 nm holographically with a HeCd laser (lower limit for grating period:

325 nm/2 = 162.5 nm) in standard resist material. The used InGaAs QW laser material for the twin waveguide laser is designed for emission at about 980 nm, thus needing a grating period of about 190 nm, which is accessible with our setup as shown in Fig. 4.

2.2 Laser interferometer

The realization of a laser interferometer, consisting of a VCSEL and a detector integrated on one chip is the final goal of this project. At the beginning, Bragg mirrors consisting of GaAs and AlAs layers were grown and characterized by reflection measurement and layer thickness measured by scanning tunneling microscope (Fig. 5).



Fig. 5: STEM picture of AlAs/GaAs Bragg mirror.

The first VCSEL structures we realized consist of an upper dielectric Bragg mirror – made of SiO/SiN in a PECVD (plasma enhanced chemical vapor deposition) system – deposited on an MBE grown active region and a lower AlGaAs/AlAs Bragg mirror. These lasers showed single mode emission at room temperature but relatively broad linewidth [7]. Improvements are achieved by using a selective oxidation technique to reduce problems with current spreading and QWs as active region.

3. Conclusion

We started the growth of AlGaAs/GaAs bandgap lasers and were able to realize DH structure laser, strained InGaAs QW lasers and VCSELs which are state of the art, and in the near future we are going to realize new single mode lasers and an integrated laser interferometer.

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Wavelength Adjustable Surface Emitting Single Mode Laser Diodes with Contradirectional Surface Mode Coupling

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Single-mode surface emission has been achieved from visible red GaInP/AlGaInP laser diodes by applying the contradirectional surface mode coupling technique. The emission wavelength (≈ 679.5 nm) of the laser structures was adjusted (decreased) in steps of 0.2 nm in an interval of 1.5 nm by reducing the thickness of the waveguide on top of the laser diode. The laser diodes emitted via the surface with a beam divergence of 0.10° and showed single-mode emission both in AC as well as in DC operation with a minimum spectral linewidth of 0.09 nm. The highest sidemode suppression achieved in DC operation was 26 dB.

1. Introduction

Semiconductor laser diodes in the visible regime are very suitable to be employed as powerful emitters in optical short-range data transmission (the attenuation minimum of *polymethylmethacrylate* (PMMA) fibers lies near 650 nm) and as light sources in the next generation of optical disk drives with their ability to read and write highly condensed optical information. The field of applications is widely spread, including spectroscopy, displays and optical sensing. Several red laser-diode-configurations have been successfully realized so far by using $Ga_xIn_{1-x}P/(Al_yGa_{1-y})_{0.5}In_{0.5}P$ sample structures. Excellent laser emission with low threshold current and high output power in the wavelength range between 620 and 690 nm has been reported.

Improvement of the emission characteristics and flexibility of the emission wavelength is desirable for advanced technical usage. If one achieves laser diodes with several single-mode emission spectra near the attenuation minimum of the optical fiber, the transmission bit rate of communication systems can be increased significantly by *dense wavelength division multiplexing* (DWDM) as the heart of *multiwavelength optical networking* (MONET). If surface emission (emission vertically to the epitaxially grown layers) is accomplished, the beam divergence is decreased essentially due to the expanded outcoupling window. Surface emission also eases the fabrication of twodimensional arrays and the integration with the driving circuit on the same wafer.

Several concepts for obtaining single-mode surface emission have been presented by using second-order grating *distributed feedback* DFB lasers. They use the incorporation of a phase-shifting film [1], preferential current pumping [2], the effect of chirping the grating structure [3] or a complex-coupled grating [4]. There is no beam steering effect due to wavelength and temperature variations, since the beam direction is fixed by the

DFB grating structure. Wavelength shift in DFB laser arrays is achieved by changing the grating period of the individual elements requiring a very precise definition of the grating period to achieve a well defined emission wavelength. But there have been no papers reporting about the realization of these concepts in the red wavelength regime. In contrast the red *vertical cavity surface emitting laser* (VCSEL) diodes [5], [6], with which large-signal modulation of 1.5 Gb/s has been demonstrated. A wavelength shift can be achieved by generating a thickness gradient across the wafer during epitaxial growth [7].

2. Methods

We have developed a method to achieve single-mode surface emission from horizontal cavity laser diodes, which is based on *surface mode coupling* (SMC). The laser diode characteristics (wavelength, emission-angle) can be adjusted after the processing as a laser diode by changing only the surface parameters (waveguide's optical thickness). This leads to a straight way of creating multi wavelength laser diode arrays [8]. As SMC laser diodes can be fabricated by using the established technique of the conventional stripe-contact laser the complex fabrication process of VCSEL structures and of DFB lasers is avoided. The principle of these laser diodes is based on a coupling mechanism between the laser mode and the surface mode which exists in a semitransparent metal/dielectricum waveguide structure on top of the laser diode. Phase matching of the laser mode and the surface mode is achieved by a surface relief grating in the laser diode. The grating causes radiation losses of the laser mode, which are reduced significantly only in a narrow spectral range by the excitation and feed back process of the surface mode. The effective gain mechanism of this resonance leads to single mode emission. Recently we have shown that the SMC technique with codirectional (the laser mode and the surface mode are propagating in the same direction) coupling can be applied to GaAs/AlGaAs and to GaInP/AlGaInP laser diodes to achieve both a singlemode emission as well as a surface emission with very narrow beam divergence [9], [10]. The radiation and the longitudinal mode characteristics of the waveguide grating structures have been investigated numerically with an in-depth analysis based on the Floquet-Bloch theory. The numerical analysis shows that in case of contradirectional (the laser mode and the surface mode are counterpropagating) coupling between the laser mode and the surface mode the sidemode suppression of the emission wavelength is increased compared to the codirectional coupling mechanism due to a narrower resonance. In Fig. 1 the waveguide loss with co- and contradirectional surface mode coupling is shown. In case of contradirectional coupling the depth of the resonance increases with the gain. The contradirectional surface mode coupling concept has now been realized for the first time.

The physical background of the SMC-concept with surface emission and with contradirectional coupling is the following: the laser light propagating in the active region is exciting a transverse electrically polarized (TE₀) surface mode in a waveguide structure on the top of the laser diode through a 2^{nd} order grating coupling. Therefore the phase matching condition

$$\beta_{\text{laser}} - 2 \times k_{\text{g}} = \beta_{\text{TEo}} + \delta$$
 (1)

has to be satisfied. β_{laser} is the propagation constant of the laser, $k_g = 2\pi/\Lambda$ the grating vector (Λ is the grating period), β_{TEo} the propagation constant of the TE₀-surface mode and δ is the phase mismatch. The surface mode couples both into the vacuum light cone resulting in surface emission and back to the active region leading to a gain mechanism and thus to single-mode emission. β_{TEo} can be "tuned" by changing the thickness of the surface waveguide. With β_{TEo} also β_{laser} and the emission wavelength of the laser diode is adjusted. The angle α of surface radiation is governed by the emission condition

$$\beta_{\text{TEo}} - k_g = \beta_{\text{light}} \times \sin \alpha$$
 (2).



Fig. 1: Waveguide loss with codirectional (a) and contradirectional (b) surface mode coupling. In case (b) the numerical analysis shows a narrower resonance and the depth of the resonance increases with the gain (G).

3. Materials

The devices realized in this work are double-quantumwell $Ga_xIn_{1-x}P/(Al_yGa_{1-y})_{0.5}In_{0.5}P$ laser diodes grown by low-pressure metallorganic vapor-phase-epitaxy (MOVPE). Sedoped (n-doped) GaAs and $Ga_{0.51}In_{0.49}P$ buffer layers, followed by a Se-doped ($Al_{0.66}Ga_{0.34})_{0.5}In_{0.5}P$ cladding layer (1000 nm) and an undoped ($Al_{0.27}Ga_{0.73})_{0.5}In_{0.5}P$ waveguide layer (65 nm) are grown successively on a n-GaAs substrate, which is tilted 6° off towards the [111]-plane. Two compressively strained $Ga_{0.4}In_{0.6}P$ quantum wells (2×10 nm) with an ($Al_{0.27}Ga_{0.73})_{0.5}In_{0.5}P$ barrier (4 nm) form the active region. Next are a ($Al_{0.27}Ga_{0.73})_{0.5}In_{0.5}P$ waveguide layer (55 nm), a Zn-doped ($Al_{0.60}Ga_{0.40})_{0.5}In_{0.5}P$ cladding layer (400 nm), a Zn-doped $Ga_{0.51}In_{0.49}P$ layer (30 nm) and finally a Zn-doped GaAs cap layer (20 nm). Asymmetric cladding layers (by the aspect of thickness and refractive index) are designed to shift the electric field distribution of the laser mode towards the surface to achieve a sufficient coupling between the laser light and the TE₀ surface-mode. The second-order grating (duty cycle 0.67) for surface mode coupling is defined by holographic exposure of a spin-coated photoresist (Hoechst AZ 5214) on the p-side of the laser structure. The pattern is etched into the top layers by ion milling (period Λ = 270 nm, height H = 100 nm). The evaporation of semitransparent Au/Zn/Au metal stripes (thickness 5 nm/5 nm/20 nm) with a width of 12.4 µm defines the stripe contacts of the lasers. Ti/Au contact pads (50 nm/250 nm), which overlap the laser stripe contact by 3.7 µm from both sides leaving a 5 µm wide window in the center of the laser stripe contact, are evaporated on a polymid isolation in between the single stripe contacts. Next the laser stripe is coated with two dielectric layers (~150 nm SiO_x (\bar{n} = 1.5) below ~250 nm SiN_x (\bar{n} = 1.9)) forming a slab waveguide on the top of the laser diode, which supports the TE₀-surface-mode. The combination of low-index and high-index substrate. Finally, the laser bars are cleaved to a length between 350 µm and 500 µm and mounted on a Peltier element.

4. Results

The SMC laser diodes showed a threshold current density (j_{th}) of 1 kA/cm^2 at a temperature of 10°C in pulsed driven (AC) and at -5° C in continuos wave (DC) operation. The series resistance of the laser diodes was near 9 Ω .

The farfield pattern of the laser diodes was measured by scanning from one cleaved facet along the laser stripe-contact to the other facet. The surface emission was observed at $\pm 50^{\circ}$ with a beam divergence of 0.10° . The divergence in the perpendicular direction was 10° . The intensity emitted per solid angle into the single surface beam was three times larger than the emitted intensity per solid angle at the edges.



Fig. 2: Wavelength emission spectrum in DC operation. The laser diode emitted at 678.1 nm with a sidemode suppression of 26 dB.

The laser diodes showed a single mode emission in AC condition as well as in DC operation. A wavelength emission spectrum in DC operation is shown in Fig. 2 ($j_{th} \times 1.3 = 1.3 \text{ kA/cm}^2$, -5°C). The laser diode emitted at 678.1 nm with a sidemode suppression of

26 dB. The minimum spectral linewidth achieved was 0.09 nm (spectrometer resolution 0.07 nm). The longitudinal mode separation of the Fabry-Perot cavity was measured to be 0.11 nm.



Fig. 3: The emission wavelength of the laser structures was adjusted (decreased) in steps of ≈0.2 nm in an interval of ≈679.5 nm to 678 nm by reducing the thickness of the waveguide on top of the laser diode.

As shown in Fig. 3 the emission wavelength of the laser structures was adjusted (decreased) in steps of ≈ 0.2 nm in an interval of ≈ 679.5 nm to 678 nm by reducing the thickness of the waveguide on top of the laser diode. (The surface waveguide was sequentially etched with HF 0.25%.) The temperature of the Peltier element was held constant at 25 °C. The resonance of the surface and the laser modes (and with it the emission wavelength of the laser diode) was shifted to the maximum of the laser gain spectrum (≈ 678.8 nm) and then to smaller wavelengths. This led to an increase and then decrease of the sidemode-suppression and of the light output intensity.

5. Conclusion

The contradirectional surface mode coupling concept has now been realized for the first time. Single-mode surface emission has been achieved from visible red GaInP/AlGaInP laser diodes by applying this technique. The emission wavelength (≈ 679.5 nm) of the laser structures was adjusted (decreased) in steps of 0.2 nm in an interval of 1.5 nm by reducing the thickness of the waveguide on top of the laser diode. The laser diodes emitted via the surface with a beam divergence of 0.10° and showed single-mode emission both in AC as well as in DC operation with a minimum spectral linewidth of 0.09 nm. The highest sidemode suppression achieved in DC operation was 26 dB.

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GaAs/AlGaAs Based Intersubband and Interminiband Mid-Infrared Emitters

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Intraband optical transitions in the conduction band of GaAs/AlGaAs heterostructures are used to generate mid-infrared radiation. Bandstructure engineering and epitaxial growth techniques make it possible to tailor the emission wavelength of mid-IR light emitting diodes over a broad range (6 - 12 micrometer). We report on the realization of these emitters, showing two different concepts. The first, interminiband emitter is based on optical transitions across the minigap of a strong coupled superlattice. The second concept is using optical transitions between discrete states in a system of coupled quantum wells. Emission, photovoltage and transmission spectra are presented. Self consistent calculations of these structures are performed and compared to the experimental data. The structures are designed to achieve population inversion in different subbands of the conduction band.

1. Introduction

Environmental monitoring, medicine, and many other technological branches are yearning for compact light sources in Mid-Infrared (MIR) part of the spectrum. The only commercially available solid state lasers working in MIR are based on lead-salt semi-conductors. Since the demonstration of the first Quantum Cascade Laser (QCL) by Faist et al (1994) [1] it became a viable source of coherent (MIR) radiation. A significant progress in the performance and operating characteristics of the QCLs has been achieved during the last five years. In 1996 operation above room temperature and peak powers of 100 mW [2], as well as CW operation at 110 K [3] was reported. A distributed feedback (single mode) QCL [4] and tunable QCL [5] were introduced in 1997. Microcylinder QCL with a bow-tie mode is reported in 1998 [6].

All these results have only been reported using a single material system, InGaAs/InAlAs lattice matched to InP. The strain requirements limit the composition of the InGaAs and the InAlAs ternaries. The GaAs/AlGaAs [7] system offers very good lattice match over the whole range of aluminum content in AlGaAs. Emitters based on this material are demonstrated [8] and lasing action at cryogenic conditions is achieved [9]. GaAs/AlGaAs is the most common III-V semiconductor material system used in the technology. Economical aspects of its using are also not negligible, since many possible applications are cost limited which is the only obstacle in their introduction to praxis.

2. Unipolar Quantum Cascade Emitters

Radiation in common laser diodes is achieved via radiative recombination of electronhole pairs across the bandgap. Quantum cascade emitters are using optical transitions of electrons between the discrete states within the conduction band of a semiconductor heterostructure. Thus the emitted wavelength is significantly less temperature dependent compared to the bandgap emitter. Bandstructure engineering allows tailoring of the emission wavelength to the application requirements over a broad range.

A Quantum Cascade (QC) emitter consists of an active cell, where the radiative transitions take place, and of an injector. The injector supplies electrons into the upper state of the active cell and secure extraction from its lower states. Active cell-injector units are cascaded (typically 25 units in cascade).



Fig. 1: Conduction band of the intersubband emitter



Fig. 2: Conduction band of the interminiband emitter

Two concepts of the active cells are known. The intersubband (ISB) concept is using typically three coupled quantum wells with three discrete energetic levels (Fig.1). Transition (3-2) is radiative. Transition (2-1) is tailored to have an energetic spacing around 36 meV (LO phonon energy in GaAs). It serves for fast extraction of the electrons from

state two. Since the ratio of $\tau(3-2)/\tau(2-1)$ lies in the order of 10, transition (2–1) is necessary to maintain population inversion. A superlattice, where the radiative transition across the minigap is used as an active cell of the interminiband concept (IMB) (Fig. 2). The internal field arising from the doping acts against the external field across the device which results in the band alignment depicted in Fig. 2. Electrons are tunneling from the injector into the miniband MB II. Optical transitions occur from the lowest state of MB II into the highest state of MB I and the electrons are free to move via the following injector into the adjacent active cell. Optical transitions between the higher states in the minibands appear at higher bias voltages. The active cell of the interminiband emitter can be a regular periodic superlattice or an aperiodic (chirped) superlattice. These modifications are used in order to maximize the optical dipole matrix element and to suppress the tunneling of the electrons from the upper states into the continuum.



Fig. 3: SEM picture of a processed disk

The implementation of these emitters into a resonator enables lasing action. Optical confinement is achieved using cladding layers that are embedding the gain medium. An alternative concept with direct access of the current to the gain medium is a disk resonator (Fig. 3). It offers the possibility to study lasing action in the gain medium independently of any cladding layers. Lasing action can take place on the free standing periphery of the disk. Light is totally reflected on the boundaries of the disk and forms closed whispering gallery modes. Low threshold current and weak omnidirectional emission is typical for these lasers.

3. Experiment

Samples are grown using standard molecular beam epitaxy (MBE) [7]. They consist typically of about 500 layers. They are lithographically processed into ridges, mesas or disks (Fig. 3). Non alloyed metallic contacts are evaporated, before these emitters are soldered to a heat sink and bonded.

The current-voltage characteristics are measured at cryogenic conditions using both quasistatic and pulsed method. Parallel to pulsed I-Vs an integral output characteristics is recorded. Light is collected using f/0.7 optics and focused on a LN₂ cooled MCT detector. Since the emitted power of these devices lies in the range of nanowatts, correlation techniques must be used to detect the signal. Step-scan, Fourier transform spectroscopy [10] is used for the spectral analysis of the electroluminescence. Besides the emission measurements we perform photocurrent and transmission measurements as a complementary characterization of the emitters.



Fig. 4: Spectra of the unipolar QC emitters

Both intersubband and interminiband concepts are tested. Some of the measured spectra are depicted in Fig. 4. Emission wavelengths are covering the range between five and twelve μ m. Peak quality (Position/FWHM) of 14 testifies outstanding quality of the growth and the used materials. The electroluminescent light was analyzed using a grid polarizer. High degree of TM polarization (up to 100%) was observed. Comparison of the peak maxima positions to the self-consistent calculation of the structures shows good agreement.

Trade-off between the requirement of high electrical conductivity and the optical parameters, like sufficient thickness and low absorbance of the cladding layers, appears to be the substantial problem on a way to electrically pumped laser. A disk resonator was fabricated. Measurements encountered problems with the inhomogeneous current distribution and did not allow to achieve lasing action.

4. Conclusion

GaAs/AlGaAs unipolar quantum cascade emitters have been designed, grown, and characterized. Optical and electrical methods are used for the investigation. We have demonstrated function of both intersubband and interminiband concepts as well as possibility of tailoring the wavelength from five to twelve μ m. The measurement results are showing good agreement with the calculations, proving us outstanding quality of the technology.

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Far-Infrared Electroluminescence in Parabolic Quantum Wells

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We have measured the far-infrared emission from parabolically graded quantum wells driven by an in-plane electric field in the temperature range from 20 K to 240 K. The peak emission corresponds to the intersubband plasmon in the parabolic potential. Its photon energy (6.6 meV / 9.8 meV) remains rather unaffected by temperature variations, the full width at half maximum ranges from 1 meV (T = 20 K) to 2 meV (T = 240 K). The reduction of emission efficiency with increasing temperature is attributed to the change in the non-radiative lifetime.

1. Introduction

The need for solid state far-infrared sources operating without a magnetic field has stimulated the research on intersubband electroluminescence in semiconductor heter-ostructures. Experiments have been performed on parabolic quantum wells [1], on superlattices [2], and more recently on quantum cascade structures [3], [4].

Parabolically graded quantum wells are promising candidates for far-infrared sources operating above liquid nitrogen temperature. The large temperature-induced variation of the electron distribution is expected to have little impact on the emission performance. In accordance with the generalized Kohn's theorem [5] the emission frequency is independent of the electron distribution and concentration in the well. In absorption and emission spectroscopy coupling between the radiation and the electron system has been observed at only one frequency [6], [1]. This is the harmonic oscillator frequency, solely determined by the width and the energetic depth of the quantum well. Here, we demonstrate the stability of the intersubband emission in a parabolic quantum well up to a temperature of 240 K [7].

2. Experimental

Two samples were examined: one with 140 nm, the other one with 200 nm well width, both with 167 meV energetic well depth. Figure 1 shows the layer structure and the device geometry of the 140 nm well sample schematically. The samples were grown by molecular beam epitaxy, depositing alternate layers of $Al_{0.3}Ga_{0.7}As$ and GaAs on a semi-insulating GaAs substrate. By adjusting the ratio of the layer thicknesses, the average Al-content in the well region is parabolically graded from x = 0 to x = 0.2. The well is sandwiched between $Al_{0.3}Ga_{0.7}As$ spacer layers and remotely doped. The sample was

contacted with two parallel AuGe Ohmic contact stripes. In order to couple out the intersubband radiation that is polarized with its electrical field perpendicular to the layers a metallic CrAu grating was evaporated between the contacts. A more detailed description of the 200 nm well sample had been given elsewhere [1].



Fig. 1: Layer structure and sample geometry of the 140 nm well sample.

We measured the electroluminescence using a Fourier-transform infrared spectrometer in step scan/lock-in mode with a spectral resolution of 0.5 meV. The sample was mounted on the cold finger of a helium-flow cryostat. The emitted radiation was collected by an off-axis parabolic mirror, transmitted through the spectrometer, and then focussed on a helium cooled Si bolometer. The whole beam path was purged with dry nitrogen gas to minimize the far-infrared absorption of water vapor. In order to excite the electron gas a pulsed electric field at a frequency of 411 Hz and 50 % duty cycle was applied between the Ohmic contacts.

3. Results

In Fig. 2 a, spectra of the 200 nm well at various temperatures are displayed. The peak emission is observed at a photon energy of 6.6 meV for all temperatures. This value corresponds to the harmonic oscillator energy calculated from the well dimensions as 6.0 meV. In agreement with the generalized Kohn's theorem, the emission energy is unaltered by the temperature-induced variation of the electron distribution in the well. The spectra of the 140 nm well in Fig. 2 b show a 20 K emission peak at 9.8 meV (calculated as 8.4 meV) that is slightly shifted to lower energies (9.1 meV) as the temperature is raised to 240 K. The full width at half maximum of the emission line of both samples ranges from 1 meV at low temperatures to 2 meV in the high temperature regime (T > 100 K). The temperature dependence of the optical power collected by the bolometer P_{co} of both samples is depicted in the inset of Fig. 2. It was determined as the integrated area of the emission spectra divided by an amplification factor and the bolometer responsivity.



Fig. 2: Emission spectra of the two samples for various temperatures as indicated. The inset shows the dependence of the collected optical power P_{co} on the inverse temperature 1/T.

The collected optical power Pco is assumed to depend on the electrical input power P_{el} and on the ratio of non-radiative lifetime τ_{nr} and radiative lifetime τ_r (in case of $\tau_r \gg \tau_{nr}$) like

$$P_{co} \propto P_{el} \frac{\tau_{nr}}{\tau_r}$$
.

The proportionality between the collected optical power P_{co} and the electrical input power P_{el} has been confirmed up to ~70 mW, above which saturation occurs. The difference in the optical power P_{co} between the two samples can be qualitatively understood by looking at the radiative lifetime τ_r . It was calculated in the model of a classical electron oscillator as 59 µs for the 140 nm well and 130 µs for the 200 nm well. With the simplifying assumption of similar non-radiative lifetimes, grating-coupler efficiencies and excitation efficiencies, one would expect the optical power P_{co} of the 140 nm well sample to be approximately twice the one of the 200 nm well sample at comparable electrical input powers P_{el} .

The decrease of (collected) optical power is induced by a thermally activated process. The solid lines in the inset of Fig. 2 are fits of the inverse sum of two exponential functions in 1/T yielding activation energies of $E_1 = 34$ meV, $E_2 = 0.8$ meV for the 140 nm well sample and $E_1 = 41$ meV, $E_2 = 2.2$ meV for the 200 nm well sample. The higher energy E_1 is probably the activation barrier for the emission of optical phonons. The intersubband transition rate $1/\tau_{nr}$ shows a similar behavior of thermal activation, as de-

scribed by Heyman et al. [8]. We may deduce that the temperature dependence of the optical power is governed by the non-radiative lifetime τ_{nr} . At temperatures above ~100 K, the emission of optical phonons limits the optical power.

4. Conclusion

We have demonstrated electrically driven far-infrared emission of parabolic quantum wells up to a temperature of 240 K. At high temperatures, the thermal energy k_BT exceeds the photon energy by a factor greater than two. Despite of the large temperature related shift of the electron distribution, we observe single frequency emission, and the impact of high temperatures on the frequency and the line shape is small. The emission efficiency is limited by the temperature dependent decrease of intersubband lifetime.

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Focused Ion Beam Technology – A New Approach for the Sub 100 nm Microfabrication Regime

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Focused ion beam (FIB) technology is an attractive tool for various maskless processes with the capability of structure fabrication below 100 nm. The current state of the art and the potential application for device modification, failure analysis, and process development is reviewed. The utilization of the FIB as a substantial component for fabrication and testing of metrology and the relevant electrical properties in the sub 100 nm regime is described.

1. Introduction

The focused ion beam represents a versatile tool for metrology and highly resolved 3-dimensional imaging of complex multilayer structures. Furthermore, it allows the fabrication of ultrafine structures by direct deposition of metal or insulator schemes and spatially confined doping. A minimum feature size down to 25 nm and a nesting tolerance of 10 nm could be obtained. Composite materials were selectively etched in reactive gas atmospheres achieving aspect ratios up to 100.

These characteristics are very attractive for future VLSI device processing techniques, because FIB provides the flexibility and reliability necessary for explorative work on scaled or entirely new devices. The ability to view, modify and analyze devices in the submicron range has established this technique in three major semiconductor applications of industrial relevance: device modification, failure analysis, and process monitoring.

The initial results shown prove the flexibility of the FIB for nanostructuring of microcircuits and suggest the relevance of this technique for the development of entirely new devices.

2. Experimental

All the experiments reported were performed on a Micrion 2500 FIB system operating at 50 kV acceleration voltage with a Ga liquid metal ion source (LMIS). The system allows the use of an ion beam with currents ranging from 1 pA to 11 nA, with a beam diameter of 5 nm (FWHM), respectively 500 nm (FWHM) for the high current mode. The energy of the ion beam can be varied between 15 and 50 keV in steps of 5 keV. The system has an additional charge neutralization electron flood gun system which guarantees higher beam stability and ESD prevention.

The stage allows translation of the sample \pm 38 mm perpendicular to the beam, 360° continuous rotation, and tilting of the sample up to 60°.

The vacuum in the recipient ($p < 10^{-7}$ Torr) is maintained by a turbo molecular pump backed by a remote mechanical pump to guarantee hydrocarbon free vacuum.

The precursor gas for the tungsten deposition was $W(CO)_6$ respectively trimethylcyclotetrasiloxane (TMCTS) and oxygen for SiO₂ formation. All depositions were performed at room temperature. For enhanced etching, XeF₂ and Cl₂ could be introduced through a nozzle. The process conditions for deposition and gas assisted etching are summarized in Table 1.

FIB	Gaseous component	Accel. voltage	Beam current	Minimum spot size	Pixel dwelltime	Pixel spacing
		kV	pA	nm	μs	μm
GAE (Fig. 1)	XeF ₂	50	1575	100	0.5	0.15
W-depo. (Fig. 1)	W(CO) ₆	50	700	65	0.5	0.11
GAE (Fig. 2)	C12	50	1575	100	0.5	0.15
W-depo. (Fig.3)	$W(CO)_6$	50	5	8	0.5	0.11

 Table 1: Process parameters

3. Measurements and Results

3.1 Device modification

This tool provides as well the potential to fabricate novel circuit layouts directly without the necessity for a sophisticated mask layout and will foster the development and introduction of new IC designs.





Fig. 1: Sample device modification by isolation cut and rewiring with tungsten deposition.

Beyond the analytical capabilities, a combination of deposition and etching steps for metals, semiconductors and insulators allows the direct construction of prototype microelectronic devices. In this operation mode the in-situ modification of circuits directly on the chip was demonstrated (Fig. 1). After the selectively removal of the passivation layer by gas assisted etching the wiring of an exemplary device was locally remodeled by first disconnecting the existing structure with subsequent redeposition of tungsten.

3.2 Failure Analysis

Failure analysis utilizes the capability of FIB technology to access and image structural details hidden beneath the surface. Knowledge of the wiring and type of the composition allows to identify the source of failure.

Using an exemplary microelectronic device the analytical feasibilities of the FIB were exploited revealing an imaging resolution down to 5 nm. By ion milling and gas assisted etching, multilayered structures could be made accessible for investigation within a few minutes and without further laborious preparation. In-situ cross-sectional imaging is highly beneficial in a multilayered fabrication sequence as it allows quick evaluation and interpretation of process steps.

Figure 2 shows a preparation sequence of an integrated circuit which was exposed to chlorine assisted sputtering. Conductive material and dielectrics could be very well distinguished by the differing contrast of the materials.



(a)



- (b)
- Fig. 2: Sequential preparing steps of an integrated circuit: (a) Removal of passivation layer/metal lines/isolation layer, respectively; (b) cross-sectional preparation of a memory cell array.

3.3 Process development

The most attractive feature of the FIB apart from the high imaging resolution is the ability of metal and insulator deposition. Unfortunately, in all cases these deposits contain influential concentrations of carbon, and oxygen. This affects the resistivity of the deposited metal inasmuch the resistivity of FIB deposited conductors is usually higher compared to pure bulk material.

In situ annealing of the deposition by heating the substrate during the focused ion beam deposition enhances the conductivity nearly equal to the pure metal [1], [2], but could introduce thermal drifts during the deposition process leading to lower pattern accuracy. John Melngailis and coworkers [3] promote a method assigned as laser assisted focused ion beam induced deposition. Thereby a laser heats the area where the ion induced chemical vapor deposition takes place confined to the diameter of the laser beam.

Using a siloxane precursor the FIB offers the capability to deposit insulator materials by ion-beam induced chemical vapor deposition from tetramethylcyclotetrasiloxane (TMCTS) in the presence of oxygen. The variation of the partial pressure of TMCTS respectively oxygen and the variation of dwell- and refresh time allow the variation of the stoichiometric composition. Hence, insulating layers with adjustable optical and electronic properties can be evolved. Such insulating materials formed by ion beam induced CVD mainly consist of Si, O, but may contain trace impurities of Ga (from the LMIS) and C by fragmentation of the silicon precursor [4]. The optical transmittance and electrical properties of the layers are mainly controlled by the amount of enclosed Gallium.

The comprehensive understanding of the deposition process will allow to improve the electrical properties of FIB deposited insulators providing the required reliability for performing circuit modifications. Baker [4] suggested metal-insulator-metal capacitor structures with FIB insulators to test the influence of enclosed Ga with regard to resistivity and breakdown voltages.

Figure 3 displays a capacitance test structure (a) formed by SiO_2 deposition between two metal pads. This setup allows monitoring of leakage current, breakdown voltage, dielectric strength and resistivity for dielectric layers feasible.



Fig. 3: Capacitor test structure (a) and interdigitated tungsten-fingers (b) with a 220 nm pitch placed on an in situ generated SiO₂ pad.

In general, new materials will be occasionally introduced and the deposition process needs to be adapted in respect to the available precursors, beam energy, refresh- and dwelltime etc. to achieve the desired resistance, dielectric strength, contact resistance and interconnect properties (ohmic or rectifying).

The installation of routine test vehicles is projected for systematic investigation of the morphological and electrical features obtained for specific deposition parameters. The deposition process was found to strongly affect the line width, nesting tolerance, contact hole sizes, etc., and yield of structures. Unified test vehicles provide a suitable mean for gaining a thorough understanding of the complex deposition mechanism.

First test structures (Fig. 3) fabricated by FIB deposition were interdigitated fingers with a 220 nm pitch (b) and metal-insulator-metal capacitor structure (a) to determine conductor to conductor shorts, surface and interfacial leakage currents respectively the dielectric strength of the SiO_2 layer. The highest performance in resolution and pattering achievable was 5 nm respectively 30 nm.

3.4 Shallow implantation

Recent applications of FIB for semiconductor devices focus on an optimized MOSFET (FIBMOS) using the localized beam to fabricate a unique, laterally tailored doping profile along the channel. The arrangement of Ga-LMIS in combination with the high resolution ion column and adjustable beam energy in the range from 50 keV to 15 keV allows generating a strategically placed ultrashallow doping profile with tolerable crystal distortion. Former investigations [5] confirmed that the output resistance improves, detrimental hot electron effects diminish and threshold voltage stabilizes as channel length is reduced, which in general leads to significantly better device performance.

4. Conclusion

Concluding the presented material illustrates the potential of FIB for metrology and highly resolved 3-dimensional imaging of complex multilayer structures. Spatially confined doping and deposition of metal as well as insulating layers was demonstrated in spatially confined areas in the nm range. Concluding, FIB is a prospective tool for the improvement of high-frequency devices as well as fabrication of entirely new circuits.

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Internal Characterization of IGBTs Using the Backside Laserprobing Technique

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This work presents the time-resolved measurement of charge carrier concentration and temperature profiles in IGBTs by Backside Laserprobing. Calibrated numerical device simulation is employed for investigating the effects of the sample preparation on the device under test and for supporting the interpretation of the experimental results.

1. Introduction

The high operating temperature due to extensive heat dissipation has become a severe and critical issue in the optimization of modern power semiconductor devices as the blocking voltage and forward current are steadily increasing [1]. Time-resolved measurements of carrier concentration and temperature during dynamic device operation provide valuable information for the verification and calibration of the electrothermal models [2] implemented in device simulation tools. In this paper we present the thermal characterization of Insulated Gate Bipolar Transistors (IGBTs) during transient switching under shorted load conditions.

The interpretation of the results is supported by calibrated numerical device simulation. Moreover, the relevance of effects on the measurement results introduced by the sample preparation are studied by multi-cell simulation.

2. Backside Laserprobing

The Backside Laserprobing technique makes use of the dependence of the refractive index of silicon on temperature (thermo-optical effect [3]) and on carrier concentration (plasma-optical effect [4]). The modulation of the refractive index is measured by detecting the phase shift of an infrared laser beam ($\lambda = 1.3\mu m$). The laser beam propagates in vertical direction and is reflected at the top metallization layer (as illustrated in Fig. 1). Thereby, its phase is shifted by

$$\varphi(t) = 2 \cdot \frac{2\pi}{\lambda} \cdot \int_{0}^{L} \left(\frac{\partial n_{si}}{\partial T} \Delta T(z,t) + \frac{\partial n_{si}}{\partial n} \Delta n(z,t) + \frac{\partial n_{si}}{\partial p} \Delta p(z,t) \right) dz, \tag{1}$$

where $\partial n_{Si}/\partial T$ is the temperature coefficient of the refractive index, $\partial n_{Si}/\partial n$ and $\partial n_{Si}/\partial p$ describe the dependence of the refractive index on the concentration of electrons and holes, respectively. ΔT , Δn and Δp are the changes of the temperature and the electron and hole density, respectively. *L* is the thickness of the substrate. Note that the influence of the temperature increase and the increase of the charge carrier density on the refractive index are opposite in sign.



Fig. 1: Cross section view of an IGBT with probing and reference laser beam. The probing beam can be placed at different positions within the window area.

To detect the phase change we use a modified version of a heterodyne laserprober setup [5] outlined in Fig. 2. A probe and a reference beam with slightly shifted wavelengths are positioned inside and outside the device active area, respectively, as shown in Fig. 1. The lateral resolution is determined by the laser beam spot size of approximately 3 μ m. The beams reflected from the device surface metallization interfere on the detector yielding a signal of the form sin($2\Delta\omega t + \varphi(t)$), where $\varphi(t)$ is the phase evolution according to Eq.1. The beat frequency $2\Delta\omega=2(\omega_1-\omega_2)$ determines the lateral distance of the two laser beams within the device structure and their wavelength shift. The phase signal $\varphi(t)$ is obtained from the time domain analysis of the detector signal.

The measurement technique requires to etch a window of 70 μ m x 70 μ m in size in the collector contact metallization. This window opening is done by a photolithographically structured etching in a two step process using HNO₃ and HF acids. Thereby, the contact metallization, which consists of a few different layers, can be removed without etching the silicon. To suppress multiple reflections within the silicon substrate (Fabry-Perot-interference), the window area is coated with an antireflective layer of Si₃N₄ by a PECVD deposition process.

The devices used in this study are vertical IGBTs with 1200 V blocking voltage. The schematics of the cross section is given in Fig. 1. The devices are operated under shorted load conditions with U_{CE} up to 500 V. Thus, operating conditions with high power dissipation as they typically occur in industrial applications can be investigated.



Fig. 2: Experimental setup of the Backside Laserprobing technique.

3. Numerical Modeling

For the quantitative evaluation of the experimental results, the device performance is simulated using a self-consistent electrothermal extension of the drift-diffusion model, as it is implemented in the general-purpose device simulator DESSIS^{ISE} [6]. The electrothermal models for the transport parameters have been calibrated with reference to the forward characteristics and the internal carrier concentration and temperature profile, which have been determined by Internal Laser Deflection measurements [2].

By simulating several IGBT cells, the effect of the window in the collector metallization on the device behavior is investigated. A current crowding causes a local increase of the carrier concentration at the edges of the window. Due to this current crowding the MOS structures, which can be seen through the window, feature a higher power dissipation. The resulting inhomogeneity of the lateral temperature profile is about 15% at the topside, whereas the temperature rise at the bottom due to the window preparation is negligible (see Fig.3).



Fig. 3: Lateral temperature profiles at different depths of the prepared IGBT device (short circuit operation at $U_{CE} = 50$ V). Due to symmetry only one half of the structure is simulated. Thus, the center of the window is located at the lateral position of 0 μ m. The schematics on the right hand side shows the 4 cutlines.

4. Experimental Results

In order to investigate the contribution of the carrier concentration on the phase shift signal, the device is investigated at low power dissipation (U_{CE} biased at 2 V). The measured phase shift for a pulse duration of $\tau = 50 \,\mu s$ is shown in Fig. 4. The contributions of carrier concentration and temperature are of the same order of magnitude. When the pulse duration is increased, the contribution of the carrier concentration does not change, as the current remains unaffected. The contribution due to the temperature increase, however, changes according to the varying power dissipation.



Fig. 4: Phase shift at low power dissipation under short circuit condition ($U_{CE} = 2 V$, pulse duration $\tau = 50 \mu s$). (a) Schematics of charge carrier and temperature contribution to the total phase shift. (b) Comparison of measured and simulated phase shift. The default implementation of the device simulator does not take into account the Peltier heating at the semiconductor/metal interface of the collector contact [7]. Adding this extra heat source yields the correct thermal contribution.

(b)

In the case of short circuit operation at high collector emitter voltages the thermal contribution becomes dominant. The phase change due to a change of the charge carrier density can be neglected. Therefore, the phase shift $\varphi(t)$ is a measure of the integral of the temperature change along the beam path.

The IGBTs are designed to withstand shorted load conditions for 10 μ s. According to this specification gate pulses of 15 V height and length of 10 μ s are applied. The power dissipation is controlled by varying the collector emitter voltage U_{CE} between 50 and 500 V. The current is nearly independent of the applied voltage as it is confined by the MOS-structure of the IGBT. For different voltages U_{CE} the measured phase shift is shown in Fig. 5. The constant power dissipation during a current pulse causes a linear rise of the phase shift. A small increase of the phase shift is observed after pulse turn-off for about 40 μ s. This is due to heat conduction from the edge of the window to the center of the window [8]. After this short time effect the cooling of the device is visible on a time scale of several 100 μ s.



Fig. 5: Phase shift for short circuit operation at high collector emitter voltages U_{CE} with a pulse duration of 10μ s. The surface temperature is calculated assuming a linear vertical temperature distribution.

The vertical temperature profile (in direction of the beam propagation) during the current pulse is dominated by the power dissipation in the channel region. Therefore, a linear decrease of the lattice temperature with increasing depth can be assumed. Thus, the phase shift can be interpreted as a measure for the maximum temperature in the device during the heating pulse (cf. scaling on the right hand side in Fig. 5). A temperature increase of $\Delta T = 120$ K is obtained at U_{CE} = 500 V at the end of the heating pulse. This temperature is far below the critical values assumed for latch-up, thus verifying safe operation at short circuit bias.

5. Conclusion

The internal transient behavior of vertical IGBTs under short circuit conditions has been studied by employing the Backside Laserprobing technique. Charge and temperature induced phase signals are analyzed in order to determine the temperature variation in the surface region. The influence of the preparation of the samples has been investigated by accurate numerical simulations, which have shown to be indispensable for the correct interpretation of the experimental results.

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Enhanced Energy Resolution in Ballistic Electron Emission Microscopy Through InAs Base Layers

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Ballistic Electron Emission Spectroscopy (BEES) and Ballistic Electron Emission Microscopy (BEEM) offer the unique possibility of probing subsurface quantum states. To improve the spectroscopic sensitivity, it is important to increase the amount of electrons which are able to penetrate into the sample. In this work we show that the transmission coefficient and the attenuation length of the base layer can be enhanced by more than one order of magnitude, if the commonly used thin metal film is replaced by a molecular beam epitaxy (MBE) grown InAs layer. At low temperatures (T = 100 K), a passivated InAs layer yields an attenuation length in the order of 70 nm – 90 nm instead of 5 nm obtained on Au films.

During the last years, scanning tunneling microscopy (STM) and related techniques have evolved as powerful tools in the investigation of surfaces [1], [2]. With the introduction of ballistic electron emission microscopy/spectroscopy by Kaiser and Bell [3], [4] the unique spatial resolution of the STM has been combined with the possibility of local probing the electronic structure of sub-surface interfaces.

In typical BEEM experiments, the ballistic electron current is in the low pA range and thus, the transmission coefficient though the metal base becomes a limiting factor for spectroscopic resolution. If buried structures, such as minibands in superlattices, shall be investigated [5], the ballistic electron current through the superlattice will be smaller by at least one order of magnitude than e.g. for an Au-GaAs Schottky diode. In this work, low temperature BEEM studies are carried out on MBE grown InAs-GaAs heterostructures, where a degenerately n-doped InAs layer replaces the commonly used metallic base. At appropriate growth temperatures (550 °C) a closed and suitable flat InAs layer was achieved. Due to the large lattice mismatch between InAs and GaAs (7.2 %), such layers are strained, but as shown by Ke and coworkers [8] the strain is fully relaxed by dislocations for film thickness above 33 monolayers. InAs carries the unique advantage of a surface accumulation layer. For this reason, insulating surface depletion barriers like on other semiconductors such as GaAs or silicon do not play a role.

InAs-GaAs heterostructures with InAs film thickness between 160 nm and 300 nm were investigated. Bar-shaped InAs mesas (0.3 mm x 2.5 mm) were defined by photolithography and using a wet chemical etchant. Then, a In-Sn back contact was alloyed in forming gas atmosphere. A second etch process was made to obtain different InAs film thickness, followed by a polishing and passivation process based on an aqueous $P_2S_5/(NH_4)_2S$ solution originally introduced for GaAs [6]. Finally, an In-coated Au-wire was attached to establish an ohmic contact to the InAs layer. More details on this passivation process will be published elsewhere [11]. At room temperature, the internal resistance of the InAs samples was too low for reliable BEEM current detection and thus the STM head was put into a cryostat and slowly cooled to lower temperatures. For the present experiment, a temperature of T = 100 K was chosen, since this provides convenient STM operation conditions. All experiments were performed using Au tips and a tunnel current of $I_T = 1$ nA at a initial bias voltage $V_{Bias} = 2$ V. The electronic circuitry for measuring the BEEM current is described in [7].

In contrast to the data of Au-GaAs reference samples, two onset voltages are clearly visible in typical BEEM spectra. The lower onset voltage in Fig. 1(a), $V_b = 0.65$ V, is the threshold voltage for ballistic electrons overcoming the barrier at the InAs-GaAs interface in the Γ -valley. Using BEEM, Ke and coworkers [8], [9] have studied the properties of InAs-GaAs heterojunctions as a function of the InAs thickness, however, still with an Au-base layer on top. They found that the barrier height at the InAs-GaAs interface depends on the thickness of the InAs film and decreases non-linearly from 0.9 eV at a thickness of one monolayer to 0.63 eV at 33 monolayers. Above that thickness, a constant barrier height was obtained in their work indicating that the strain in the InAs film is fully relaxed. The onset voltage of $V_b = 0.65$ V in our work is in excellent agreement with their data. The second threshold at higher bias, $V_L = 0.79$ V, can be associated with the onset of ballistic electron transport through the L-valley of the InAs film. The Lvalley of GaAs cannot be associated with the observed current onset at V_L, since it is much higher in energy in our samples. A third onset at somewhat higher bias voltages due to ballistic electron transfer into the L-valley of GaAs, however, could not be resolved in the present experiment.

To analyze the data in more detail, a modified Bell-Kaiser [4] model was applied. In addition to the original model, we also included electron transmission through Γ and Lvalley of InAs, quantum mechanical reflection[10] at the GaAs-InAs barrier and a experimentally measured voltage dependent tip-sample separation [11]. For the InAs film, a bulk-like bandstructure was assumed. The effective masses in Γ and L valley were taken from [12]. Nonparabolicity effects were neglected since their influence on the calculation was found to be relatively small. Phonon assisted interface scattering is supposed to play a major role in our samples, and thus, the strict $k_{l'}$ conservation rules were relaxed in our calculation. As we have included electron transmission through the Γ and L-valley of InAs in our model, the onset voltages V_b and V_L as well as the transmission factors through the Γ and L valley, t_{Γ} (= 0.7 %) and t_{L} (= 6 %), are obtained independently. Fig. 1(b) shows the transmission of an InAs film as a function of film thickness (T = 100 K). For reference purpose, the transmission of different Au-films (T = 300 K) is shown also. Note that the attenuation length of Au is almost independent of temperature and changes only in the order of 10 % between T = 300 K and T = 77 K (see Ventrice [13] e.g.). As one can see, the transmission of an Au-film is considerably smaller than the transmission of an InAs film. For the InAs film itself, the transmission through the L-valley is found to be 8.6 times larger than through the Γ -valley for all film thicknesses. From these data, the attenuation length of ballistic electrons, λ_a , can be determined. For this purpose, the ballistic electron current IBEEM is expressed as

$$I_{BEEM} = I_T t e^{-d/\lambda_a} \tag{1}$$

where I_T is the tunneling current, t the transmission coefficient of the base layer obtained from the Bell-Kaiser model and d the film thickness. From this procedure, we obtain values of $\lambda_a = 4.6$ nm for gold, 46 nm for the InAs Γ -valley and 70 nm for the InAs Lvalley, respectively.



Fig. 1: (a) Representative BEEM spectrum for a 240 nm InAs layer. (b) Transmission coefficients for ballistic electrons through an Au-film (T = 300 K) and the Γ and L-valley of InAs (T = 100 K).

The attenuation lengths in InAs are approximately one order of magnitude larger than in Au and moreover, the attenuation length in the L-valley is approximately 30 % larger than for the Γ valley. For the Γ valley, the large attenuation length is qualitatively understood by low electron-electron scattering rates, due to the low carrier concentration in the InAs film compared to a metal film. The large transmission coefficient and the large attenuation length for electrons passing the L-valley of InAs, however, is somewhat surprising and needs a more detailed discussion. In our opinion, the process can be explained as follows: To be transmitted ballistically through the InAs L-valley, the electron has to undergo at least two scattering processes. First, the electron has to gain a large k-vector, necessary to enter the L-valley of InAs which is located at the boundary of the Brillouin zone in k-space. After the electron has reached the InAs-GaAs interface, a second scattering process is necessary to enable the transfer from the InAs L-valley into the Γ -valley of GaAs. Electron transfer into the L-valley of GaAs will only occur at higher energies and was not observed in the present experiment.

The second major advantage of InAs, or in general semiconductor base layers, results from the low effective mass. Due to the large electron mass difference in Au and GaAs, parallel momentum conservation leads to considerable electron refraction at the Au-GaAs interface. As a consequence, the energetic distribution of the ballistic electron current is inverted beyond the interface and the corresponding energetic resolution is considerably decreased. For InAs-GaAs heterostructures, however, this is not the case, since the effective mass in InAs is smaller than in GaAs. Consequently, the energetic distribution of the ballistic electron current is focussed beyond the InAs-GaAs interface and the energetic resolution of the measurement is enhanced.

In summary, we have performed BEEM studies on InAs-GaAs heterostructures, were the commonly used metal base was replaced by an degenerately doped InAs film. We have demonstrated that the BEEM current and the attenuation length of ballistic electrons is enhanced by approximately one order of magnitude on this samples. It is found that this enhancement is due to lower scattering rates in the Γ -valley of InAs and also to a large contribution of ballistic electrons passing the semiconductor base through the InAs L-valley. This enhancement of the BEEM current is beneficial for all applications, where the BEEM signal is expected to be small such as for the investigation of buried superlattices or self assembled quantum dots.

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Onset of Scattering Induced Miniband Transport

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A systematic study of electron transport in undoped GaAs/GaAlAs superlattices is presented. Hot electron spectroscopy is used to measure the superlattice transmittance at different bias conditions. The transmittance of a five period superlattice is found to be independent of the direction of the electric field, while for a superlattice larger than ten periods, a dependence of the transmission on the electric field direction is observed. The onset of scattering induced miniband transport is clearly evident. From the experimental data a coherence length of 150 nm is derived. The limiting mechanism is found to be interface roughness scattering.

1. Introduction

Decreasing the barrier thickness of multiple quantum well structures leads to a stronger coupling between the degenerate eigenstates in the wells and thus to the formation of superlattice minibands. The application of an external electric field parallel to the growth axis quantizes the energy continuum associated with the miniband dispersion into a Stark ladder of discrete energy levels, and transforms the extended Bloch waves into strongly localized wave functions. Under strong localization coherence will be reduced to a few periods and in the limit, to a single quantum well.

Numerous studies of the formation of superlattice minibands have been reported including transport measurements of biased n-i-n superlattice structures. However, it turns out that the experimental study of electronic properties of a biased superlattice is hindered by the interdependence of the intensity of the current injected and the field present in the superlattice [1]. At high electric fields the large current densities make the field in the superlattice non-uniform and causes the formation of high field domains and leads to thermal saturation of miniband transport [2].

In this work we present a study of ballistic transport in nominally undoped GaAs/ $Ga_{0.7}Al_{0.3}As$ superlattices, where the influence of electron-electron and electron-impurity scattering can be neglected. Under flat band conditions the eigenstates of the periodic structure are expected to be extended over the entire length of the superlattice. We apply the technique of hot electron spectroscopy to measure the positions of the minibands and to investigate the transmission of hot electrons in biased superlattices.

2. Experiment

A three terminal device is used to probe the transmittance of undoped GaAs/GaAlAs superlattices. An energy tunable electron beam is generated by a tunneling barrier and passes the superlattice after traversing a thin highly doped n-GaAs base layer and an undoped drift region. The measured collector current reflects the probability of an in-

jected electron to be transmitted through the superlattice. The transmittance of the superlattice can be measured directly at given superlattice bias conditions by varying the energy of the injected hot electrons independent from the superlattice bias.

Our samples, grown by molecular beam epitaxy, have the following common features: A highly doped n⁺-GaAs collector contact layer (n = 1×10^{18} cm⁻³) is followed by a superlattice and the drift regions which are slightly n-doped (5×10^{14} cm⁻³). This is followed by a highly doped (2×10^{18} cm⁻³) n⁺-GaAs layer (base) of 13 nm width. On top of the base layer a 13 nm undoped Ga_{0.7}Al_{0.3}As barrier is grown followed by a spacer and a n⁺-GaAs layer, nominally doped to n = 3×10^{17} cm⁻³, in order to achieve an estimated normal energy distribution of injected electrons of about 20 meV. Finally, a n⁺-GaAs contact layer (n = 1×10^{18} cm⁻³) is grown on top of the heterostructure to form the emitter.

In Fig. 1 the calculated conduction band diagram is shown for typical bias conditions. The miniband positions (indicated by shaded areas) are calculated using a self consistent Schrödinger calculation. The static transfer ratio $\alpha = I_C/I_E$ of a five period superlattice with 2.5 nm AlGaAs barriers and 8.5 nm GaAs wells is plotted as a function of the injection energy. The position of the first peak coincides very well with the calculated position of the first miniband. The second observed peak is shifted 36 meV to higher injection energies and is ascribed to the first LO-phonon emission replica ($\hbar\omega_{LO} = 36 \text{ meV}$) of the injected electron distribution. The peak at 150 meV represents transport through the second superlattice miniband, and the sharp rise of the transfer ratio at 280 meV is due to the transition to continuum.



Fig. 1: Calculated conduction band diagram along the growth direction. The transfer ratio of a 5 period superlattice with 2.5 nm barriers and 8.5 nm wells is plotted vs. injection energy.

The measured static transfer ratio of a 5 period superlattice with 2.5 nm AlGaAs barriers and 6.5 nm GaAs wells versus injection energy is shown in Fig. 2 for different collector biases. The black solid line represents the transfer ratio at flat band condition ($U_{BC} = 0$). The sharp increase of the transfer ratio at about 45 meV coincides very well with the lower edge of the first miniband which is calculated to be 46 meV. A clear shift of the maximum (due to the voltage drop in the drift region) and a reduction of the amplitude of the transfer ratio is observed for increasing collector voltages.



Fig. 2: Transfer ratio versus injection energy at different collector base voltages of a 5 period superlattice with 6.5 nm GaAs well and 2.5 nm AlGaAs barriers. The solid black line represents the transfer ratio under flat band condition ($U_{BC} = 0$).

In order to investigate the transmission of biased superlattices we have taken the total miniband transmission (T_{α}) which is defined as twice the area of the lower energy side of the first transfer ratio peak as a measure for the average current through the first miniband at given bias conditions. The analysis of T_{α} versus applied electric field for the five and 20 period superlattices is shown in Fig. 3. The total miniband transmission T_{α} (dots) of the 5 period sample is symmetric for both bias directions, while clear asymmetric behavior is observed for the 20 period sample (diamonds).



Fig. 3: Miniband transmission versus electric field of the 5 and 20 period superlattice compared to a one- and three-dimensional calculation respectively.

To understand our findings we have performed two different kinds of calculations for the transmission through the superlattice. In a first calculation, based on a transfer matrix method, we consider a 1-dimensional ideal structure with nominal sample parameters. The calculated coherent transmission T_{α} (dashed line) is in good agreement with the experiment for the 5 period sample as shown in Fig. 3, demonstrating that the transport is dominated by coherent transmission in this case.

However, the picture changes dramatically for the 20 period structure: For negative bias (decelerating field) the measured current decays much faster with field than the one pre-

dicted by the 1-dimensional calculation. For positive bias the current first increases slightly until it decays rapidly but always stays higher than the calculated coherent model.

We assign the observed difference between the 20 and 5 period superlattice to the onset of diffusive transport. For a longer superlattice only a small fraction of the carriers can traverse the structure without scattering. Typically, the scattering process decreases the kinetic electron energy in the transport direction, either by transferring the energy difference to a motion perpendicular to the superlattice-direction (elastic scattering), or by exciting a phonon (inelastic). If a positive bias is applied to the collector, we observe an increase of the transfer ratio since the scattered electrons contribute additionally with the coherent electrons to the collector current. For the negative bias only coherent electrons traverse the superlattice, scattered electrons are flowing back to the base according to the applied electric field. Therefore the presence of scattering destroys the symmetry of the transmission with respect to the field direction. The transition from coherent to diffusive transport is clearly evident.

In order to check this reasoning the results were compared with a second calculation of the transmission through a full 3-dimensional structure where interface roughness is included [3]. As shown in Fig. 3, the calculated transmission (solid line) becomes asymmetric in excellent agreement with the experimental result (diamonds) indicating the limitation of the coherence length due to interface roughness scattering.

Following our reasoning given above, the transmission for negative fields is mainly due to the fraction of electrons traversing the structure without scattering. The average velocity in the miniband is of the order of $\Delta d/(2\hbar) = 1.5 \times 10^7$ cm/s where d is the superlattice period and Δ the miniband width. Using this value in a mean free path of $\ell_{coh} = v\tau_{scatt} = 150$ nm, which is one of the longest reported so far.

In summary, we have used hot electron spectroscopy to investigate the transmission of biased undoped superlattices. The onset of scattering induced miniband transport has been observed and the coherence length has been determined to be 150 nm. We have shown that the coherent transport at 4.2 K is limited by interface roughness scattering.

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Analysis of Single-Mode Grating Coupled Twin Waveguide Laser Structures

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An analysis of semiconductor laser structures with adjustable single-mode emission based on a contradirectionally grating coupled twin-waveguide structure consisting of an ITO/low-index dielectric waveguide on top of a corrugated active laser waveguide is presented. At resonance between the laser mode and the surface mode the grating-coupled radiation losses show a sharp drop with a linewidth comparable to the Fabry-Perot-mode spacing of the laser cavity, thus preferring a single longitudinal mode. Intermodal discrimination of up to 20 cm^{-1} and moderate threshold gain of ~50 cm⁻¹ can be obtained. Since the resonance wavelength depends on the optical thickness of the surface waveguide, a simple post-processing adjustment of the emission wavelength with a tuning range in excess of ~15 nm can be achieved.

1. Introduction

For the realization of highly integrated wavelength division multiplexing (WDM) transmitter devices monolithic laser diode arrays are considered as a compact choice due to their capability of simultaneous transmission of several channels into a single optical fiber, thus decreasing system size and costs. Efforts on multiwavelength laser diode arrays have focussed on DFB [1] and VCSEL laser arrays. Wavelength shift in DFB laser arrays is achieved by changing the grating period of the individual elements which, however, requires a very precise definition of the grating period to achieve a well defined emission wavelength. In VCSEL arrays the wavelength shift can be achieved by generating a thickness gradient across the wafer during epitaxial growth [2]. Recently a five wavelength laser diode array [3] has been reported which utilizes the surface mode emission (SME) technique [4]. This technique provides the advantage of a simple postprocessing adjustment of the emission wavelength of the individual laser diodes by adapting the surface waveguide thickness on top of the structure. A drawback of the SME technique, however, is the relatively low side mode suppression of about 20 dB. The laser structures suggested in this paper combine both the simple post-processing wavelength adjustment of the SME technique and considerable intermodal discrimination.

2. Laser Structures

The laser structures under consideration are based on a GaAs/AlGaAs DH-Laser structure utilizing an InGaAs/GaAs-MQW active region (at $\lambda = 980$ nm) embedded in highly asymmetric cladding layers in order to shift the mode field pattern towards the surface. The n-type cladding layer on top of the GaAs-substrate (refractive index $\bar{n} = 3.523$) is formed by Al_{0.3}Ga_{0.7}As ($\bar{n} = 3.333$, thickness 1200 nm). The active layer with a thickness of 250 nm ($\bar{n} = 3.523$) is followed by a typically 300 nm thick p-Al_{0.2}Ga_{0.8}As layer ($\bar{n} = 3.393$) and a p-GaAs top layer which is 250 nm thick. The top layer is corrugated by a trapezoid shaped grating with the period $\Lambda = 192$ nm, duty cycle 0.5, slope angle of 70° and a height of 80 nm. The grating is covered with a 120 nm indium tin oxide (ITO, $\overline{n} = 1.6 + 0.04i$) film which is needed for current injection. The SWG is made of ~200-400 nm SiO_x ($\overline{n} = 1.5$) below a ~300 nm SiN_x layer ($\overline{n} = 1.9$). This combination of high-index and low-index dielectric is utilized in order to avoid excessive leakage losses into the high-index substrate.

3. Waveguide Modes

Since the WGS is basically a twin waveguide structure, two modes — a laser mode "a" and a surface mode "b" with the propagation constants β_a and β_b , respectively — exist. The grating causes grating coupled radiation into the substrate thus creating additional losses. In case of surface mode resonance (SMR), i.e. when the phase matching condition $\beta_a - \beta_b \approx 2\pi/\Lambda$ is satisfied, contradirectional coupling between the mode "a" and "b" occurs. (Note that $\Re\beta_b < 0$ since mode "b" is counterpropagating.) This means that energy is transferred from the LWG to the SWG and in turn back again. This energy transfer is accompanied by a resonant decrease of the grating coupled radiation loss into the substrate for both modes. Another benefit of this coupling is the effective increase of gain which a wave travelling over a certain in the active LWG experiences, since power is coupled into the SWG where it is transferred into the opposite direction and in turn coupled back into the LWG where it is amplified again.



Fig. 1: Attenuation curves for a WGS with a 120 nm ITO/350 nm SiO/SiN SWG for different SiN thicknesses ranging from 260 to 380 nm. α_A and α_B are the attenuation constants of the laser mode and the surface mode, respectively.

The analysis used for the calculation of the waveguide properties follows the numerical approach presented in [5]. It is a coupled mode theory which is based on a rigorous Floquet-Bloch analysis of the grating waveguide problem yielding accurate results even for strong gratings. The governing equations relating the slowly varying amplitudes of the waves propagating in the LWG and the SWG a(z) and b(z), respectively, are obtained as $da/dz = (i\kappa_{11} + G)a + i\kappa_{12} \exp(-i\delta z)b$ and $db/dz = i\kappa_{21} \exp(i\delta z)a + i\kappa_{22}b$, where the coupling coefficients κ_{ij} (*i*, *j* = 1, 2) provide information about absorption loss, radiation

loss and coupling between mode "a" and "b". The influence of gain is described by G; $\delta = \beta_a - \beta_b - 2\pi/\Lambda$ is the phase mismatch between modes "a" and "b".

Figure 1 shows the (power) attenuation curves of a WGS with a 250 nm p-Al_{0.2}Ga_{0.8}As layer and a 120 nm ITO/350 nm SiO/SiN SWG with SiN-layer thicknesses varying from 380 to 260 nm. Since the dispersion of the SWG depends on the SWG thickness the resonance wavelengths range from 990.4 to 975.2 nm. The linewidth of the SMR increases from 0.21 nm to 0.53 nm due to increasing leakage losses of the SWG. However, due to the stronger penetration of the SWG field into the grating region a moderate increase of the mutual coupling coefficient from 27 + 8.4i cm⁻¹ to 45.1 + 21.3i cm⁻¹ is observed.

4. Finite Length Resonators

The finite length resonators are formed by the WGS terminated by as cleaved facets located at $z = \pm L/2$ (cavity length L) with amplitude reflection coefficients $r_a = \sqrt{0.3}$ and $r_b = \sqrt{0.05}$ for the LWG and the SWG. The laser structures are basically Fabry-Perot (FP) cavities with an intrinsic narrow-band wavelength filter favoring to lase just one FP mode coinciding with the resonance wavelength. In order to obtain single mode operation two requirements must be met: 1) The linewidth of the SMR has to be comparable or yet better smaller than the FP mode spacing and 2) a proper matching of the SMR and the FP mode spectrum must be achieved. The former requirement is fulfilled since both the SMR and the FP mode spacing are in the sub-nm regime. The latter requirement, however, needs to be discussed in detail: An effective mode selection only occurs if one of the FP resonances is near the wavelength with minimum losses. If the wavelength of minimum loss is between two FP modes, single mode emission cannot be expected since both FP modes suffer almost equal losses. The relative position of the FP modes and the SMR, however, can be adjusted thermally since the FP modes shift with a rate of $\Delta \lambda_{FP} / \Delta T \approx \lambda / n_a \cdot \Delta n_a / \Delta T = 0.067 \text{ nm/K}$, whereas the SMR shifts more slowly $(\Delta \lambda_{res} / \Delta T \approx \lambda / (n_a + n_b) \cdot \Delta n_a / \Delta T = 0.045 \text{ nm/K})$. This is a consequence of the much smaller temperature dependence of the effective index of the SWG (n_b) than that one of the LWG (n_a). For a cavity length $L=600 \ \mu m$ a temperature deviation of 10 K shifts the FP mode spectrum from one optimum position with respect to the SMR to the next one. Thus in order to avoid mode hopping a temperature stabilization allowing maximum deviations of ~1 K is necessary.

Figure 2 shows the longitudinal mode spectrum of a laser structure (length $600 \mu m$) with an ITO/SiO/SiN SWG (layer thicknesses 120, 350 and 300 nm; the p-Al_{0.2}Ga_{0.8}As layer thickness is 300 nm). Additional losses of 10 cm⁻¹ were assumed for both sub-waveguides. The lowest threshold mode has a mode gain $2G = 45.2 \text{ cm}^{-1}$ and a threshold gain difference of about 14 cm⁻¹ which is suitable for single mode operation with a side mode suppression of more than 30 dB. A clear resonant decrease of the power radiated into the substrate is observed whereas the power emitted via the facets peaks. However, due the resonant increase of optical power in the absorbing ITO layer, also the absorbed power peaks at the SMR.



Fig. 2: Longitudinal mode spectrum (a) and normalized powers (b) for a 600 μm long device with an ITO/SiO/SiN SWG. The powers are normalized with respect to the stimulated emission power.

5. Conclusion

We have suggested a novel design for single-mode laser diodes with adjustable emission wavelength. The mode selection mechanism is based on a narrow-band suppression of radiation loss of an active/passive twin-waveguide structure. Intermodal discrimination can be as high as 20 cm⁻¹ while maintaining relative low threshold gain (~50 cm⁻¹) and moderate differential output efficiency (~40 %). Simple and precise post-processing wavelength adjustment with a range in excess of ~15 nm is feasible, since changing the SWG thickness yields a shift of the SMR at a rate of $\Delta \lambda_{res} / \Delta d_{SWG} \approx 0.12$.

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Microelectronics Technology — Cleanroom Linz

Microstructure Research: Cleanroom Linz

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The GMe supports in Linz the microstructure research in the cleanrooms of the Institut für Halbleiter- und Festkörperphysik and the Institut für Mikroelektronik. In the field of high frequency devices in 1998 a 0.5 µm MESFET-technology was developed and adapted for the realization of a hot-electron injection field effect transistor. In a collaboration with an Austrian company processing steps for a Si/SiGe heterobipolar transistor were investigated and Si/SiGe MODFET structures were fabricated. The capabilities for nanostructure patterning were expanded by further work on e-beam lithography as well as on scanning force microscopy, where structural widths down to 30 nm could be realized. The optoelectronic activities were pursued for Er-doped Si for light generation in the 1.54 µm wavelength range, and in particular electroluminescence investigations were carried out at 77 K and 300 K. Furthermore, using II-VI compounds ZnSe/ZnCdSe quantum wires were fabricated by overgrowth on prepatterned GaAs substrates, and their luminescence was studied, and highly efficient mid-infrared Bragg mirrors were grown using IV-VI heterolayers. Semiconductor nanostructures fabricated by self-assembled growth (Si/SiGe, Mn/CdTe and PbSe/PbEuTe) were investigated with respect to their elastic properties, and for the first time a three dimensional ordering could be observed.

1. Introduction

The funding of the activities in the two cleanrooms at the University of Linz which are jointly used by three groups is of vital importance for our microstructure research activities. This basic funding allows for investigations which are made possible through additional funding coming from the FWF, the OeNB, as well as through cooperations with industrial groups as listed below.

In the following short presentations an overview is given on the achievements in the year 1998. The basic equipment which is available in the clean rooms allows for MBE growth of Si-based heterostructures, of II-VI and IV-VI heterostructures, as well as for MOCVD growth of III-V compounds like GaAs/GaAlAs and GaAs/GaInAs. Apart from *in-situ* and *ex-situ* structural characterization, lateral patterning is made possible through equipment like optical, holographic and electron beam lithography. Processing includes also facilities for the deposition on insulating as well as contact layers.

Consequently, studies related to high frequency electronic and to optoelectronic devices can be performed which are described in some detail below and which were also presented at the meeting of the GMe held in Hofgastein in March 1999.

For the section on HF-systems, the microelectronics group has performed studies on a Ka-band detector InGaAs Schottky diode with high sensitivity for the 35GHz band. This diode is actually used as the receiving part of a Doppler-radar front end, developed by this group.

HF devices for the lower GHz range are now in the focus of the interest through their importance for communication and are important for the Austrian industry as well. In the semiconductor physics group in Linz work on the realization of a Si/SiGeC based heterobipolar transistor is in progress, where the carbon in the base region prevents the outdiffusion of the boron and thus allows for appreciably higher doping levels than in standard Si/SiGe HBT's. Si/SiGe based modulation doped field effect transistors were fabricated using MBE grown samples. The complete transistor requires six lithographic steps, with contact lithography down to 0.5 micrometers and e-beam lithography below this size. The essential device and process parameters were established.

Structural investigations on Si/SiGe modulation doped field effect transistors (MOD-FETs) were carried out, by studies of the strain fields in the Si channels as a function of the mesa size in the range down to 3x3 micrometers. Furthermore, in collaboration with a Swiss group, structural properties of Si/SiGe MODFET structures which were grown by an extremely fast growth technique using low energy dc plasma enhanced chemical vapor deposition techniques, a project funded also by the European commission. Finally in this context studies of growth instabilities found in Si homoepitaxy should be mentioned which are important for establishing the proper growth conditions for MBE grown heterostructures on Si substrates.

The lithographic capabilities were enhanced last year in Linz by working both on ebeam lithography as well as on the fabrication of semiconductor nanostructures employing scanning atomic force microscopy.

In the section on optoelectronics several contributions are incorporated into this report: the studies on light generation from Si by using Er doping found wide recognition: it was established that for properly designed diodes, driven in reverse bias, the electroluminescent emission turns out to be nearly temperature independent up to room temperature. Fabrication and annealing conditions for these types of diodes for maximum luminescence yield are described.

Finally, as far as the compound semiconductor activities for optoelectronics are concerned, plasma etching techniques were developed which turned out to be also useful for the fabrication of highly efficient Bragg mirrors for the mid-infrared, with stop bands between 4 and 6 micrometers and reflectivity as high as 99%.

In the field of low dimensional quantum wire and quantum dot structures, the luminescence from quantum wires grown on prepatterned substrates was investigated as well as the growth and properties of self assembled nanostructures. For the control of their growth new real time reflectance difference spectroscopy was incorporated into an existing MBE system. Furthermore, exploiting the huge elastic anisotropy as well as growth along a crystallographic [111] direction for the first time three dimensional dot crystals could be realized by self assembled growth.

Project Information for 1998

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Kainz	Ursula	Technician	
Katzenmayer	Hans	Technician	
Rabeder	Klaus	Technician	
Wirtl	Elisabeth	Technician	
Wurm	Ernst	Technician	
Kocher-Oberl.	Gudrun	Technician	
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Wilamowski	Zbyslaw	Guest	
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Publications in Reviewed Journals

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- 27. A. Bonanni, D. Stifter, K. Hingerl, H. Seyringer, H. Sitter: "In Situ Characterization of the Growth Dynamics in MBE of Mn-based II-VI Compounds: Self-organized Mn Structures on CdTe", Proc. MBE Cannes 1998 (in print)
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Presentations

Invited Talks:

- G. Bauer: "X-ray diffraction and reflectivity from semiconductor nanostructures", 27h Internationals School on Physics of Semiconducting Compounds, Jaszowiec Poland, June 7-12 1998
- 3. G. Bauer: "Halbleiternanostrukturen", Physikalisches Kolloquium, Universität Innsbruck, 25. Juni 1998
- G. Bauer, A. Darhuber, V. Holy: "Elastic Relaxation in Ge Islands", Lattice-Mismatched and Heterovalent Thin Film Epitaxy, September 13-18, 1998, Barga Italien
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Cooperations

- 1. Siemens München, Dr.Heide
- 2. Daimler Benz Reserach Laboratories Ulm, Dr. Presting, Dr. König
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A Ka-Band Detector Diode with High Sensitivity

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In this work the design and matching of a zero bias InGaAs-Schottky detector diode for 35 GHz is described. High voltage sensitivity at zero bias is achieved by incorporating indium and by matching the input impedance to 50 Ω . This diode is used as the receiving part of a Doppler-radar front-end.

1. Introduction

In millimeter-wave systems suited for automotive applications Schottky-barrier diodes are used for detecting and mixing signals because of their high switching speed which results from the unipolar conduction mechanism. III-V semiconductors are the preferred materials because of their higher electron mobility at low fields compared to Silicon. Important parameters of Schottky barrier detector diodes are series resistance, barrier height, and junction capacitance. There are two types of detector diodes: zero-bias devices and detector diodes used with bias, which need a more complicated circuitry.

2. InGaAs Diode

The voltage sensitivity of a detector diode is a function of its reverse saturation current [1]. For optimum sensitivity this current has to be in the range of 10^{-6} A. To achieve this value with GaAs technology at zero bias – which is desirable to keep the circuit as simple as possible – the barrier height must be tailored to 0.22 - 0.25 eV by incorporating indium. With increasing In content the energy gap of the semiconductor is lowered from 1.42 eV (GaAs) to 0.33 eV (InAs). With In_{0.38}Ga_{0.62}As the desired barrier height of the Schottky contact can be achieved.

The diodes were fabricated using epitaxial layers of GaAs and InGaAs grown by metal organic chemical vapor deposition (MOCVD) on GaAs-substrates. Ni/GeAu/Ni/Au films were evaporated thermally and by e-beam, respectively, and annealed to form ohmic contacts on n-type layers, Ti/Au and Cr/Au were evaporated and used for Schottky contacts. The ohmic contacts were recessed by wet chemical etching and the connection to the Schottky contact on the top was led over a SiO₂ bridge. The SiO₂ layers were etched in a reactive ion etching (RIE) reactor. The patterns for the contact pads, the interconnections and the circuit were transferred to the substrate using e-beam lithography. The layer sequence of the Schottky-barrier diodes is shown in Fig. 1. Details of the fabrication can be found in [2].



Fig. 1: Layer sequence.

The DC parameters were determined from computer controlled *I-V* measurements. The measured forward current-voltage relationship of a typical device is shown on a semilogarithmic scale in Fig. 2. The semi-logarithmic plot also allows to calculate ideality factor, series resistance, and barrier height of the devices. A straight line was fitted to the semi-logarithmic data to extract the parameters. Typical values for reverse saturation current I_S , series resistance R_S and ideality factor n of diodes with contact area $3x3 \,\mu m^2$ are shown in Table 1.

ideality	saturation	series	barrier	capacitance
factor	current	resistance	height	
1.45	$8.2 \cdot 10^{-6} \mathrm{A}$	9.7 Ω	0.22 V	10.7 fF

Tab. 1: Typical values of $In_{0.38}Ga_{0.62}As$ Schottky barrier diodes (3 μ m x 3 μ m)



Fig. 2: Semi-logarithmic plot of measured current voltage relation.

From the measured junction capacitance of a diode with $100 \times 100 \ \mu\text{m}^2$ Schottky contact area, the junction capacitance for diodes with $3 \times 3 \ \mu\text{m}^2$ anode area can be calculated. The resulting cut-off frequency $f_{co} = 1/2\pi R_S C$ for these devices is approximately 1500 GHz.



Fig. 3: Small signal model of the diode.

3. Impedance Matching

A connection of the diode to a 50 Ω microstrip line with no further impedance matching yielded a sensitivity of 1 mV/ μ W. In order to enhance sensibility it is necessary to match the diode impedance to the 50 Ω of the transmission line.



Fig. 4: Reflection coefficient of unmatched diode, frequency range 10 – 67 GHz.

Firstly, a small signal model of the diode was established by fitting the reflection coefficient (S_{11}) of the circuit shown in Fig. 3 to the measured data. The measurement of the diode was accomplished using a vector network analyzer and a wafer prober with copla-

nar probe tips. For these measurements the diodes were connected via coplanar transmission lines (CPW) deposited on the semi-insulating GaAs substrate. Figure 4 shows both measured and simulated reflection coefficients. The phase shift of S_{11} is mainly caused by the coplanar transmission line between probe tip and diode.



Fig. 5: Reflection coefficient of matched diode, frequency range 34 – 36 GHz.

Next, a three element T-structure matching network was optimized with respect to low S_{11} using HP-EESOF's Series IV Design Suite. The matching network was realized using microstrip technology with radial stubs serving as RF-grounds. Since the operating frequency of the radar front-end is restricted to 34 - 36 GHz a narrow band design is sufficient. Figure 5 shows the reflection coefficient obtained with the matching circuit. With this approach the voltage sensitivity exceeded 5 mV/ μ W [3]. The dependence of the sensitivity on the input power as well as the frequency dependence are depicted in Fig. 6. A photograph of the realized chip is shown in Fig. 7.



Fig. 6: Voltage sensitivity vs. frequency and input power



Fig. 7: Chip with three different matching circuits

4. Results

The described diode is used as a mixer in the receiving path of a Doppler-radar frontend. The signal is amplified with automatic gain control to achieve a sufficiently high signal level at the A/D-converter. A digital signal processor (DSP) analyzes the sampled signal and calculates the target speed. With a corner reflector moving at constant speed an accuracy of 0.1% is possible.

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Carbon Co-Doping of Si_{1-x}Ge_x:B Layers: Suppression of Transient Enhanced Diffusion

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 $Si/Si_{1-x}Ge_x$ heterobipolar transistors (HBTs) are now commercially available and expected to open the mobile communication market for Si-based electronics. A technological problem is caused by transient enhanced diffusion (TED) of boron in the extremely thin base layer of such transistors. It is mainly caused by injection of interstitials from a subsequent implantation processes. Co-doping of the Si_{1-x}Ge_x base with carbon is shown to significantly reduce TED.

1. Introduction

 $Si_{1-x}Ge_x$ is the obvious choice for extending the physical properties of Si through the exploitation of heterostructures without sacrificing standard Si technologies. Most of the worldwide activities in that area are dedicated to the Si/Si_{1-x}Ge_x heterobipolar transistor (HBT), which is now available commercially in integrated analog circuits that will open fast growing high-frequency markets for Si-based electronics. In contrast to even more potent devices based on III-V materials, Si_{1-x}Ge_x is readily integrated with standard Si MOS devices, which allows cost effective monolithically integrated circuits with mixed analog and digital functions. The feasibility of such hetero-BiCMOS circuits with a high degree of complexity in both their bipolar and CMOS components have been demonstrated by several companies [1], [2]. Their introduction is expected to be of major impact on the development of high-frequency electronics up to 20 GHz and beyond.

2. Transient Enhanced Diffusion

Depending on the concept of the HBT, its speed advantage is either caused by an additional drift field in a graded $Si_{1-x}Ge_x$ base (drift transistor; [3]) or by the reduction of the base width and simultaneous increase of the base doping (true HBT; [4]). In either case it is important that the heterointerfaces coincide with the p/n junctions to prevent detrimental parasitic potential barriers. Precise doping control during all fabrication and annealing steps is therefore a stringent condition for successful high frequency operation. It is especially the p-type (boron) doping of the base layer which can cause problems in later process steps, because boron is well-known for its transient enhanced diffusion in the presence of interstitials [5]. Those can be created by an oxidation process (known as oxygen enhanced diffusion; OED), or by implantation of high doses of dopants, which are routinely employed for the n-doping of the poly-emitter above the epitaxially fabricated base layer. Thermal activation of these dopants causes boron in the base to diffuse transiently much faster than would be expected from the well established bulk diffusion constant at that temperature. This can cause severe degradation of the high frequency behavior and other essential characteristics of these devices.

To suppress TED, co-doping with substitutional carbon has been proposed in the literature [6]. At sufficiently high concentrations, carbon is believed to form complexes with the injected Si interstitials [7]. This limits the density of interstitials available to transient boron diffusion, which should therefore be strongly reduced.

3. Experiments

Most experiments dealing with TED and C co-doping are based on Si layers implanted with B and C. But, since the base of a $Si_{1-x}Ge_x$ HBT is grown and doped epitaxially, it appears straightforward to deposit a B-doped $Si_{1-x-y}Ge_xC_y$ layer with a C concentration of 0.5 to 1 at. %. We have shown that such layers can be grown with a high degree of perfection under low-temperature growth conditions that allow substitutional C concentrations of a few at.%, i.e. far below the solid solubility [8].



Fig. 1: SIMS profiles of Si_{1-x}Ge_x:B and Si_{1-x-y}Ge_xC_y:B epilayers with *ex-situ* implanted Si cap layers.

To study TED in a realistic, HBT-like situation we grew by molecular beam epitaxy (MBE) highly boron-doped $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ layers, which were capped by an initially undoped Si layer. Figure 1 shows SIMS profiles of a $Si_{0.79}Ge_{0.2}C_{0.01}$:B layer in comparison with a reference layer that was lacking the C co-doping. Ge concentrations are of the order of 20 at.%, and scaled down in Fig. 1 by a factor of 100 to fit the logarithmic concentration scale of the dopants. The Si cap layers were subsequently implanted ex-situ both with As and P to create the interstitials required for TED.

Figure 2 shows the development of the B profile as a function of oven anneals in the temperature range between 550 and 900°C. Since the Ge profile is not affected in this temperature range it is just indicated by a shaded area for reasons of clarity. As ex-

pected, the reference sample shows strong TED, which leads to a basically useless doping profile after the 900°C anneal. In contrast, the presence of about 1 at.% of carbon suppresses boron TED almost completely. The B profile remains within the Si_{1-x-y}Ge_xC_y layer, and only a minor reduction of the peak concentration is observed, which lies within the accuracy of SIMS. Obviously, C co-doping is a very efficient means to stabilize the doping profile of a Si_{1-x}Ge_x n-p-n HBT during integrated circuit processing.



Fig. 2: Transient enhanced (TED) boron diffusion after annealing cycles in the temperature range 500° – 900°C. Left: Si_{1-x}Ge_x:B epilayers shows strongly enhanced diffusion at all temperatures studied. Right: Si_{1-x-y}Ge_xC_y:B epilayer suppresses TED of B almost completely.

4. Conclusions

We demonstrated that the use of a ternary $Si_{1-x-y}Ge_xC_y$ base layer with a C concentration $\leq 1\%$ for the usually employed pure $Si_{1-x}Ge_x$ layer can drastically improve the notorious transient enhancement of boron diffusion, and thus conserve the basic speed advantages associated with an HBT. Further work will concentrate on possible side effects associated with the presence of substitutional and non-substitutional carbon, and on an process-compatible optimization of the carbon concentrations necessary (and tolerable) for device operation.

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Modulation Doped Si/Si_{1-x}Ge_x-Field-Effect Transistors

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Modulation doped Si/Si_{1-x}Ge_x samples show high electron mobilities because of the motion of the carriers along a crystalline heterointerface and the absence of ionized impurities in the conduction channel. We present the methods and technologies that are applied at our institute to fabricate field-effect transistors on MBE-grown modulation doped Si/Si_{1-x}Ge_x substrates. Ion implantation is used to form highly doped regions in the substrate; metal evaporation then realizes ohmic source and drain contacts on the implanted regions, and Schottky gates on unimplanted regions. In a following mesa process, reactive ion etching (RIE) is used to isolate the devices on the substrate laterally. The complete transistor process requires six lithographic steps. We employ optical contact lithography for structures down to 0.5 μ m and electronbeam lithography for gate lengths <0.5 μ m. By incorporation of a variety of test structures in our process, we are able to derive the essential device and process parameters after each technology step. For these characterizations we use an HP 4155 semiconductor parameter analyzer and an HP 4284 LCR-meter in connection with an on-wafer prober.

1. Introduction

In a modulation doped $Si/Si_{1-x}Ge_x$ heterostructure, a 2-dimensional electron gas (2DEG) is formed which shows much higher mobilities than the 2DEG in a conventional SiO_2/Si heterostructure [1]. This is for one due to the fact that the charge carriers move along a crystalline heterointerface instead of an amorphous one. In addition, by modulation doping, the doping layer is spatially separated from the conduction channel, so free electrons are provided without having ionized impurities in the conduction path.

Our aim is to test the device applications of modulation doped $Si/Si_{1-x}Ge_x$ heterostructures grown by MBE at our institute. For this purpose we process several test structures up to a modulation doped field-effect transistor (MODFET). These fabrication processes consist of different technological steps [2] which have to be controlled and optimized with respect to the device and process parameters. In this outline we describe the technological steps that are necessary, as well as the different test structures which we employ to get information about our samples.

2. Technological Background

A field-effect transistor requires two kinds of contacts, nonrectifying ohmic contacts and well rectifying Schottky contacts. For an ohmic metal-semiconductor contact, the semiconductor has to be highly doped, so the charge carriers can tunnel through the Schottky barrier. This doping procedure is done by ion implantation, where the ionized dopants are accelerated toward the sample. The doping profile depth is then a function of the initial kinetic energy of the ions. In a following rapid thermal annealing step, the spatially destroyed lattice is rebuilt and the dopants become electrically active. Metal evaporation then realizes ohmic source and drain contacts on implanted regions and Schottky gate contacts on unimplanted regions of the sample.

When processing several device structures on one sample, they need to be isolated laterally. For this we apply a mesa structuring that defines the shapes of the devices and prevents electrical contacts via the 2DEG between them. This mesa structuring is done by reactive ion etching (RIE), where the Si and SiGe layers are dry-etched in an SF_6 or CF_4 plasma process.

Every technological step requires a mask structuring of the sample, so that only certain regions of it are prepared while the other regions are shadowed. We employ optical contact lithography for the masking process. A photoresist is applied to the sample and illuminated through a photomask. The illuminated regions of the resist can then be removed in the developing process, the remaining resist saves the underlying sample from the technological processing. With these methods of optical lithography it is possible to process Gate lengths of down to 0.5 μ m. For preparing smaller Gate lengths, e.g. for high-frequency applications, electron beam lithography is used.

3. Fabrication of Test Devices

To test the material properties of our MBE-grown modulation doped $Si/Si_{1-x}Ge_x$ heterostructures, we developed a simple fabrication process for a MODFET together with different test structures and devices. The complete process requires six lithographic steps, for which we designed a series of masks [3]. These masks are defining the regions on the sample that are implanted, evaporated or etched. They contain the MODFET Source, Drain and Gate contacts, different Hall bars with optional Gates and various test structures to control and optimize single aspects of the whole process (Fig. 1).

For Hall measurements of our samples, two Hall bars of different sizes and a square Van-der-Pauw geometry are prepared. The Hall bars can have optional gates to control the density of charge carriers in the conduction channel. With a transmission line it is possible to evaluate the ohmic contact resistances and the sheet resistance of the conduction channel. The Schottky diodes allow the measurement of the Schottky barrier height of the gate contacts and the leakage currents around the mesa etched structure. On a transistor flute with varying gate lengths the saturation drift velocity of the charge carriers ban be evaluated.

The transistor fields contain several MODFET structures with different gate lengths. A completely-processed transistor with a gate length of 1 μ m is shown in Fig. 2. At these structures we derive the transistor parameters and so the direct device application of our samples as a MODFET. For all of the mentioned characterizations we use an HP 4155 semiconductor parameter analyzer and an HP 4284 LCR-meter in connection with an on-wafer prober. The I-V characteristics for a MODFET with a 1 μ m Gate are shown in Fig. 3.



Fig. 1: Overlay of the masks for our MODFET process with six lithographic steps. In the upper left corner the Hall structures are placed, in the upper right corner the Schottky diodes. In the middle there are the transmission lines. The lower half shows the transistor fields and the transistor flutes.



Fig. 2: MODFET with a gate length of 1µm. It is processed on a modulation doped Si/SiGe sample ZSG365 grown by MBE in Linz.



Fig. 3: I-V characteristics of a MODFET with a gate length of 1 μ m. This transistor is working in an enhancement mode, so the gate voltage V_{GS} has to be increased.

4. Conclusions

We employ a technological process that allows us to derive the essential material and device parameters of our modulation doped Si/SiGe heterostructures. The test structures and devices can be fabricated in a short time and offer many possibilities for a complete characterization. The device processing can be advanced to Gate lengths <0.5 μ m by electron beam lithography, e.g. for high-frequency applications.

Acknowledgements

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Growth Instabilities in Si Homoepitaxy

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We report on a new type of growth instability in Si homoepitaxy that arises from a slight sample miscut. This instability leads to a considerable surface roughness of up to 20 Å on a distance of 250 nm and occurs in a temperature regime frequently used for Si buffer growth. We also provide a recipe to avoid surface roughening.

1. Introduction

The technical relevance of Si (001) surfaces and interfaces caused strong interest and intensive research efforts in their growth properties. The Si surface shows a general tendency for roughening during strained layer heteroepitaxy. Recently, some groups investigate this phenomenon that is commonly known as step bunching and try to amplify it to obtain templates for lateral ordering in subsequent self-organized growth, such as e.g. Ge islands.

The electronic properties of layers resulting from overgrowth are strongly influenced by their interface morphology as carrier scattering from interfacial roughness plays a major role for transport in heterostructure devices. Therefore, ideally flat Si and SiGe interfaces are indispensable prerequisites for optimum performance in present and future Sibased heterostructure devices. It is the goal of our work here to investigate the involved roughening mechanisms on the Si [001] surface and understand their driving forces to allow for the fabrication of interfaces that are as flat as possible and thus ideal for heterostructure devices.

2. Experiment

2.1 Experimental

The samples used for this study were cut from standard Si (001) wafers into 17×17 mm pieces. The substrates have well-defined miscuts of some 1° and 2° along the [100] and 1,5° along the [110] direction, respectively. We used an HF-free standard RCA cleaning procedure before loading them into our Riber SIVA 45 MBE machine. An oxide desorption step at 1000 °C initiates subsequent overgrowth. Si and SiGe layers were deposited at growth rates of 0,2 and 0,8 Å/s and growth temperatures between 350 °C and 750 °C, the layer thickness usually being 1000 Å.

After growth the surface morphology was immediately mapped in ambient air with a Park Scientific atomic force microscope (AFM) in contact mode.

2.2 Results

In Fig. 1, a series of $5\times5 \ \mu\text{m}^2$ AFM micrographs is depicted. The morphology undergoes a quite dramatic metamorphosis within this narrow temperature range: At 450 °C, the surface shows a rather regular terrace structure perpendicular to the miscut direction with an average spacing of 0.25 μ m and a height of just a few mono-atomic layers (ML; 1 ML = 1.36 Å). The period is more than an order of magnitude larger than the expected terrace width of 78 Å for equally spaced ML steps leading to a 1° miscut. The slightly undulating pattern is characteristic for the low temperature growth regime and persists at least down to temperatures of 350 °C. At 490 °C, the terrace structure is still present, but it is now covered with triangular features. Those line up almost perfectly along the [100] miscut direction, forming ridge structures perpendicular to the terrace edges. At 550 °C, remnants of the terraces and the ridges remain, but individual triangles can no longer be resolved. Upon further increase of the temperature the feature heights decrease until finally a flat surface results at 750 °C.



Fig. 1: 5×5µm AFM pictures of samples with 1° miscut along [100]. Films were deposited with 0.8 Å/s at growth temperatures of (a-c) 450, 490 and 550 °C, respectively.

The evolution of the surface morphology was found to depend surprisingly little on the growth rate in the range between 0.2 and 0.8 Å/s studied here. At 0.2 Å/s the features, especially the triangles, become more regular (Fig. 2a), but both the lateral periods and the feature heights remain constant within experimental error.



Fig. 2: The surface morphologies resulting from different miscut directions are quite variable. (a) shows a sample miscut 1° along [100], (b) 1.5° along 10° off [110]. Both layers were deposited at 490 °C and 0.2 Å/s to a thickness of 1000 Å.

The influence of the miscut direction was assessed by experiments on substrates having a 1.5° miscut along an in-plane direction 10° off [110]. An example is shown in Fig. 2b next to a [100] miscut reference sample. Obviously, the terraces run perpendicular to the respective miscut direction, but in both cases the terrace edges disintegrate into zigzag arrangements of <110> segments.

For a characterization of the surface morphologies, we extracted the average period widths of the terraces and the average peak-to-valley height variations as a function of the growth temperature, miscut angle and direction (Fig. 3).



Fig. 3: The evolution of surface features is depicted as a function of growth temperature. (a) shows the development of the feature distance and (b) the height evolution.

The most prominent feature in Fig. 3 is the simultaneous tripling of both the period length and the amplitude over the temperature range. It should be noted that the roughest surfaces result at temperatures being quite commonly used for buffer growth, i.e. 500 - 550 °C. Beyond 550 °C the feature height decreases rapidly leading to a surface showing a non-correlated roughness of merely a few Å at 750 °C.

Subsequent annealing for sufficiently long times results in flat surfaces with a rms roughness of about 2 Å and no long-range correlation. Hence, the observed instabilities are kinetically driven and thermodynamically unstable.

RHEED oscillation measurements revealed that the evolution of the surface structures takes place entirely in the step flow regime.

2.3 Discussion

The striking difference in surface morphology between the sample miscut in the [100] and [110] direction gives strong evidence for an influence of the microscopic properties, namely the dimerization of the (001) surface, on the roughness morphology. In the case of a [110] miscut two energetically different terrace edges exist : S_A steps are oriented parallel to the dimer rows on the upper terrace, and S_B steps perpendicular [1]. Initially, growth occurs mainly via S_B steps, since it is energetically more favorable to attach Si atoms to the end of a dimer row, but also because adatom diffusion is estimated to be 1000 times larger along the dimers [2], S_B step growth is mainly fed from the upper terrace as no step edge barrier (Schwoebel barrier) is present. Consequently, at low growth is mainly temperatures, S_B terraces are kinetically unstable and grow much faster. Faster growth in

return leads to a larger upper terraces, which again means a larger capture ratio, as compared to S_A type steps. In the end, this instability generally leads to step bunching and rough surfaces (see fig 2b). At somewhat higher temperatures, however, the diffusion perpendicular to the dimer rows becomes enhanced and finally the predominant diffusion asymmetry observed at lower temperatures is overcome, S_A steps advance as fast as S_B steps and the result is a flat surface.

The behavior of the [100] miscut samples is far more complex and not yet fully understood. The <110> segmentation can be understood as caused by "diffusion trenches" along the step edges, where diffusion barriers might be lower and adatoms are highly mobile. The almost perfect alignment of the triangles could be explained in terms of strain fields that are known to be connected with the surface dimer rows.

3. Conclusions

Considering the fact that every wafer is usually specified only within $\pm 0,5^{\circ}$ of an exact crystal plane the outcome of our experiments bears important implications for Si-based epitaxy. They clearly show that one has to be very concerned about Si buffer growth. Investigations on strain-induced step bunching should be carried out quite carefully. Bearing in mind that HF cleaned wafers cannot be overgrown at high temperatures because of the formation of SiC precipitates and as a consequence thereof the evolution of a considerable surface roughness. This leaves us in principal with two alternatives : Flat Si buffers on an HF cleaned wafer by either two successive buffer layers the first grown at a low temperature to avoid SiC precipitates to be formed and a second grown at higher temperatures above 600°C to smoothen the surface afterwards or annealing of the substrates after buffer growth. The second viable way to achieve a flat surface is to use RCA cleaned wafers. RCA cleaning leaves a nearly C-free oxidized wafer surface that thus can be overgrown with a Si buffer at temperatures above 650°C. This approach provides the surfaces best suited for heterostructure devices as well as future surface investigations.

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Fast Growth Method for the Fabrication of Modulation Doped Si/SiGe Field Effect Transistors

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The fabrication of SiGe-based n- and p-type MODFET structures requires the growth of strained Si or SiGe quantum wells on top of relaxed SiGe buffer layers. In order to achieve a sufficiently low threading dislocation density in the active layers, the concept of SiGe buffers with gradually increasing Ge content was developed. A disadvantage of these buffers is the time required for their fabrication, mostly by MBE or UHV-CVD. We present a novel, fast technique based on DC-plasma enhanced CVD which offers growth rates 10 - 50 times bigger than those obtained with MBE or UHV-CVD. The investigations of graded SiGe buffers by x-ray diffraction, atomic force microscopy and secondary ion mass spectroscopy reveal structural properties comparable to MBE or UHV-CVD grown material.

1. Introduction

SiGe-based MODFET structures have demonstrated device performances superior to conventional Si-based MOSFETs in the field of high-frequency applications. In order to achieve the desired electronic structure, i.e. to tailor the band gaps and band alignment, Si and SiGe channels have to be grown pseudomorphically on top of relaxed SiGe layers. In a tensely strained Si channel on top of relaxed SiGe, the sixfold degeneracy of the Δ -minima of the conduction band is removed. Two of these (Δ_2 -minima along growth direction) are lowered in energy and form the quantum well for electrons. As growth is usually performed on the (001) surface, the effective mass of the electrons relevant for the in-plane movement is then the small transverse mass ($m_t = 0.19 m_0$ for unstrained Si), which is favorable for fast device applications. However, misfit dislocations, which are required for the plastic relaxation of SiGe, are accompanied by threading segments which intersect the active layers and decrease the device performance. It has become a main aim of growth optimization to reduce the threading dislocation densities [1]. The most widely used technique is the growth of SiGe buffers, where the Ge content is graded from zero up to the final concentration of typically 20 - 30 %, followed by a constant composition buffer and the active layers (see Fig.1) [5]. The whole buffer stack has a typical thickness of several μ m, and hence the time required with conventionally applied techniques such as MBE or UHV-CVD is considerably large, since the growth rates are typically in the order of Angstrom per second.

A novel growth technique developed at the ETH Zurich in cooperation with Balzers is the so-called "Low Energy DC Plasma Enhanced CVD" (LEPECVD) [2]. With this method growth rates higher than 50 Ås⁻¹ have been demonstrated. We have investigated the structural quality of LEPECVD grown samples by means of x-ray diffraction (XRD), atomic force microscopy (AFM) and secondary ion mass spectroscopy (SIMS). It turned out that the sample quality is comparable to material grown by conventional techniques.



Fig. 1: Scheme of a n-type MODFET grown on a graded SiGe buffer. The layer thicknesses are not on scale, in reality the active layers are much thinner.

2. Experimental

The samples have been grown at the ETH Zurich on (001) oriented Si wafers. HF dipped wafers were loaded into the growth chamber via a load-lock. After outgasing and cleaning in an H-plasma, 100 nm Si buffers were grown at 600 °C, followed by the SiGe buffer layers grown at temperatures between 500 – 600 °C and at rates between 10 - 50 Ås⁻¹, typically. In contrast to conventional CVD techniques, in LEPECVD an intense low-energy plasma (arc discharge voltages of 20 - 30 V DC) is used to decompose the reactive gases SiH₄ and GeH₄ and to enhance the hydrogen desorption on the surface. The energy of the ions impinging on the substrate can be controlled by the substrate bias and usually lies in the region below 10 eV. Details on the method and sample growth can be found elsewhere [2], [3].

XRD reciprocal space maps have been recorded using a triple-axis setup with primary beam divergence and analyzer resolution of 12 arcsec, respectively. From maps around the symmetrical (004) and asymmetrical (224) reciprocal lattice points (see Fig. 2) the strain in the samples could be determined as a function of the Ge content [4].



Fig. 2: Reciprocal space maps around the (004) and (224) reciprocal lattice points for LEPECVD grown sample 5418.

Asymmetrical maps have been recorded in different (110) azimuths to detect a possible anisotropy of strain relaxation, but no such effect has been observed. Combining the XRD results with the SIMS profiles of the depth-distribution of the Ge content, finally the strain as function of depth below the sample surface has been determined. Figure 3b shows a typical SIMS profile. From the combination of this profile with the strain data from the XRD maps, finally the strain as a function of depth can be determined (Fig. 3b).



Fig. 3: (a) SIMS profile of the Ge content of sample 5418 as a function of depth below the sample surface. The graded region is grown as a sequence of small steps in the Ge content, which is clearly resolved by the SIMS. (b) Strain distribution of sample 5418 as a function of thickness above the interface between Si buffer and SiGe graded buffer.

As intended, the strain is virtually zero in the lower part of the graded buffer, and increases linearly in its upper part [5]. The constant composition part of the SiGe buffer as well as the active layers have been grown pseudomorphically on top of the graded buffer. Figure 4 shows an AFM image of the surface of a LEPECVD grown buffer layer. The typical "cross-hatch" pattern connected with the extended misfit dislocations within the graded part of the buffer is clearly visible.



Fig. 4: AFM image of LEPECVD grown sample 5441. The typical cross-hatch pattern connected with the misfit dislocations along {110} directions in the graded buffer is clearly visible.

3. Conclusion

The comparison of these results with measurements on comparable samples grown by MBE shows that the structural quality of LEPECVD grown material is quite comparable to samples grown by conventional techniques. The FWHM along ω -direction in the reciprocal space maps is only slightly larger than in MBE grown samples. The surface roughness of the samples is typically 20 – 30Å (r.m.s. value), also comparable to MBE grown material. Thus LEPECVD seems to be a promising method for the fast growth of SiGe buffer layers for high-speed device applications on an industrial scale.

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Si/SiGe Layers on Patterned Substrates for MODFET Applications

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We present a systematic study on the strain status of Si channel in Si/SiGe MODFET structures grown on mesa structures with lateral dimensions ranging from 3 to 20 μ m, as well of its surface morphology. With decreasing mesa size, the surface undulations flatten and the in-plane strain of the Si channel is decreased.

1. Introduction

In Si-channel n-MODFET structures, a two dimensional electron gas is confined in a strained about 100 Å thick Si layer [1]. For tensile strain, the six-fold degenerate conduction band of Si is split into a two-fold $\Delta 2$ and a fourfold $\Delta 4$ state. The confining potential for the electrons in this Si-channel layer is determined by the conduction band offset between the SiGe barrier and the $\Delta 2$ states of strained Si. In order to achieve the desired strain status, usually a graded SiGe buffer layer is deposited on (001) Si, on top of which a constant composition SiGe layer is deposited, followed by the Si channel and finally a modulation doped SiGe layer on top. The grading rate of the Ge content, the thickness of the graded layer (B1) and of the constant composition buffer (B2, see Fig.1) determine the amount of strain relaxation and thus the in-plane lattice constant of the top B2 SiGe layer. The subsequently grown Si channel is pseudomorphic, i.e. biaxially tensily strained with respect to buffer B2. The plastic relaxation of the SiGe buffer layer is through misfit dislocations, the stress fields of which give rise to the roughening of the epilayer and consequently also of the interface to the strained Si layer [1], [2]. The resulting cross-hatch surface or interface morphology has a lateral periodicity of typically 1 μ m in the two orthogonal <110> directions, with rms heights of about 20 – 50 Å [2]. Too high values of this surface roughening might be not fully compatible with planar integrated circuit technology.

A concept for Si-based heterostructure devices has been developed, in which such devices could be integrated with conventional Si MOS technology on the same wafer (chip) by growing the layer sequence for heterostructure in selected areas. However, the quality of these devices always suffered from the high density of defects induced by the large lattice mismatch between Si and Ge. It has been found that reducing the lateral dimensions of the growth zone results to a dramatic decrease in the defect densities [3]. In this paper we describe a systematic study both of the strain status of the Si layer containing the 2D electron gas and of the surface morphology as a function of the lateral dimensions.

2. Experimental

The layer sequence as shown in Fig. 1 was grown on arrays of square Si (001) mesa pillars, oriented along the <110> directions, with lateral dimensions of 3, 4, 6, 10, 20 μ m and for comparison also on an unpatterened region. The mesas were etched to a depth of 2 μ m. By molecular beam epitaxy a Si buffer layer was deposited, followed by the graded SiGe buffer region (5 – 25%, with thicknesses ranging in three sample series from 250, 500 and 750 nm). A 200 nm thick SiGe buffer layer with constant Ge composition was followed by the 10 nm thick strained Si channel and a 50 nm thick SiGe layer for the n-type dopant Sb followed by a Si cap layer. The growth temperature was 550°.



Fig. 1: (a) Sketch of a MODFET grown on lateral patterned sample; (b) Top view on the sample with $(10 * 10) \,\mu\text{m}^2$ mesa size by AFM.

From x-ray reciprocal space maps we have determined the in-plane lattice constant of the top SiGe buffer layer and thus strain status of the Si channel. The data for series of mesas with the 750 nm thick B1 buffer layer are shown in Fig. 2.



Fig. 2: In plane lattice constant (a_{\parallel}) and strain (ϵ_{\parallel}) of Si-channel vs. mesa size. $\epsilon_{\parallel} = (a_{\parallel} - a_{si})/a_{si}$. a_{si} is the cubic Si lattice constant.

With decreasing mesa size the in-plane lattice constant and thus the in-plane strain in the Si channel decreases, causing a decrease of the confining potential. Below 6 μ m mesa size, due to the simultaneous SiGe growth on the Si substrate beneath the etched pillars, the data cannot be reliably interpreted. In Fig. 3 the surface morphology from atomic force microscopy is shown for a samples sequence with mesa sizes from 6 μ m to 20 μ m and for layers grown on the unpatterned substrate. The line scans exhibit remarkable differences: For the smallest mesa size of 6 μ m, in an area of 2.6 x 2.6 μ m² no cross hatch pattern is visible and the line scan shows a quite smooth surface morphology. With increasing mesa size the troughs and hills due to the cross hatch formation cause the observed surface undulations. However, the smoother surface morphology for mesa size below 10 μ m is accompanied with less SiGe relaxation of the SiGe buffer layers, and thus a decreased tensile strain of the Si channel.



Fig. 3: (a) Surface morphology of samples with different mesa size from 6, 10, 20 μm and for growth on unpatterned substrate (B1: 750 nm thick). (b) Line scans (height modulation) for these samples.

In principle for the strain relaxation in the SiGe buffers grown on mesas two mechanisms have to be considered which mainly affect the strain in the upper Si layer, namely the elastic strain relaxation due to the limited mesa size, and at the same time the decrease of the misfit dislocation density with shrinking lateral dimension. The first mechanism increases the lateral strain in the Si layer, while the second one decreases it. In order to model these trends we have calculated the dislocation density profile by minimizing the total deformation energy (the elastic energy and the energy due to the line tension of dislocation) on the basis of a phenomenological assumption of the elastic relaxation (degree of relaxation decreases exponentially from the bottom towards the free surface of the mesa). According to Tersoff [4], we obtained this profile as shown in Fig. 4 (a). Limiting the lateral mesa size, we decrease the dislocation density in the relaxed part of the buffer. In Fig. 4 (b) the lattice constant as a function of the z-coordinate in the graded buffer B1 above the Si substrate is plotted for different mesa sizes. One can distinguish regions for which the elastic relaxation dominates (for z > 550 nm, for the 750 nm thick graded B1 layer) from regions where the decrease of the dislocation density with decreasing lateral mesa size dominates (for z < 500 nm). From the experimental data it follows that actually the second mechanism dominates in the samples studied. This is actually unfavorable for the total biaxial strain in the Si channel. Apparently for achieving a better correspondence between the calculations and the experimental data a more detailed finite element calculation of the strain status has to be performed.



Fig. 4: (a) Dislocation density profile vs. depth in the graded buffer B1 for various mesa sizes L. (b) Lattice constants of B1(in plane: a_p and vertical: a_n) vs. z-coordinate. Origin of z-coordinate lies in the interface between Si buffer layer and B1 layer.

3. Conclusion

From the series of experiments on the strain status of Si/SiGe MODFET structures grown on mesa like pillars we draw the following conclusions: For mesa sizes below about 10 μ m, the lateral period of the cross hatch pattern is substantially enlarged. The surface undulations are decreased. However, the reduction of dislocation density is accompanied by a decrease of the absolute value of the in-plane strain in the Si channel. In the samples studied, elastic relaxation might alter these conclusions for sufficient small mesa size does not yet play an important role.

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Electron Beam Lithography of Nanostructures

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After a short description of the hard- and software we have used for making the nanostructures, we report on three activities: i) For Si/SiGe modulation-doped fieldeffect transistors, we fabricate Schottky gates by a lift-off technique with gate lengths below 100 nm. ii) By exposing arrays of boxes with a side length of less than 70 nm and by transferring them via reactive ion etching into a pre-structured Hall bar we produced antidots for magnetotransport investigations. iii) Oxide-patterned silicon substrates are used as a template for selective molecular beam epitaxy. By combining the prepatterned substrates with Stranski-Krastanov growth of Ge or SiGe layers, self-organized quantum dots can be arranged in a regular pattern for selective excitation or contacting.

1. Introduction

For electron beam lithography of nanostructures on Si/SiGe heterostructures we use a JEOL JSM 6400 scanning electron microscope at an accelerating voltage of 40 keV and Polymethylmetacrylat (PMMA) resists with molecular weights between 50k and 950k a.u. The samples are cleaned in acetone and methanol in combination with ultrasonic. On samples with no oxide layer we have used additionally a HF dip to increase the adhesion between substrate and photoresist. Beside the HF dip we have used no other chemicals (like hexamethyldisilicane) to improve the adhesion between substrate and photoresist.

To create the masks and for exposure we have used "Elphy FE 1.233D" from Raith. After a short trial period we have realized some bugs in the "Elphy FE" software which made it necessary to program at least a part of the software by ourselves. The "Nanoli-thography" package, we have programmed as a supplement for the "Elphy FE" software includes a design part which allows to generate the masks and export them to "Elphy FE". This solved the problem with instabilities in the mask design part of "Elphy FE". To improve the exposure quality of periodic dot structures we have implemented a small utility which optimizes the exposure parameters.

As a part of this optimization "Nanolithography" finds the proper combination of working area, working distance and magnification based on databases which include all the technical parameters of the JSM 6400. This optimization takes also into account that the JEOL has only some discrete magnifications and working distances. Without these routines "Elphy FE" would expose either to small or to big structures.

The calibration of the scaling routines has been done with the help of a Park Scientific atomic force microscope. First we calibrated it with a gold grating of known period. After calibration we investigated a grating, which we had exposed with our electron

microscope. By comparing the nominal grating period with the real period, we got a correction factor that we use now in the scaling part of the optimization.

Nanolithography by Heinz	Seyringer		_ 0	×
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Fig. 1: Utility page of the "Nanolithography" software.

Using this setup we were able to produce holes with a diameter of less than 50 nm in an SiO_2 layer.

2. Modulation-Doped Field Effect Transistors

One of the most important applications of nanostructures is the fabrication of Schottky gates for Si/SiGe modulation-doped field-effect transistors with gate lengths below 100 nm. To align these gates properly we use the mark recognition and alignment system of "Elphy FE". In the first step of the mark recognition we scan some big marks outside of the transistor structures to make a rough alignment of the mask coordinate system with the sample coordinate system. For the fine alignment we scan four masks in the immediate surrounding of the gate (see Fig.2). These four marks are used to correct the shift, rotation and scaling of the mask coordinate system.



Fig. 2: Schottky gate for Si/SiGe modulation-doped field-effect transistor written by electron beam lithography.

For the lift-off technique it is very important to get negative resist flanks. The usual way to achieve this is by exposing the resist to chemicals like chlorbenzene before it is developed. This makes the top layer of the resist more resistant against developer, which causes the developer to produce slightly negative flanks. The disadvantage of this method is that the chemicals are toxic and that the chemical reaction depends on the surface morphology.

To avoid these problems we have developed a simple but efficient method to create negative flanks. We use the highest possible accelerating voltage - which is in the case of our electron microscope 40 kV - and optimize the exposure parameters for the exposure of structures with dimensions of a few nanometers. Then we expose nominally 5 nm wide gates with a dose that is much to high. A remarkable percentage of the electrons scatters from the substrate-resist interface back into the resist (because of the proximity effect) and causes a much broader exposure distribution at the interface. The result is that we get gates with gate length below 100 nm with negative flanks without any additional chemicals.

To optimize the high frequency behavior of the transistors we investigate multiple resist layers for the fabrication of gates with T- or Γ cross sections. Basically, we use PMMA 50k and PMMA 950k as the two layers. To increase the height of the gates we investigate three layer resist systems with two layers of PMMA 950k on top of a PMMA 50k layer.

3. Antidots for Magnetotransport Investigations

To produce the antidots we have used PMMA 50k and exposed arrays of boxes with side lengths of less than 70 nm. It is important for the magnetotransport investigations that all dots have the same size and shape which means that the astigmatism correction has to be done very precisely. In vacuum there are always some hydrocarbon compounds which can be used for electron beam induced chemical vapor deposition. This deposition occurs only in the region where the primary electrons hit the sample and therefore gives an image of the beam shape which allows a precise correction of the astigmatism.



Fig. 3: Picture 3a shows a typical array of antidots. In picture 3b the astigmatism is properly corrected, while there can be seen a small astigmatism in the dots of picture 3c.

To transfer the dots from the PMMA into the silicon we use reactive ion etching (= RIE) with CF_4 gas at a power of 85 W and a pressure of 30 mtorr. The problem of the RIE is that we damage the sample and create depletion regions which have a big influence on carrier density and mobility.

By measuring the magnetoresistance we can calculate carrier density and mobility from the Shubnikov De Haas oscillations. Change in size and period of these antidots will provide information about the damaged area around the anti-dots. This information can be used to optimize the etching process and increase the electron mobility in devices by decreasing the surface scattering.

4. Oxide Windows for Ge-Dot Growth

Oxide-patterned silicon substrates are used as a template for selective molecular beam epitaxy [1]. By electron beam lithography we transferred arrays of windows less than 100 nm wide into a SiO₂ layer. These allow crystalline growth in areas where the substrate is exposed and polycrystalline deposition on the oxide covered areas. The latter can be removed selectively by etching the SiO₂ layer in diluted HF.

These oxide-windows allow the control of dot sizes and arrangements.



Fig. 4: Ge-dots grown on unpatterned silicon substates have a high density with a random distribution (Fig. 4a). In contrast, oxide patterned silicon substrates (Fig. 4b) allow us to control position and size of Ge-dots (Fig. 4c).

5. Conclusion

With the combination of "Nanolithography 2.0" and "Elphy FE" we are able to produce nanostructures for a multitude of application. Especially the use of antidots in Hall bars for optimizing RIE damage might be of interest for industrial applications.

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Fabrication of Semiconductor Nanostructures by Scanning Force Microscopy

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A process for fabrication of semiconductor nanostructures using scanning force microscopy (AFM) in combination with conventional optical lithography is described. It is based on the mechanical modification of ultra-thin photoresist layers with super-sharp AFM tips and subsequent pattern transfer by reactive ion etching. Minimal feature sizes of 45 nm and periods of 88 nm were achieved by this technique.

1. Introduction

The fabrication of semiconductor nanostructures for the development of quantum electronic devices has attracted tremendous interest in the last few years. In such devices, the electron wavelengths of typically 20 - 50 nm are comparable to the device dimensions. Therefore, the electronic properties are dominated by quantum phenomena. The realization of nanostructures remains a big technological challenge. Although with scanning probe microscopy controlled surface modifications have become possible down to the level of single adatoms [1], for practical applications one would like to combine the high lateral resolution of scanning probe techniques with existing semiconductor process technologies [2]. In the present work, we have developed a process sequence that combines conventional optical lithography with mechanical modifications of ultra-thin photoresist layers with super-sharp atomic force microscopy (AFM) tips [3]. This allows an efficient definition of very large, as well as nanoscale resist patterns with subsequent pattern transfer to the substrate in one single reactive ion etching step.

2. Process Description

The AFM patterning is realized by indentation of an AFM tip into a soft photoresist layer. This produces well defined structures where the resist is locally removed. The minimal feature size is mainly determined by three parameters, namely, 1) the resist thickness, 2) the size and shape of the AFM tips, and 3) the directionality of the final pattern transfer process. For optimum results the use of ultra-thin photoresist layers is of particular importance because the size of bulge of the displaced photoresist around the holes is the main limitation for the minimal feature separation.

2.1 Lithography with Ultra-Thin Photoresists

To produce an ultra-thin photoresist layer, the positive resist 'Shipley S1805' is diluted with a thinner ('Shipley EC Solvent') in the proportion 1:12 to 1:15. The highly thinned photoresist is spin-coated on the sample with 5500 rpm, forming a homogeneous layer

with a thickness of about 15 nm. Conventional optical photolithography with a 'Süss Mask Aligner' was used for definition of a test pattern in the resist with various device structures with typical feature sizes of several μ m (see Fig.1a).



Fig. 1: AFM images illustrating the different stages of the lithography process: a) large scale resist pattern produced by optical lithography, b) hole array indented into the 10 nm photoresist the AFM, c) large scale and d) zoomed-in images after RIE pattern transfer to the Si wafer and oxygen plasma resist removal.

Ultra-thin photoresists require a careful choice of the developer since a very low solubility of the unexposed resist is required. We have tested two different developers. The developer 'Shipley MF319' shows a significant solubility of the unexposed resist as it is increasingly diluted. While the solubility of the unthinned resist is about 0.4 nm/s, it is 1.1 nm/s for a resist thinned to 1:15. Therefore, the final resist thickness of 15 nm is very difficult to control. For the 'Microposit Developer' no solubility of the unexposed resist was found. For 15 nm resists, 15 sec developing time was found to be sufficient.

The mechanical properties of the photoresist are significant for the following AFM nanofabrication process. If the resist is too soft, a reflow of the features occurs, and if it is too hard, unnecessary large indentation forces are required. This leads to increased chances of tip damage during the resist modification. The mechanical properties of the photoresist can be adjusted by a hardbake step after the developing. Here we have used a 30 min hardbake at 130° C. This hardbake also causes a shrinking of the photoresist, which becomes more pronounced with increasing resist dilution. At a 1:15 dilution, this shrinking amounts up to 30%, i.e., the resist thickness is reduced from 15 to 10 nm.

2.2 Mechanical Patterning Using Scanning Force Microscopy

Nanoscale patterns were generated by indentation of the AFM tip into the photoresist. This produces holes with the displaced photoresist left as a bulge around the holes, as is shown in Fig. 1b). The crucial parameters of this mechanical modification process are: 1) the shape and material of the AFM tip, 2) the thickness and hardness of the resist, 3) the applied indentation force, and 4) the nonlinearity corrections of the AFM piezo scanner. In order to minimize the mechanical stress on the AFM tips during indentation, the AFM was operated throughout in the 'tapping' mode, where the cantilever is vibrated near its resonance frequency with an amplitude of about 100 nm.

At first we have used focused ion beam sharpened silicon tips of 'Park Scientific Instruments'. Although these ultra-sharp tips with tip radius of around 10 nm produce very narrow holes in the resist, the monocrystalline Si tips easily break during the mechanical contact with the sample. A much better reproducibility was achieved when using carbon EBD tips that are produced by electron beam induced deposition of very hard amorphous carbon on standard silicon tips and the subsequent sharpening with an oxygen plasma [3]. This yields tip diameters in the 10 nm range. With the EBD tips many thousands of holes can be produced without significant tip degradation. Failure usually occurs only by breaking off of the carbon tip from the cantilever. The optimal tip force applied during the indentation process is reached when the tip just penetrates the layer of photoresist down to the sample surface. If the force is too strong, apart from possible tip damages, the size of the indented holes increases. At too low indentation forces the photoresist is not penetrated entirely and no reproducible pattern transfer is possible. For the 10 nm resist, we use an exposure force of about 2 μ N. This corresponds to a scanner extension of 100 nm for cantilevers with a spring constant of 20 N/m.

The resist thickness is a crucial parameter for the ultimate resolution to be reached. Thicker resist layer lead to larger bulges, which limits the minimal distance between adjacent holes. On the other hand, since the resist is also attacked in the final pattern transfer by the reactive ion plasma, a reasonable thick resist is needed to allow a sufficiently deep etching of the samples. Therefore, a compromise between resolution and pattern transfer has to be found. For a resist thickness of 10 nm, a sufficient pattern transfer is possible (depth after etching about 30 nm), while the resolution is still good (minimal period about 85 nm, see Fig. 2). An important aspect for the fabrication of well defined complex structures is the compensation of the large nonlinearities of the AFM piezo scanners. This generic problem of AFM was solved using the external position control provided by the AFM of 'Park Scientific Instruments'. Test structures written without the scan correction exhibit pattern distortions as large as 10%.

2.3 Pattern Transfer by Reactive Ion Etching

For pattern transfer of the resist patterns to the Si wafers that were used as test samples, we have used an 'Oxford Instruments' reactive ion etcher with SF_6 as reactive gas. As the ultra-thin etch mask of the photoresist is attacked by sputtering, a high etch selectivity between the resist and Si is of crucial importance. We have increased the selectivity by using low RF powers (reduced sputtering rate of the resist). In addition, higher gas pressures and flow rates were found to increase the Si etch rate. A drastic reduction of the resist sputtering rate can be achieved by adding CH_4 , which generates a protecting polymer layer, but unfortunately this decreases also the Si etch rate. The optimal etch conditions were found to be a RF power of 30 W, SF_6 flow rate of 50 sccm, pressure of

40 mtorr and a CH_4 flow of 25 sccm. This results in an etch rate for Si of 49 nm/min and of 6 nm/min for the resist. Finally, the photoresist is stripped from the sample in the same RIE reactor with an oxygen plasma (90W, 10 sccm, 60 mtorr). The resulting patterns after these processing steps are shown in Fig. 1 c) and d).



Fig. 2: Atomic force microscopy image and cross sectional profile of a periodic hole array in Si fabricated by AFM nanolithography. Array with 10 x 10 holes with a period of 88 nm, hole diameter of 44 nm and hole depth of 16 nm.

3. Summary of the Results

The minimal feature sizes that were made by the combined optical and AFM lithography process are shown in Fig. 2. The test pattern of a periodic hole array exhibits feature diameters of about 44 nm with an etch depth of about 30 nm. Minimal grating periods of 88 nm were achieved. Apart from such hole structures we have also fabricated lines with 45 nm line widths. The lines were drawn by putting a series of holes in very close proximity (less than 30 nm) to each other. In this way also more complicated structures can be made. The largest dot arrays we have produced so far consisted of several thousand individual dots and exhibited no apparent pattern distortions within fields of several micrometer in size. The big advantage of our approach is that is a mask-based lithography technique that is independent of the substrate and which allows the use of proven semiconductor processing steps. Therefore, we were able use our method for GaAs nanostructure fabrication just by modifying the final etching process.

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Light Generation by Er in Si Related Materials

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Er-doped Si is utilized for Si-based light generation in the $1.54 \,\mu\text{m}$ region, which is of particular interest for optical data communication. The main problem of Si: Er was so far the huge temperature quenching of the luminescence yield of forward biased diodes. It turned out that properly designed diodes driven in reverse bias avoid this temperature quenching due to different excitation and deexcitation mechanisms. The fabrication and annealing conditions for maximum luminescence yield at room temperature are presented.

1. Introduction

One of the last unsolved problems and challenges in Si technology is the integration of compatible light sources as needed for optical communication within or between chips. Although there are different approaches followed worldwide, there is no obvious solution so far [1]. One of the most promising principles proposed is the light generation by intra-4f transitions in Er, which can be integrated in very different hosts giving always the same characteristic sharp spectra. Additionally, as a consequence of the well shielded 4f-shell, the emission wavelength at 1.54 μ m is temperature independent. Since the first diodes fabricated by Ennen [2] *et. al*, the temperature quenching of the luminescence yield in forward bias is still the main problem, although several groups [3], [4] were focused on Si:Er. The intensity of the room temperature emission in forward bias, however, is rather weak and comparable to the dislocation related luminescence.

For reverse bias, a completely different situation occurs. Almost no temperature quenching of the electroluminescence (EL) signal is observed indicating different excitation and deexcitation mechanisms of the Er-ions compared to forward biased diodes [5]. High resolution spectra show, that no additional emission centers are excited in reverse bias. The excitation efficiency of some specific center is very different in the two excitation modes. The efficiency for exciting isolated Er centers with a sharp emission is higher in forward bias, whereas in reverse bias mainly centers are excited with an emission similar to Er-doped silica. At elevated temperatures only the SiO₂ centers are excited, in both forward and reverse biased diodes. Therefore we investigated the preparation conditions for optimum formation of Er-doped SiO₂ centers within the Si host, which lie in a narrow region of Er and O concentrations and specific annealing treatments after ion implantation.

2. Experimental

Erbium was implanted in n-type (100)-CZ-Si with a resistivity of 10 Ω cm at room temperature. The Er-dose at an implantation energy of 300 keV was varied between 10¹²

and 10^{15} cm⁻² producing a maximum Er concentration in a depth of 100 nm ranging from 10^{17} to 10^{20} cm⁻³. The dose and energy of oxygen was adjusted to reach a ten times higher O concentration than Er concentration, which was found to give maximum photoluminescence (PL) yield. In order to remove the implantation damage and to optically activate the dopants, the samples were annealed for 30 min at temperatures between 400 and 1000 °C. Si: Er diodes were implanted through a SiO₂-mask for improved diode characteristics in reverse bias. The p/n-junction in a depth of 100 nm was formed by implantation of Er with a dose of 3×10^{14} cm⁻² at an energy of 600 keV and with B at 40 keV and a dose of 6×10^{13} cm⁻². Ohmic contacts were formed by implantation of B with a dose of 2×10^{14} cm⁻² at 30 keV at an implantation angle of 80° and with P at 30 keV and a dose of 10^{15} cm⁻² at the back side. After annealing at 1000 °C Al contacts were evaporated, the light output was enabled through an open area of the front contact.

3. Results and Discussion

At low Er concentrations an increase of the PL intensity with increasing Er concentration is observed for samples annealed at 900 °C. These samples emit atom-like spectra with linewidths of 0.5 nm. Although O co-doping increases the number of optically active Er ions, above an Er concentration of 10^{18} cm⁻³ a decrease of the PL intensity at 77 K for samples annealed at 900 °C is observed.



Fig. 1: a) Dependence of the PL-yield on the annealing temperature for Er concentrations of 10¹⁸ and 10¹⁹ cm⁻³ at 77 K. b) Temperature quenching of the PL intensity from samples with Er concentrations of 10¹⁸ and 10¹⁹ cm⁻³ annealed at 900 °C and 1000 °C.

An annealing treatment at 1000 °C increases the maximum emission yield to an Er concentration of 10^{19} cm⁻³, accompanied by a change of the emission spectra. Samples annealed at 1000 °C show spectra similar to Er-doped SiO₂, independent of the particular Er concentration. The conditions for the formation of the SiO₂ center are optimized at an Er concentration of 10^{19} cm⁻³.

The luminescence intensity of the dominating center is shown in Fig. 1a for an Erconcentration of 10^{18} and 10^{19} cm⁻³. Between 400 and 600 °C, the emission is rather weak due to implantation induced defects depending on the Er dose. Although the PL intensity of the 1000 °C annealed sample is lower at 77 K than from the 900 °C annealed sample, the onset of the temperature quenching is shifted to higher temperatures, as shown in Fig. 1b, allowing weak room temperature emission of the 1000 °C annealed sample. Different deexcitation energies of 150 meV (Er: 10^{19} cm⁻³, 1000 °C) and 100 meV (Er: 10^{18} cm⁻³, 900 °C) indicate different levels in the Si bandgap participating in the energy backtransfer from Er to the host. Such a backtransfer mechanism is responsible for the temperature quenching of 3 orders of magnitude of the luminescence intensity and this amount is nearly independent of the applied sample treatment under PL conditions.



Fig. 2: EL spectra of forward and reverse biased Si:Er LEDs at 77 K and at room temperature. In forward bias, the Er emission is nearly quenched, whereas the EL yield under reverse bias conditions is practically temperature independent.

The electroluminescence (EL) yield of forward biased diodes suffers, similar to PL conditions, from backtransfer induced quenching at higher temperatures. The EL spectra at 77 K indicate that the efficiency in exciting dislocations is higher in forward bias compared to the reverse biased diode, as shown in Fig. 2. The room temperature spectrum of the forward biased diode is dominated by dislocation related luminescence, the Errelated EL is hardly visible.

In reverse bias, however, almost no difference of the EL yield is observed by increasing the temperature up to 300 K. In addition to the Er-4f-emission, a broad background extending up to the visible range is emitted from the reverse biased diode. This background is proposed to originate from scattered hot carriers, which were accelerated within the high electric field in the reverse biased p/n-junction. In contrast to the exciton

mediated excitation of forward biased diodes, the Er-ions are impact-excited by hot carriers under reverse bias [6]. The absence of the strong temperature quenching of the EL yield in reverse bias indicates a different deexcitation as compared to forward bias. Either the backtransfer path is passivated in the high electric field or only those Er ions are impact-excited which lie within silica precipitates without efficient energy transfer back to the Si host. The spectra of highly O codoped diodes are similar to Er doped silica, indicating the possibility of Er doped SiO₂ precipitates responsible for room temperature emission.

4. Conclusion

The standard annealing treatment at 900 °C after Er implantation induces the formation of isolated Er centers giving rise for sharp emission at low temperatures. The emission of those centers, however, is quenched already at temperatures below 200 K. Increasing the annealing temperature to 1000 °C removes all sharp lines, the obtained spectra are similar to those of Er doped silica. The EL spectra of Si: Er diodes indicate that mainly those Er doped silica precipitates are excited in reverse bias. Therefore, the conditions for the formation of this particular center were optimized. Strong room temperature EL was obtained from diodes in reverse bias with an Er concentration of 10^{19} cm⁻³ and an annealing treatment at 1000 °C.

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Fabrication of Highly Efficient Mid-Infrared Bragg Mirrors from IV-VI Semiconductors

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High reflectivity IV-VI semiconductor Bragg mirrors were grown by molecular beam epitaxy on BaF₂ (111) substrates. The $\lambda/4$ layer pairs consisted of a low refractive index Pb_{1-x}Eu_xTe layer with $x_{Eu} = 6$ % and a higher index pseudoalloy PbTe/Pb_{1-x}Eu_xTe superlattice with average x_{Eu} of 1 %. Mirrors with stop bands in the range between 4 and 6 μ m were obtained with reflectivities as high as 99%.

1. Introduction

Due to their favorable electronic band structure [1], lead salt (IV-VI) lasers have long dominated the field of mid- and far infrared band gap lasers in the 3 - 30 μ m region. The inherent wavelength tunability of these lasers have made them an ideal tool for high resolution infrared (IR) spectroscopy [2]. While these lasers are usually grown on lead salt substrates, (111) oriented BaF₂ has proven to be an excellent alternative as substrate material for lead salt heterostructures [3]. In comparison to lead salt substrates, BaF₂ exhibits a much higher thermal conductivity and mechanical hardness. This would allow significant improvements in heat dissipation during laser operation and facilitate device processing procedures. In the present work, we have explored the possibilities for molecular beam epitaxy (MBE) of highly efficient lead salt based mid-infrared Bragg mirror structures required for realization of vertical cavity surface emitting diode lasers in the 4 – 6 μ m spectral region. Such devices, grown on readily available BaF₂ substrates, have great potentials for reducing threshold currents and increasing the operation temperatures of IV-VI lasers.

2. The Design of Bragg Mirrors

The basic design for high reflectivity Bragg interference mirrors is the stacking of two alternating layers with different refractive index and with a thickness equal to a quarter optical wavelength. The mirror characteristics are then governed by the refractive index contrast and the number of $\lambda/4$ pairs. In the present work we have focused on Pb_{1-x}Eu_xTe of different composition for realization of MIR Bragg mirrors that are compatible with PbTe as active material. For Pb_{1-x}Eu_xTe the refractive index below the fundamental absorption decreases with increasing Eu content and the energy gap Eg increases with dEg/dx = 3.5 eV [4]. Using Pb_{1-x}Eu_xTe layer pairs with alternating lower/higher Eu contents, Bragg mirrors without absorption of light emitted from a PbTe active region can be made. In order to keep the lattice mismatch as low as possible the Eu contents must be restricted to below about 10 %. Here, we have chosen a layer pair with Eu contents of 1 and 6 %. The 1 % layer was realized in the form of a short

period PbTe/Pb_{1-x}Eu_xTe (x = 6 %) superlattice pseudoalloy with 50 Å period and thickness ratio of 5:1.

For the mirror design, the optical properties of the individual layers were determined by FTIR transmission measurements of a thick $Pb_{0.94}Eu_{0.06}Te$ reference layer and a 3 μ m pseudoalloy superlattice.



Fig. 1: Refractive index versus wavenumber at 300 K for two $Pb_{1-x}Eu_xTe$ reference layers ($x_{Eu} = 1$ and 6%). The arrows labeled #A and #B indicate the intended stop band positions for the Bragg mirror samples.



Fig. 2: Theoretical reflectivity at the stop band center (1570 cm⁻¹) as a function of the number of $\lambda/4$ pairs for Bragg mirrors of Pb_{1-x}Eu_xTe layers. (a) for incidence of the light from PbTe as active region, (b) incidence of light from air. The full and open symbols correspond to the different layering sequence where "2" corresponds to 6% Eu, and "1" to 1% Eu.

The optical constants (absorption constant $\alpha(\omega)$ and refractive index $n(\omega)$) were derived from the fit of the transmission spectra using a method described in Ref. [4]. As shown in Fig. 1, below E_g, the refractive index is determined by a constant dielectric background ε_{∞} and, close to E_g, by the Kramers-Kronig contribution due to the changing absorption constant. The refractive index contrast therefore varies significantly with ω and is largest close to the band gap of the 1 % pseudoalloy layer.

For the mirror design we calculated the reflectivity of various mirror structures using the transfer matrix method and the experimental $\alpha(\omega)$ and $n(\omega)$ values as input parameters. As shown in Fig. 2, we find that for incidence of light from an optically denser medium (e.g. PbTe) 18 mirror pairs are required to achieve a reflectivity of 95 % and 28 pairs for R above 98 % at a wavelength of 5 μ m. For incidence of light from air, due to the additional phase shift, the stacking sequence of the mirror pair has to be reversed.

3. Results

The PbTe/Pb_{1-x}Eu_xTe multilayers were deposited on cleaved BaF₂ (111) by molecular beam epitaxy. The ternary composition was determined by the PbTe to Eu beam flux ratio, and an excess Te₂ flux was used to retain the correct stoichiometry of the ternary. All flux rates were calibrated with a quartz crystal microbalance that could be moved into the substrate position. To minimize the growth time for the thick multilayer stacks, growth rates of about 2 μ m/h were used.

In the following we show the results for a Bragg mirror designed to match the 77 K PbTe band gap (217 meV or 1750 cm⁻¹). The number of $\lambda/4$ pairs was 32. From Fig. 1, the refractive index contrast is 6 %, which is comparable to that for Bragg mirrors of III-V materials [5].



Fig. 3: (a) Measured (dots) and calculated (full line) transmission spectra for a 32 pairs Bragg mirror at 77 K with a stop band at $v_m = 1740 \text{ cm}^{-1}$ (emission wavenumber of PbTe at 77 K), (b) Cross sectional scanning electron micrograph of a 20 pair Bragg mirror mesa structure. The cleavage edge was selectively etched to reveal the layers with different Eu composition.

Due to the pseudoalloy superlattices the required total number of individual layers is 3230 and the total thickness of the Bragg mirror is 16 µm. The sequence of the $\lambda/4$ pairs, starting with the 6 % Pb_{1-x}Eu_xTe on BaF₂, was chosen to yield a high reflectivity for incidence of the light from air. The structural properties of the Bragg mirrors were determined by high resolution x-ray diffraction and scanning electron microscopy (SEM). The right hand side of Fig. 3 shows a cross sectional SEM micrograph of a 20 pair Bragg mirror sample with mesa structure, demonstrating the high lateral homogeneity and smooth interface structure of the samples. The cleavage edge was selectively etched to reveal the $\lambda/4$ layers with different Eu composition using a CH₄/H₂ plasma etch. The dark layers correspond to the $\lambda/4$ layers with the lower average Eu content, but the short period superlattice structure of this pseudoalloy layer can be resolved only by x-ray diffraction.

The FTIR transmission spectra of the 32 pair Bragg mirror sample measured at 77 K is shown in Fig. 3 (a). The main features are (1) the Fabry-Perot interference fringes due to the multiple reflections at the sample surface and the layer/BaF₂ interface, (2) the stop band of low transmittance of the Bragg mirror at $v_m = 1740$ cm⁻¹, and (3) the high frequency cut off at around 2150 cm⁻¹ due to the absorption edge of the 1 % $Pb_{1-x}Eu_xTe$ pseudo-alloy. The spacing of the fringes corresponds to the inverse optical thickness of the multilayer stack. The large refractive index jump at the BaF_2 interface also enhances the Bragg reflectivity of the samples. The transmission in the stop band region is below 0.5 %, which indicates a mirror reflectivity of better than 99 % (negligible absorption losses in the stop band region). Bragg mirrors with 20 $\lambda/4$ pairs typically exhibit a larger stop band transmission with corresponding reflectivity of about 93 %. Both values agree very well with our calculations. In spite of the large total thicknesses and large number of layers we have obtained excellent control and reproducibility of the layer thicknesses and composition. This opens promising perspectives for fabrication and applications of IV-VI mid-infrared resonant cavity light emitting diodes and vertical cavity surface emitting laser devices.

Acknowledgments

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CH₄/H₂ Plasma Etching of IV-VI Semiconductors

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We demonstrate for the first time CH_4/H_2 plasma etching of IV-VI nanostructures. Similar as for II-VI compounds, we find a power law dependence between the etch rate and the energy band gap. However, if other than group IV elements are incorporated in the crystal, the etch rate deviates from this behavior. In particular, for $Pb_{1-x}Eu_xTe$ the etch rates drastically decrease with increasing Eu content, which can be used, e. g., for preferential etching.

1. Introduction

The narrow gap IV-VI semiconductor compounds have major importance for the fabrication of mid infrared optoelectronic devices like lasers and detectors operating in the spectral range between 3 μ m and 30 μ m [1]. In the fabrication of such devices lithographic patterning and etching are of crucial importance. Up to now only wet chemical etching has been used for the fabrication of buried IV-VI heterostructure lasers. For III-V and II-VI semiconductors, however, it has been shown that plasma etching is superior in several aspects as compared to wet chemical etching. In this work we demonstrate for the first time the feasibility of CH₄/H₂ plasma etching for the structurization of IV-VI semiconductors.

2. Experimental Procedures

Our etching experiments are performed in a Technics Plasma PP300/M barrel reactor operating at 2.45 GHz. The samples are placed in the center of the reactor, which consists of a glass chamber with a total length of 40 cm and a diameter of 24.5 cm. The gas flow through the reactor is controlled by mass flow controllers for CH₄, H₂, and Ar, and the pressure is adjusted at about 0.3 mbar by a control valve to the vacuum pump. The typical steady state temperature of the samples during plasma etching reaches 150 °C. Prior to the etching, photoresist patterns are produced by standard photo lithography. Etch masks are obtained by depositing 500 Å to 1500 Å Cr on the photoresist and subsequent lift-off. For our etch experiments we use several micrometer thick molecular beam epitaxial PbTe, PbSe, and Pb_{1-x}Eu_xTe layers grown on [111] oriented BaF₂ substrates. The etch process was characterized by a profilometer and by examining the etched profiles by scanning electron microscopy.

3. Plasma Etching of Different IV-VI Compounds

In a first set of experiments we etched several different IV-VI semiconductor compounds simultaneously in the barrel reactor. Thus, the process parameters (gas flows of 5 sccm CH₄, and 50 sccm H₂, 300 W rf power, 0.2 mbar pressure in the chamber) were identical for all samples. The achieved etch depths after 10 min etching time are shown in Fig. 1 as a function on the energy band gap for the binary compounds PbSe, PbTe, and PbS, revealing a systematic decrease of the etch rate with increasing band gap. The experimental data can be fitted by a power law:

as demonstrated by the dashed line in Fig. 1.



Fig. 1: Etch depth as function of band gap for binary IV-VI semiconductors achieved in a barrel reactor with 5/50 sccm CH_4/H_2 gas flow, 300 W rf power, 10 min etch time and p = 0.2 mbar. The dashed line represents a power law fit of the data.

A similar dependence is also valid for II-VI semiconductors. In our barrel reactor we achieved for CdTe, ZnTe, ZnSe, ZnS:

$$etch rate_{II-VI} [nm/min] = 7000 E_{gap} [eV]^{-5.9}$$
(2)

This suggests an equivalent etch reaction for IV-VI and II-VI semiconductors. For $A_{II}B_{VI}$ semiconductors the etch process was suggested to be [2]:

$$A_{II}B_{VI} + 2H + 2CH_3 \longrightarrow A_{II}(CH_3)_2 + H_2B_{VI}$$
(3)

The H and CH₃ radicals are generated in the plasma [3]. However, the CH₃ radicals can also react to form a polymer deposit [4], so that deposition and etching are always competing processes. As a consequence, the etch rate depends strongly on the CH₃ content in the plasma. The assumption that the B_{VI} component is reacting with the hydrogen was supported by Auger spectroscopy on the etched surfaces [5]. The similar dependence of the etch rate on the band gap energy of II-VI and IV-VI compounds indicates that the reaction in equ. (3) describes also that of the IV-VI compounds just by exchanging A_{II} with A_{IV} . However, when Pb is substituted by other elements such as in ternary IV-VI alloys, the chemical reactions are altered. We find that the etch rate is strongly reduced and the power law dependence does not hold when Pb is partially replaced by Sn, Mn, or Eu.

4. Plasma Etching of Pb_{1-x}Eu_xTe

For more detailed investigations of the etching behavior of ternary IV-VI compounds we have focused on the PbTe/Pb_{1-x}Eu_xTe system which is one of the important material combinations for IV-VI laser fabrication. In Fig. 2(a), the etch depth of PbTe and Pb_{1-x}Eu_xTe (x = 1 %) is shown as a function of methane concentration.



Fig. 2: (a) Etch depth of $Pb_{1-x}Eu_xTe$ after 10 min for a total gas flow of 55 sccm and an rf power of 300 W; (b) Time dependent etch depth for 30/25 sccm CH₄/H₂ gas flows. The dashed lines are guides for the eye.

These results are achieved with a total CH_4/H_2 gas flow of 55 sccm as optimized for this reactor and a rf power of 300 W. With increasing methane concentration the etch depth of PbTe after 10 min increases first from 1000 nm at 10 % CH₄ to 2600 nm at 54 %. Increasing the CH₄ content above 60 % leads to a decrease of the etch depth. This behavior indicates that the etch rate increases with the CH₃ content as long as no polymerization takes place. For PbEuTe (x = 1 %) a similar concentration dependence is observed. However, the etch rate is more than a factor of 3 lower than for pure PbTe and decreases drastically with increasing Eu content (see Fig. 2(b)). In addition the maximum etch rate shifts to lower CH₄ concentrations with increasing Eu content or by the formation of non-volatile Eu compounds.

This interpretation is further confirmed by our time dependent etching experiments as summarized in Fig. 2(b). In these experiments, a methane concentration of 54 % is chosen to give a maximum etching rate for PbTe, while the total gas flow and the rf power are the same as in Fig. 2(a). While for PbTe the etch rate is nearly constant in time, the etch rate of PbEuTe decreases more and more rapidly with time with increasing Eu concentration. In fact, for $x_{Eu} = 6$ % the etching stops completely after 60 minutes due to polymer or non-volatile Eu-compound formation. Fig. 2(b) also demonstrates the very strong dependence of the etching rate on the Eu concentration. For identical etch conditions, the etch depth decreases by a factor of 50 when x_{Eu} is increased from 0 % to 6 %.

Therefore, CH_4/H_2 plasma etching can be used as preferential etch to expose $Pb_{1-x}Eu_xTe$ heterojunctions.

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ZnCdSe/ZnSe Quantum Wires by Epitaxy on Prepatterned GaAs Substrates

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The growth rate of ZnSe depends sensitively on the crystalline orientation. This anisotropic growth enables us to obtain lateral confinement in quantum wells grown on prepatterned GaAs substrates. We obtain blue light emitting ridge quantum wires and demonstrate the feasibility to fabricate V-groove quantum wires in II-VI compounds. The lateral confinement is studied by low temperature luminescence experiments.

1. Introduction

 $Zn_{1-x}Cd_xSe/ZnSe$ quantum wells can be utilized for the fabrication of laser diodes emitting in the blue-green spectral range. For III-V semiconductors it has been demonstrated that the spike-like density of states in reduced dimensions yields much narrower and higher gain peak values as compared to quantum well lasers [1]. Up to now, ZnCdSe/ ZnSe nanostructures were fabricated by post molecular beam epitaxy (MBE) structurizing and etching techniques [2]. However, these nanostructures suffer from damage induced by the etching process, and the optical properties are dominated by nonradiative recombination and strain relaxation processes [2]. For that reason, we investigate the possibility to realize quantum wires by MBE on patterned GaAs substrates, to achieve "V-groove" or "ridge" quantum wires.

2. Selectivity of the MBE Growth

As substrates we prepare (100) oriented GaAs gratings with a period of 800 nm by laser holography and subsequent preferential wet chemical etching. The etching gives trapezoidal shaped ridges, with (111) and (1-1-1) planes as side walls, embedded between grooves with various widths and depths. The substrates were dipped in HCl/H₂O before they were transferred into the MBE chamber. As reference, an unpatterned GaAs substrate was mounted on the same sample holder. The growth was performed at a substrate temperature of 350 °C in an anion enriched growth regime using elementary Zn, Cd, and Se effusion cells. To investigate the anisotropy of the growth, a sample was fabricated consisting of a stack of nominally 50 nm thick ZnSe and Zn_{0.8}Cd_{0.2}Se layers. The transmission electron micrograph in Fig. 1 shows the cross section of this sample. It clearly demonstrates that the growth rate of both alloys, the ZnSe and the ZnCdSe, is smaller on the (111) side walls of the substrate grooves as compared to the (100) oriented substrate regions on the bottom of grooves and on top of the ridges.



Fig. 1: Transmission electron micrograph of a stack of nominally 50 nm thick ZnSe/ZnCdSe layers grown on a patterned GaAs substrate.

According to these different growth rates, a quantum well grown on such a patterned substrate will be thinner at the sidewalls of the grooves also. Carriers in the quantum well will be confined in lateral direction by those thinner parts. The carriers will be localized in the potential minima of the well at the bottom of the grooves and on top of the ridges. Thus, quantum wires can be realized by the choice of the width of the (100) surfaces of the patterned GaAs substrates and by the choice of the buffer thickness under the quantum well.

3. Fabrication of Quantum Wires

In order to obtain quantum wires the following layer sequence was chosen: a 5 nm wide $Zn_{0.8}Cd_{0.2}Se$ quantum well was grown on top of a 150 nm thick ZnSe buffer layer and was capped by 120 nm ZnSe. This layer sequence was grown on two differently patterned substrates simultaneously. For both substrates the depth of the grooves was 160 nm. In sample no. 1 the width of the (100) planes on top of the ridges was 340 nm while for sample no. 2 this width was reduced below 20 nm. Fig. 2 (a, b) shows scanning electron micrographs of the sample cross sections. The surface height profiles are measured with an atomic force microscope (AFM). The results presented in Fig. 2 (c) and (d) demonstrate quantitatively the differences between these two samples. For sample no. 1, the surface shows narrow ridges with steep side walls restoring the initial (111) planes of the GaAs substrate. The ridges are separated by flat parts in the grooves. From the surface profile and the cross section (Fig. 2) it can be concluded that in this particular sample a quantum wire could be formed on top of the ridge while the lateral dimensions of the quantum well in the groove are to large to yield quantum confinement effects.



Fig. 2: Cross section of sample no. 1 (a) and no. 2 (b) together with AFM-height profiles of the surface in (c) and (d).

However, in sample no. 2 the situation is completely changed. This sample shows a zigzag surface profile with a slope of the side walls much smaller than that of the substrate. This flattened surface indicates that the ZnSe grows slowest on top of the ridges. So, on such substrates quantum wires could be formed only in the grooves.

4. Optical Properties

At low temperatures the ZnSe/ZnCdSe quantum wire structures show bright luminescence in the blue-green spectral range. The two-dimensional reference sample shows a single, excitonic emission line at 2.60 eV with a width of 11 meV. However, the spectra of the quantum wire samples are much broader and exhibit a more complex shape. Sample no. 1 shows an emission maximum at 2.59 eV with a shoulder in the blue (Fig. 3 (a)). In the spectrum of sample no. 2 two distinct emission maxima are resolved. These emission spectra are a result of the anisotropic quantum well width. However, the luminescence is also affected by lateral carrier confinement [3] and strain relaxation [4]. An assignment of the photoluminescence spectra can be done only with the help of spatial resolved low temperature cathodoluminescence experiments. A detailed study will be presented elsewhere. However, for sample no. 1 the red edge of the luminescence is located on top of the ridge while in sample no. 2, in contrast, the origin of the red luminescence peak is on the bottom of the groove. So, the luminescence experiments confirm the suggestions presented above: sample no. 1 indeed represents a "ridge" quantum wire while sample no. 2 demonstrates the possibility to achieve blue light emitting "Vgroove" quantum wires.



Fig. 3: Low temperature luminescence spectra of sample no. 1 (a) and no. 2 (b) excited by the 458 nm line of an Ar laser.

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Self-Assembling Mn-Based Nanostructures

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We report on the fabrication, by means of molecular beam epitaxy, of Mn-based nanostructures on CdTe and on the possibility to obtain regular islands with different morphology during the subsequent deposition of semiconductor compounds. The processes are monitored in situ and in real time via reflectance difference spectroscopy.

1. Introduction

In the area of semiconductor materials, self-assembling nanostructures [1] are attracting considerable attention because of their potential applications in electronic and optoelectronic devices as e.g. single electron transistors and quantum dot lasers. CdTe-based semiconducting magnetic heterostructures (MH), both in the diluted semimagnetic (DMS) phase of Cd_{1-x}Mn_xTe [2] and in the digital (DMH) arrangement embedding MnTe magnetic layers [3], [4], offer the unique opportunity of having electronic band structures which can considerably be tuned by the application of magnetic fields of moderate intensity [5], [6]. In addition, the introduction of magnetic clusters in a semiconducting matrix opens new perspectives for applications in spin-dependent switching devices and in storage technology [7]. Puzzling morphologies of self-assembled islands, depending on the growth conditions and due to strain and stress effects [8], [9] and surface diffusion processes, could represent, when properly controlled, interesting new systems for electronic confinement in low dimensions. In addition, with the presence of magnetic elements, they could allow for the study of non-collinear magnetic structures' formation [10] and of strain effects on magnetic phases. In the present work, we essentially focus on the formation of pure Mn nanocrystallites on CdTe and then on the possibility to obtain regular islands with different morphology during the subsequent deposition of semiconductor compounds.

2. Experimental

All structures are fabricated by molecular beam epitaxy (MBE) on GaAs(001)-oriented substrates: a 0.5 μ m thick CdTe buffer layer is at first deposited in excess of Te at a substrate temperature of 280 °C. The subsequent heteroepitaxy leading to island formation is carried out on the 2x1 Te-terminated CdTe(001)-oriented surface, keeping the substrate temperature constant. The MBE system is equipped with a reflection high energy electron diffraction (RHEED) apparatus with 20 keV operating voltage, suitable to follow changes in the surface reconstruction during the growth process.

With the aim of making the various formation stages reproducible, we follow the deposition phases via *in-situ* reflectance difference spectroscopy (RDS): this real-time technique allows to measure the difference between normal-incidence reflectances for light polarized along the two principal axes of the surface and it can be considered as a normal incidence ellipsometry, sensitive to surface and interface anisotropies [11], [12]. For the (001)-oriented surface we are interested in, symmetry considerations show that the optical eigenstates are [$\overline{110}$] and [110], thus the complex reflectance coefficients for light polarized along these axes are $r_{\overline{110}}$ and r_{110} . The parameter measured is the relative difference: $\Delta r/r=(r_{\overline{110}}-r_{110})/[(r_{\overline{110}}+r_{110})/2]$. Our *in-situ* RDS system is similar to the one reported in [13]. In our study, we consider the real-time kinetic mode of RDS, where $\Delta r/r$ is monitored as a function of time. All data are acquired at the fixed energy of 3.26 eV, corresponding to the E₁ electronic transition for CdTe at the considered temperature.

By following the growth process simultaneously by means of RDS in kinetic mode and RHEED, we are able to detect the significant phases of islands' formation and to obtain the reproducibility of the structures. After major changes in RDS kinetics (Fig.1), the growth process is interrupted and the surface morphology examined *ex-situ* via atomic force microscopy (AFM).



Fig. 1: Reflectance difference spectroscopy spectra in kinetic mode

The first step in our experiment is the deposition of pure Mn with a beam equivalent pressure of 0.3×10^{-8} Torr, on the Te-terminated CdTe(001) surface. As soon as the Mn nucleation starts, the RDS signal shows (region **a** in Fig.1(A)) an abrupt drop during the time corresponding to the growth of the first monolayer (ML). Successively (region **b** in Fig.1(A)), for the next two Mn MLs, the signal keeps constant, suggesting the formation of a wetting layer. After an additional steep decrease of the signal during the deposition of the fourth ML, we observe (point **c** Fig.1(A)) a sudden rise of the RDS signal and, simultaneously, a change in the RHEED pattern (till this moment stable at the 2x1 reconstruction typical for the Te-terminated CdTe surface): regular spots appear between the streaky features of the original reconstruction. From these facts we can infer that Mn

has been deposited in crystalline phase and with a lattice constant greater (smaller in the reciprocal crystallographic space mapped by RHEED) than CdTe. The surface morphology studied at this stage by means of AFM shows an arrangement of well defined islands like the one shown in Fig.2(A). For coverages from 6 to 15 MLs, we could distinguish a bimodal size distribution of nanocrystals with the smaller crystallites growing till a maximum of 20 nm in height and 150 nm in diameter and the bigger islands showing a narrow size distribution and an average height of 50 nm and average diameter of 200 nm. The average density on the surface is of $10 \,\mu m^{-2}$. When we follow the same procedure described before, but instead of ending the growth after the formation of Mn islands, we proceed depositing Te, the evolution of RHEED pattern results in spots aligned along the 2x1 reconstruction with a distance corresponding to the lattice constant of MnTe. In addition, as soon as the Te deposition starts, the RDS signal produces an oscillation (Fig.1(B)) before saturating. By analyzing real ($\Delta r/r$) versus imaginary $(\Delta \theta)$ part of the difference in anisotropy for the interval relative to the oscillation in $\Delta r/r$, we obtain a spiral-like trend (not shown), which is explained as the developing of a buried interface [14], in our case ascribed to diffusion of Te in Mn. AFM studies of the surface morphology at this stage, show 'volcanoes' (Fig.2(B)) with an average base diameter of 200 nm, a height of 20 nm, and cone-shaped craters with a maximum diameter of 50 nm. In this context, the effect can be explained in terms of strain induced by the presence of the Mn islands and having as a consequence the migration of adatoms along the side-walls of the crystallites and concomitant lack of dangling bounds in correspondence of the upper most region of Mn nanocrystals. We underline that the antidot-like shaped craters seem to be, because of morphology and size, promising candidates as hosts for 0-dimensional quantum structures.



Fig. 2: AFM topographies.

In our search for different well controlled morphologies, we deposit 8 MLs of MnTe instead of pure Te on the precursor Mn crystallites (Fig.1(C)). After a Mn island is nucleated, the strain ε caused in the island by lattice mismatch is partially relaxed at the price of inducing an extra strain in the substrate and increasing the strain in the wetting

layer near the crystallite edge. Therefore, adatoms deposited on the wetted surface will have to overcome an energy barrier $\Delta \mu_s$ before they can attach to the island [15]. During successive growth, the evolution of the morphology is also influenced kinetically by surface stress, since adatoms tend to diffuse on the surface away from sites with high strain [16]. The strain concentration at the island edge increases monotonically with the island size; when it exceeds a critical value, the free energy for atoms to occupy a position at the island edge may become higher than that for atoms to occupy a crystallographically unusual, but less strained site [15]. These considerations explain why the growth of MnTe is hampered at the edges of the crystallites and tends to develop far from the borders of precursor Mn islands and generate the 'sombrero'-like features shown in Fig.2(C).

Finally, after the deposition of Te and successive 15 MLs of CdTe followed by 8 MLs of MnTe on the precursor Mn island (Fig.1(D)), we obtain a quasi-periodic arrangement of equally shaped 'boxes' with very regular squared bases of 200 nm x 200 nm and height of 20 nm (Fig.2(D)). Despite the presence of these features on the surface, the RHEED pattern appears streaky 2x1, due to the high density and the ML-scale flatness of the islands' top. The structures show the tendency to arrange along the [100] and [010] crystallographic directions, as predicted [17] for a stable array of islands on a (001)oriented surface. Thermodynamic calculations have shown that after an island is nucleated the system free energy decreases monotonically with increasing island size [10]. Thus, a free energy minimum at a certain size is required in order to explain why observed islands' sizes tend to be so uniform. One should bear in mind not only the energetics, but also the kinetics, which implies that the islands' height grows slowly compared to the basis and may be treated as roughly constant. The kinetics can be incorporated by minimizing the total island energy with respect to width and length of the crystallite keeping the height constant. The result is that, in thermodynamic limit, with high density of islands, they should grow until each nanocrystal is square-based. This morphology represents the optimal trade-off between surface energy and strain. In our case the 'boxes', after reaching the squared-basis configuration, do not undergo further ripening and shape and basis size keep constant. Additional growth of MnTe leads to an increase of the crystallite height.

3. Conclusions

In conclusion, we achieved the reproducibility of self-assembling Mn-based nanocrystals, by monitoring in real time the subsequent stages of the growth process. The extension to other material systems and growth techniques would be straightforward, the RDS being suitable for MBE as well as for non-ultra-high-vacuum systems like chemical vapor deposition (CVD) reactors.

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Molecular Beam Epitaxy Growth of 3D Quantum Dot Crystals

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The self-organization of pyramidal PbSe islands that spontaneously form during strained-layer epitaxial growth of PbSe/PbEuTe superlattices results in the formation of three-dimensional quantum-dot crystals. In these crystals, the dots are arranged in a trigonal lattice with a face-centered cubic (fcc)-like ABCABC... stacking sequence. As shown by theoretical calculations, the elastic anisotropy in these artificial dot crystals acts in a manner similar to that of the directed chemical bonds of crystalline solids.

1. Introduction

The spontaneous formation of nano-scale three dimensional (3D) islands during strained-layer heteroepitaxy has recently emerged as novel technique for fabrication of self-assembled quantum dots. It is based on the fundamental instability of highly strained surfaces that leads to nucleation of coherent islands on the surface after completion of the wetting layer. In multilayer structures, the buried dots tend to influence the dot nucleation in the subsequent layers due to long range elastic interactions. This usually results in a vertical alignment of the dots, but may also lead to an ordering in the lateral direction. This could lead to improved quantum dot size homogenities, which is of crucial importance for device applications.

2. Experimental Results

In the present work, we have investigated the evolution of vertical and lateral correlations in self-assembled PbSe/PbEuTe quantum dot superlattices grown by molecular beam epitaxy on PbTe (111) surfaces. In these superlattices, the composition of the ternary layer was adjusted to achieve a complete strain symmetrization of the superlattice stack, which allows the growth of an unlimited number of superlattice periods without misfit dislocation formation. Atomic force microscopy (AFM) investigations (Fig. 1) indicate a nearly perfect hexagonal ordering of the PbSe quantum dots within the layers as the number of superlattice periods increases. From high resolution x-ray diffraction and transmission electron microscopy (TEM) studies we find that the vertical correlation of the dots is not parallel but inclined with respect to the growth direction. As a consequence, an ABCABC... vertical dot stacking sequence is formed, similar to the stacking of the closely packed (111) planes in fcc-lattices.



Fig. 1: AFM images of (a) a single PbSe quantum dot layer and of the top PbSe layer of strain symmetrized PbSe/PbEuTe dot superlattices after (b) 10 and (c) 100 periods. This indicates a rapid evolution of hexagonal ordering within the dot layers, which is evident also from the 2D power spectra of the AFM images shown in the inserts.



Fig. 2: Cross-sectional TEM image of a 30 period PbSe/PbEuTe quantum dot superlattice showing the high degree of lateral and vertical order in the structure that starts already within the first few superlattice periods. The PbSe thickness was 5 monolayers and the PbEuTe spacer thickness 480Å in this sample. The right hand panel shows the fcc-like ABCABC vertical dot stacking sequence deduced by TEM as well as by high resolution x-ray diffraction.

As shown in the cross-sectional TEM image in Fig. 2, the ordering in the dot superlattices is so efficient that nearly perfect trigonal quantum dot crystals are formed. Even more, for different superlattices we find that the trigonal angle of the dot lattice remains essentially constant, which means that the in-plane dot-dot separation can be tuned continuously just by changing the spacer thickness.

3. Theoretical Calculations

In order to explain the 3D dot arrangement in the superlattices we have developed a model for calculation of the elastic energy distribution on the surface above buried Stranski-Krastanow islands taking into account the elastic anisotropy as well as surface relaxation. For (111) growth of the highly anisotropic IV-VI materials we find that the energy minimum is not directly above a buried dot but instead three side minima occur. As shown in Fig. 3a, these minima are laterally displaced along certain crystallographical directions and serve as preferential nucleation sites for the dots in the subsequent layer. This leads to the ABCABC... vertical stacking as well as the in-plane hexagonal ordering that is observed in our experiments.

Similar calculations were performed for other semiconductors and other growth directions. We find a systematic dependence of the strain distributions on the elastic anisotropy ratio $A = 2c_{44}/(c_{11}-c_{12})$ that reflects the ratio between the Youngs moduli along the <111> and <100> directions. For rock salt type materials with A < 1, an ordering similar to the PbSe/PbEuTe system is predicted, with a linear increase of the trigonal correlation angle when the elastic anisotropy increases (Fig. 3c). For the diamond and zinc-blende type semiconductors with A > 1, side minima appear only for the (001) surface orientation, which could result in a centered tetragonal dot arrangement (ABAB... stacking) if the elastic anisotropy is sufficiently large (Fig. 3b).



Fig. 3: (a) Normalized elastic energy density $\rho(x,y)$ above a strained quantum dot at 50 nm below the surface for various matrix materials and the (111) surface orientation. The curves represent cross-sections of ρ in the directions *r* indicated by arrows in the 2D contour plots. (b) Angle α relative to the surface normal under which the minima of $\rho(x,y)$ appear on the (001) and (111) surfaces vs. elastic anisotropy ratio $A = 2 c_{44}/(c_{11}-c_{12})$. The inserts show the expected dot superlattice stacking.

References

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Appendix

Program of the Seminar Aktuelle Entwicklungen der Mikroelektronik (Current Developments of Microelectronics) Bad Hofgastein, March 3 – 6, 1999

Wednesday, March 3, 1999 17:00 – 20:15 High Frequency Systems

- 17:00 18:00 KARL-REINHARD SCHÖN HF-Technologie- und Schaltungskonzepte für Mobilfunkanwendungen Invited Paper
- 18:00 19:00 FRANCO MALOBERTI High Speed Data Converters and New Telecommunication Needs Invited Paper
- 19:00 19:15 Break
- 19:15 20:15 ERICH PFAFFELMAYER Sicherheitsrelevante Systeme in der Flugsicherung Invited Paper

Thursday, March 4, 1999 09:00 – 11:30 High Frequency Systems (continued)

- 09:00 09:30 NIKOLAUS KERÖ ASIC-Design-Zentren an österreichischen Universitäten Invited Paper
- 09:30 10:00 HARTWIG W. THIM MMIC-Forschung und -Entwicklung an österreichischen Universitäten Invited Paper
- 10:00 10:30 Coffee
- 10:30 10:50 H. LEOPOLD, <u>H. SENN</u> Ein Zeit-zu-Spannungs-Umsetzer für genaue Laufzeitmessungen
- 10:50 11:10 <u>C. FÜRBÖCK</u>, M. LITZENBERGER, E. GORNIK, R. THALHAMMER, G. WACHUTKA, N. SELIGER *Laserprobing zur internen Charakterisierung von IG-Bipolar-Transistoren*
- 11:10 11:30 <u>R. FASCHING</u>, F. KOHL, R. CERNICSKA, M. BRANDL Eine neue Technologie für den Zusammenbau von ASICs and MEMS

Thursday, March 4, 199917:00 - 20:15Optoelectronics

- 17:00 18:00 <u>A. ULLRICH</u>, N. STUDNICKA 3D-Laser-Entfernungsbildaufnahme Invited Paper
 18:00 – 19:00 MARKUS-CHRISTIAN AMANN Neueste Entwicklungen auf dem Gebiet der III-V Heterostrukturlaser Invited Paper
 19:00 – 19:15 BREAK
 19:15 – 20:15 HANNO WACHERNIG
 - In-situ–Spurenüberwachung mit abstimmbaren MIR Diodenlasern Invited Paper

Friday, March 5, 199909:00 - 10:00Optoelectronics (continued)

- 09:00 09:20 G. SPRINGHOLZ, T. SCHWARZL, <u>W. HEISS</u>, H. SEYRINGER, S. LANZERSTORFER, H. KRENN Herstellung von Bragg-Spiegeln für den mittleren Infrarot-Bereich mit hohem Wirkungsgrad aus IV-VI Halbleitern
- 09:20 09:40 <u>P. O. KELLERMANN</u>, N. FINGER, W. SCHRENK, E. GORNIK, H.-P. GAUGGEL, R. WINTERHOFF, M.H. PILKUHN Adjustierbare oberflächenemittierende Single-Mode Laserdioden mit kontradirektionaler Oberflächenmoden-Kopplung
- 09:40 10:00 Coffee

Friday, March 5, 1999 10:00 – 11:00 Special Paper High Frequency Devices

10:00 – 11:00 MARTIN SCHATZMAYR Prozeβentwicklung eines SiGe-BiCMOS-Prozesses für ASIC-Anwendungen Invited Paper

Friday, March 5, 1999 11:00 – 12:00 Poster Session Optoelectronics

A. BONANNI, H. SEYRINGER, K. HINGERL, H. SITTER, D. STIFTER Self-Assembling Mn-Based Nanostructures

N. FINGER, P. O. KELLERMANN, W. SCHRENK, E. GORNIK Analysis of Single-Mode Grating Coupled Twin Waveguide Laser Structures

M. GRITSCH, H. HUTTER, L. HOLZER, S. TASCH Investigation of Local Ions Distributions in Polymer Based Light Emitting Cells W. HEISS, G. PRECHTL, D. STIFTER, H. SITTER, G. SPRINGHOLZ, L. TOTH *ZnCdSe/ZnSe Quantum Wires by Epitaxy on Prepatterned GaAs Substrate*

L. HVOZDARA, S. GIANORDOLI, G. STRASSER, K. UNTERRAINER, E. GORNIK GaAs/AlGaAs Based Intersubband and Interminiband Mid-Infrared Emitters

S. LANZERSTORFER, M. STEPIKHOVA, H. PREIER, L. PALMETSHOFER, W. JANTSCH Light Generation by Er in Si Related Materials

T. MAIER, G. STRASSER, E. GORNIK GaAs VCSELs with Dielectric Si₃N₄/SiO₂ Mirrors

S. MUSSER, H. HUTTER, P. WILHARTITZ Determination of Trace Element Distribution in Cr Sputter Targets by 3-d SIMS

W. SCHRENK, N. FINGER, T. MAIER, P. O. KELLERMANN, G. STRASSER, E. GORNIK GaAs/AlGaAs/InGaAs Bandgap Lasers — From DH Lasers to VCSELs

J. ULRICH, R. ZOBL, K. UNTERRAINER, G. STRASSER, E. GORNIK, K. D. MARANOWSKI, A. C. GOSSARD *Far-Infrared Electroluminescence in Parabolic Quantum Wells*

Friday, March 5, 199917:00 – 20:15High Frequency Devices

- 17:00 18:00 <u>HARTMUT PRESTING</u>, ULF KÖNIG Stand und Anwendungen von Si/SiGe-Hochfrequenz- und Optoelektronik-Bauelementen **Invited Paper**
- 18:00 19:00 ANDREAS SCHÜPPEN Stand der Prozeβentwicklung und Markteinführung des SiGe-HBT Invited Paper
- 19:00 19:15 BREAK
- 19:15 20:15 HARTMUT KAPUSTA GaAs-MMIC Design-Aspekte für Massenproduktion Invited Paper

Saturday, March 6, 1999 09:00 – 11:00 High Frequency Devices (continued)

- 09:00 10:00 FRIEDRICH SCHÄFFLER Hoch- und Höchstfrequenz-Bauelemententwicklung an österreichischen Universitäten Invited Paper
- 10:00 10:20 Coffee
- 10:20 10:40 <u>K. WIESAUER</u>, G. SPRINGHOLZ Nanolithographie für Halbleiter-Nanostrukturen unter Verwendung von Rasterkraftmikroskopie

10:40 – 11:00 <u>A. LUGSTEIN</u>, H. WANZENBÖCK, E. BERTAGNOLLI Fokussierte Ionenstrahlen, eine neue Technologie für die Mikrostrukturierung im Bereich unter 100 Nanometern

Saturday, March 6, 1999 11:00 – 12:00 Poster Session High Frequency Devices

R. HEER, J. SMOLINER, G. STRASSER, E. GORNIK Enhanced Energy Resolution in Ballistic Electron Emission Microscopy Through InAs Base Layers

C. RAUCH, G. STRASSER, AND E. GORNIK Onset of Scattering Induced Miniband Transport

N. SANDERSFELD, H. SEYRINGER, G. STEINBACHER, L. PALMETSHOFER, S. ZERLAUTH, F. SCHÄFFLER Modulation Doped Si/Si_{1-x}Ge_x-Field-Effect Transistors

C. SCHELLING, G. SPRINGHOLZ, F. SCHÄFFLER Growth Instabilities in Si Homoepitaxy

TH. SCHWARZL, W. HEISS, G. KOCHER-OBERLEHNER, G. SPRINGHOLZ CH₄/H₂ Plasma Etching of IV-VI Semiconductors

H. SEYRINGER, B. FÜNFSTÜCK, F. SCHÄFFLER *Electron Beam Lithography of Nanostructures*

J. STANGL, Y. ZHUANG, G. BAUER C. ROSENBLAD, H. VON KÄNEL Fast Growth Method for the Fabrication of Modulation Doped Si/SiGe Field Effect Transistors

Y. ZHUANG, P. MIKULIK, V. HOLÝ, G. BAUER, R. HAMMOND, T. E. WHALL, E. H. C. PARKER Si/SiGe Layers on Patterned Substrates for MODFET Applications

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