

Growth Instabilities in Si Homoepitaxy

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We report on a new type of growth instability in Si homoepitaxy that arises from a slight sample miscut. This instability leads to a considerable surface roughness of up to 20 Å on a distance of 250 nm and occurs in a temperature regime frequently used for Si buffer growth. We also provide a recipe to avoid surface roughening.

1. Introduction

The technical relevance of Si (001) surfaces and interfaces caused strong interest and intensive research efforts in their growth properties. The Si surface shows a general tendency for roughening during strained layer heteroepitaxy. Recently, some groups investigate this phenomenon that is commonly known as step bunching and try to amplify it to obtain templates for lateral ordering in subsequent self-organized growth, such as e.g. Ge islands.

The electronic properties of layers resulting from overgrowth are strongly influenced by their interface morphology as carrier scattering from interfacial roughness plays a major role for transport in heterostructure devices. Therefore, ideally flat Si and SiGe interfaces are indispensable prerequisites for optimum performance in present and future Si-based heterostructure devices. It is the goal of our work here to investigate the involved roughening mechanisms on the Si [001] surface and understand their driving forces to allow for the fabrication of interfaces that are as flat as possible and thus ideal for heterostructure devices.

2. Experiment

2.1 Experimental

The samples used for this study were cut from standard Si (001) wafers into 17×17 mm pieces. The substrates have well-defined miscuts of some 1° and 2° along the [100] and 1,5° along the [110] direction, respectively. We used an HF-free standard RCA cleaning procedure before loading them into our Riber SIVA 45 MBE machine. An oxide desorption step at 1000 °C initiates subsequent overgrowth. Si and SiGe layers were deposited at growth rates of 0,2 and 0,8 Å/s and growth temperatures between 350 °C and 750 °C, the layer thickness usually being 1000 Å.

After growth the surface morphology was immediately mapped in ambient air with a Park Scientific atomic force microscope (AFM) in contact mode.

2.2 Results

In Fig. 1, a series of $5 \times 5 \mu\text{m}^2$ AFM micrographs is depicted. The morphology undergoes a quite dramatic metamorphosis within this narrow temperature range: At 450°C , the surface shows a rather regular terrace structure perpendicular to the miscut direction with an average spacing of $0.25 \mu\text{m}$ and a height of just a few mono-atomic layers (ML; $1 \text{ ML} = 1.36 \text{ \AA}$). The period is more than an order of magnitude larger than the expected terrace width of 78 \AA for equally spaced ML steps leading to a 1° miscut. The slightly undulating pattern is characteristic for the low temperature growth regime and persists at least down to temperatures of 350°C . At 490°C , the terrace structure is still present, but it is now covered with triangular features. Those line up almost perfectly along the $[100]$ miscut direction, forming ridge structures perpendicular to the terrace edges. At 550°C , remnants of the terraces and the ridges remain, but individual triangles can no longer be resolved. Upon further increase of the temperature the feature heights decrease until finally a flat surface results at 750°C .

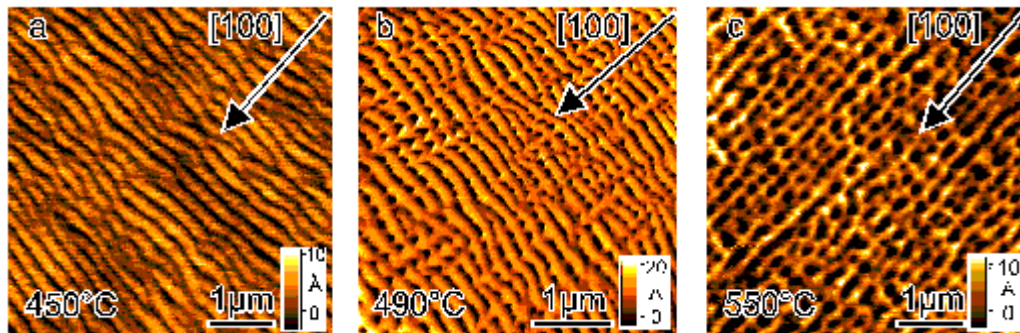


Fig. 1: $5 \times 5 \mu\text{m}$ AFM pictures of samples with 1° miscut along $[100]$. Films were deposited with 0.8 \AA/s at growth temperatures of (a-c) 450 , 490 and 550°C , respectively.

The evolution of the surface morphology was found to depend surprisingly little on the growth rate in the range between 0.2 and 0.8 \AA/s studied here. At 0.2 \AA/s the features, especially the triangles, become more regular (Fig. 2a), but both the lateral periods and the feature heights remain constant within experimental error.

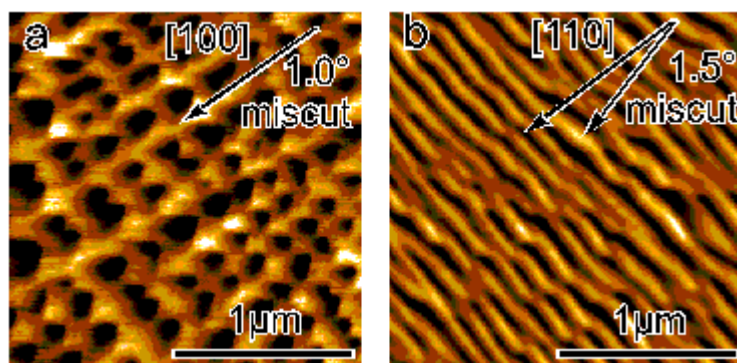


Fig. 2: The surface morphologies resulting from different miscut directions are quite variable. (a) shows a sample miscut 1° along $[100]$, (b) 1.5° along 10° off $[110]$. Both layers were deposited at 490°C and 0.2 \AA/s to a thickness of 1000 \AA .

The influence of the miscut direction was assessed by experiments on substrates having a 1.5° miscut along an in-plane direction 10° off $[110]$. An example is shown in Fig. 2b next to a $[100]$ miscut reference sample. Obviously, the terraces run perpendicular to the respective miscut direction, but in both cases the terrace edges disintegrate into zigzag arrangements of $\langle 110 \rangle$ segments.

For a characterization of the surface morphologies, we extracted the average period widths of the terraces and the average peak-to-valley height variations as a function of the growth temperature, miscut angle and direction (Fig. 3).

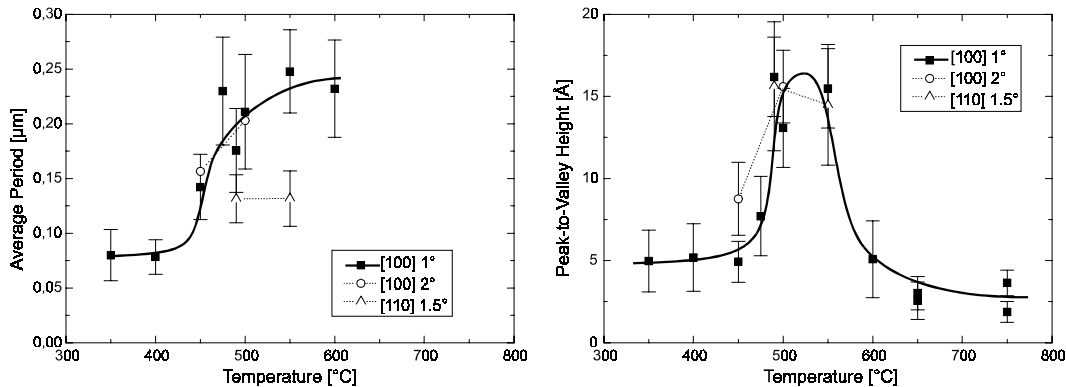


Fig. 3: The evolution of surface features is depicted as a function of growth temperature. (a) shows the development of the feature distance and (b) the height evolution.

The most prominent feature in Fig. 3 is the simultaneous tripling of both the period length and the amplitude over the temperature range. It should be noted that the roughest surfaces result at temperatures being quite commonly used for buffer growth, i.e. 500 – 550 °C. Beyond 550 °C the feature height decreases rapidly leading to a surface showing a non-correlated roughness of merely a few Å at 750 °C.

Subsequent annealing for sufficiently long times results in flat surfaces with a rms roughness of about 2 Å and no long-range correlation. Hence, the observed instabilities are kinetically driven and thermodynamically unstable.

RHEED oscillation measurements revealed that the evolution of the surface structures takes place entirely in the step flow regime.

2.3 Discussion

The striking difference in surface morphology between the sample miscut in the $[100]$ and $[110]$ direction gives strong evidence for an influence of the microscopic properties, namely the dimerization of the (001) surface, on the roughness morphology. In the case of a $[110]$ miscut two energetically different terrace edges exist: S_A steps are oriented parallel to the dimer rows on the upper terrace, and S_B steps perpendicular [1]. Initially, growth occurs mainly via S_B steps, since it is energetically more favorable to attach Si atoms to the end of a dimer row, but also because adatom diffusion is estimated to be 1000 times larger along the dimers [2], S_B step growth is mainly fed from the upper terrace as no step edge barrier (Schwoebel barrier) is present. Consequently, at low growth temperatures, S_B terraces are kinetically unstable and grow much faster. Faster growth in

return leads to a larger upper terraces, which again means a larger capture ratio, as compared to S_A type steps. In the end, this instability generally leads to step bunching and rough surfaces (see fig 2b). At somewhat higher temperatures, however, the diffusion perpendicular to the dimer rows becomes enhanced and finally the predominant diffusion asymmetry observed at lower temperatures is overcome, S_A steps advance as fast as S_B steps and the result is a flat surface.

The behavior of the [100] miscut samples is far more complex and not yet fully understood. The $\langle 110 \rangle$ segmentation can be understood as caused by “diffusion trenches” along the step edges, where diffusion barriers might be lower and adatoms are highly mobile. The almost perfect alignment of the triangles could be explained in terms of strain fields that are known to be connected with the surface dimer rows.

3. Conclusions

Considering the fact that every wafer is usually specified only within $\pm 0,5^\circ$ of an exact crystal plane the outcome of our experiments bears important implications for Si-based epitaxy. They clearly show that one has to be very concerned about Si buffer growth. Investigations on strain-induced step bunching should be carried out quite carefully. Bearing in mind that HF cleaned wafers cannot be overgrown at high temperatures because of the formation of SiC precipitates and as a consequence thereof the evolution of a considerable surface roughness. This leaves us in principal with two alternatives : Flat Si buffers on an HF cleaned wafer by either two successive buffer layers the first grown at a low temperature to avoid SiC precipitates to be formed and a second grown at higher temperatures above 600°C to smoothen the surface afterwards or annealing of the substrates after buffer growth. The second viable way to achieve a flat surface is to use RCA cleaned wafers. RCA cleaning leaves a nearly C-free oxidized wafer surface that thus can be overgrown with a Si buffer at temperatures above 650°C . This approach provides the surfaces best suited for heterostructure devices as well as future surface investigations.

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