SiGe Technology

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We report on the cleanroom activities in Linz with respect to Si-based technology. Two main topics are treated: molecular beam epitaxy (MBE) of Si and $Si/Si_{1-x-y}Ge_xC_y$ heterostructures, and e-beam nanolithography. In the former field we report on kinetic and strain-induced growth instabilities and their application for self-organized growth, the growth of modulation-doped Si/SiGe heterostructures with high mobilities and high carrier concentrations, and on the deposition of $Si/Si_{1-x-y}Ge_xC_y$ heterobipolar transistors on pre-processed wafers provided by an industrial partner. The structuring activities are concentrated on nanometer-lengths Schottky gates with T or Γ cross section realized by multi-resist-layer e-beam lithography and lift-off.

1. Molecular beam epitaxy

1.1 Kinetic versus strain induced growth instabilities

The lattice mismatch of 4% between pure Si and pure Ge has important implications for epitaxial growth. One of the most prominent features is the Stranski-Krastanov growth mode, which breaks up a compressively strained epitaxial film into islands. This growth mode is widely exploited for growing so called self-organized dots of the heteromaterial with the larger lattice constant. This works particularly well with InAs on GaAs, where the InAs dots can become small enough to show zero-dimensional behavior (”quantum dots”), and the first lasers have been demonstrated in this material combination.

Ge dots on Si are another example that found widespread interest in recent years. In the Si/SiGe heterosystem also strain-induced step bunching has been studied intensively [1], which was considered as a precursor to Stranski-Krastanov island formation. The basic idea behind strain-induced step bunching on slightly misoriented Si(001) substrates is that the strain of a SiGe layer causes an arrangement of flat terraces and macrosteps with a period that is typically 10 to 20 times larger than the natural terrace spacing at a particular miscut [2]. Several experiments seemingly supported that concept [3].

We recently discovered kinetic step bunching on the surface of homoepitaxial Si layers on miscut substrates [4], the appearance of which closely resembles the morphology that has so far been associated with strain-induced step bunching. But, since lattice-mismatch-induced stress is certainly absent in the homoepitaxial layers, and self-organization phenomena are potentially useful for the fabrication of nanostructures, it is important to distinguish strain-induced and kinetic growth instabilities. For this purpose we extended our homoepitaxial growth studies to $Si_{1-x}Ge_x$ films with Ge concentrations between 5 and 50%. To separate the kinetic growth effects of the Si buffer from the strain effects of the SiGe layers, each epilayer sequence was deposited simultaneously on three 18x18 mm^2 substrates with different miscuts: One singular (001) substrate with

miscut < 0.1°, and two substrates with miscuts around 1° and miscut azimuths along [100], and [110], respectively. Also, the deposition temperature for the Si buffer layer (typical 1000 Å thick) was varied between 500 °C, where we found the maximum corrugation height of the 1° miscut samples, and 750 °C, where the buffer layers are atomically smooth with an uncorrelated rms roughness of typically 2 – 3 Å.

The outcome of our experiments is rather surprising: We found no indication for strain-induced step-bunching under either of the conditions where such an effect was claimed in the literature. Whenever we start with a smooth silicon buffer, the subsequent SiGe layer remained smooth up to a maximum Ge concentration $x_{m.}$ beyond which the films disintegrated into Stranski-Krastanov islands rather than linear step bunches. x_m depends on the deposition temperature, and amounts to about 50% at 550 °C. Vice versa, whenever we started with a kinetically step-bunched Si buffer, the subsequent $Si_{1-x}Ge_x$ film with $x < x_m$ virtually replicated the morphology of the substrate (Fig. 1). This finding also applies to Si/SiGe superlattices, the morphological appearance of which depends exclusively on the morphology of the initial Si buffer.

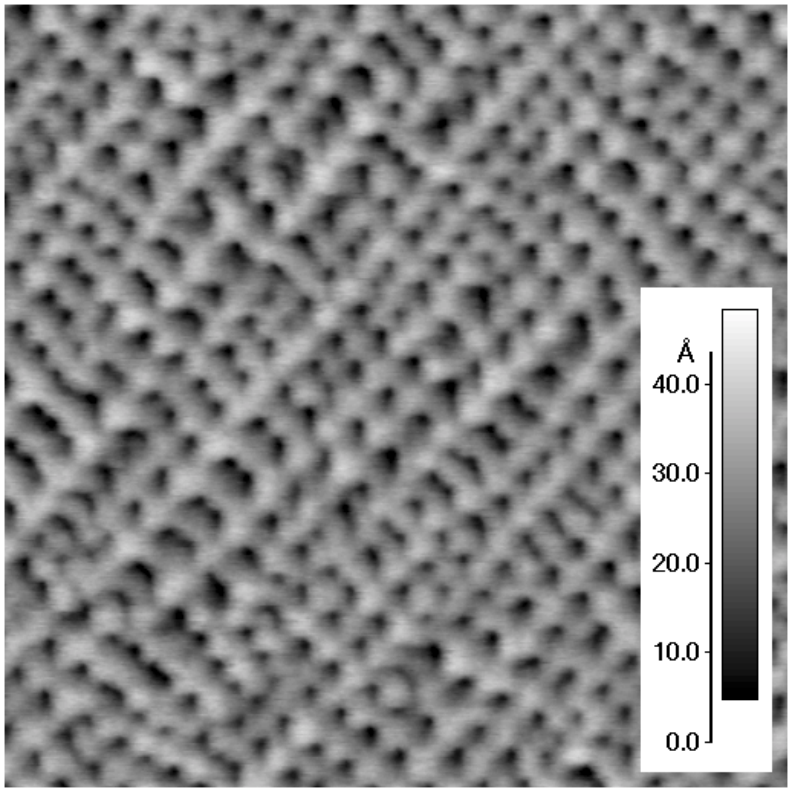

Fig. 1: 25 Å of $Si_{0.75}Ge_{0.2}$ deposited on top of a kinetically roughened Si buffer layer on a 1° miscut Si (001) substrate. No strain-induced effects are observed: the SiGe layer just replicates the morphology of the buffer. Compare also Ref. [4].

These results are important for a variety of growth phenomena in Si/SiGe epitaxy: (i) By optimizing the Si buffer, the interfaces between the Si barriers and a pseudomorphic SiGe hole channel can be made almost atomically flat. Interface roughness scattering, which has been discussed in the literature as a relevant scattering mechanism in such quantum well structures [5], can this way be suppressed. (ii) Step bunching associated with a Si buffer can be converted into an inhomogeneous strain field by adding a SiGe

film that replicates the morphology. Such an arrangement has already been used for aligning subsequent Ge dots [6], but the mechanism has incorrectly been attributed to strain-induced step bunching of the SiGe film. With our new results, the pattern formation can now be efficiently designed, because it is entirely due to the morphology of the Si buffer, which can be varied by fine-tuning of the miscut and growth parameters [4].

1.2 Growth of modulation-doped Si/SiGe FETs

So far, we have tried to optimize the low temperature mobilities of Si/SiGe modulation-doped structures, in order to establish the best possible growth conditions. However, for FET applications the channel conductivity has to be optimized, which requires a compromise between carrier density and mobility. We therefore tried to increase the number of carriers in the channel by doping both SiGe barriers, and to keep the mobility high, by retaining the undoped spacers adjacent to the strained Si channel. Such a layout was optimized by self-consistent calculations, which yield asymmetric doping concentrations because of the symmetry-breaking presence of the Schottky gate. For a given spacer thickness, which was applied to either side, the doping concentrations where adjusted such that under conditions of maximum carrier transfer into the channel both doping supply layers are completely depleted.

The main problem with the additional doping layer on the substrate side of the channel is dopant segregation into the spacer, and even into the channel. To reduce this effect low-temperature doping and a subsequent thermal flash-off of excess dopants was applied for the doping supply layer on the substrate side. The thermal-flash-off has the additional benefit of an annealing step, which reduces the number of defects that might have formed during the low temperature doping.

The results are promising: We measured on double sided doped Si/SiGe MODFET structures carrier densities of $1.3 \cdot 10^{12}$ cm^{-2}, and still maintained low-temperature mobilities of 65,000 cm^2/Vs. For comparison, a typical MOSFET has under such conditions a mobility that is at least a factor of 5 lower.

1.3 Si/$Si_{1-x-y}Ge_xC_y$ Heterobipolar Transistor (HBT)

SiGe-HBTs are now widely introduced into the production lines for high speed bipolar and BiCMOS circuits, because they offer a speed advantage of at least a factor of two without sacrificing the compatibility to standard Si technologies. A general problem of Si technology is transient enhanced diffusion (TED) of the only useful acceptor element, boron, upon injection of Si self interstitials. The latter are created during thermal oxidation and also during the annealing step of the emitter implant. As has been reported in our last annual report, the addition of less than 0.5 at.% of carbon to the SiGe base can drastically reduce transient enhanced boron diffusion of the base dopant into collector and emitter. Therefore, several HBT producing semiconductor companies and manufacturers of chemical vapor deposition (CVD) reactors are presently working on a reliable process for the controlled deposition of $Si_{1-x-y}Ge_xC_y$:B base layers. CVD is the standard epitaxial deposition technique for Si, mainly because of the high throughput and the excellent reproducibility. On the other hand, changing growth parameters in a CVD process is a tedious task, because of the complex growth kinetics and chemistry. MBE is much more flexible, because of the large supersaturation and the absence of gas phase and surface chemical reactions. It is therefore an obvious step to optimize doping

and composition profiles by MBE, and subsequently transfer the results to the CVD reactor in the production plant.

With this in mind we started a FFF-funded collaboration with Austria Mikrosysteme (AMS) in Unterpremstätten. The efforts to develop optimized HBT profiles with SiGeC base are twofold. On the one hand, layer sequences are deposited on unstructured substrates, large-area implanted and annealed. These reference samples serve for structural investigations. They are mainly characterized by x-ray, SIMS and optical spectroscopy to optimize the Ge, carbon and boron profiles. Even more important is the electrical characterization on real devices that have seen the complete fabrication process. For this purpose we overgrow by MBE preprocessed wafers provided by AMS. These have seen all process steps prior to the deposition of the $Si_{1-x}Ge_x$:B or $Si_{1-x-y}Ge_xC_y$:B base layer, and were subsequently reintroduced into the production line and processed to operational circuits. With some adjustments to our regular cleaning and epi-deposition process, we were able to demonstrate device-quality epi-layers. Also, the MBE process was found to be compatible with the CMOS part of the circuits, which was almost completed before MBE overgrowth. With these results an essential precondition for the optimization of the layer sequence has been fulfilled. The next steps will now be to optimize the HBTs with respect to their electrical and structural properties under genuine fabrication conditions.

2. E-beam lithography

2.1 Shadow masks for selective silicon epitaxy

While epitaxial layers allow vertical structuring with resolutions down to the thickness of an atomic layer, lateral nanostructuring is limited by the lithographic resolution, which is in most cases further hampered by inhomogeneous damage induced by reactive ion etching (RIE). Selective epitaxy is an alternative, which allows vertical and lateral structuring as the epilayers are deposited. This requires an adequate mask layer on the substrate, which has to be compatible with the epitaxial process and permits selective growth in the windows that expose the substrate.

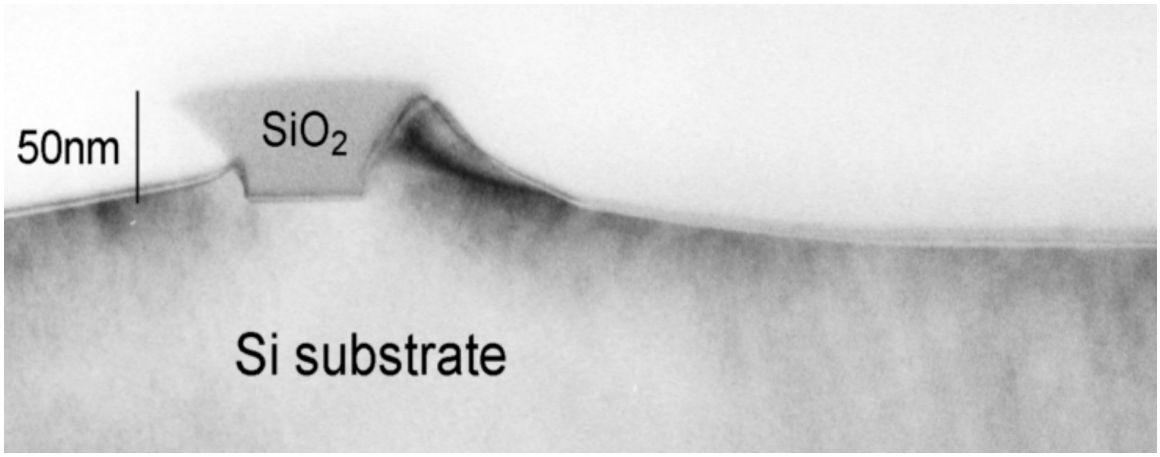

Fig. 2: Cross sectional TEM micrograph of a SiO_2 wire on a Si substrate after thermal heating at 950 °C in an UHV environment.

For Si epitaxy an SiO_2 mask is perfectly suited: It leads to epitaxial growth in the windows and to polycrystalline growth on the mask in the case of MBE and low-temperature CVD.

Under certain CVD growth conditions it is even possible to suppress deposition on the SiO_2, which is then a truly selective process, in contrast to the aforementioned standard c-Si/poly-Si process, which is occasionally referred to as "differential" epitaxy.

One of the main problems of differential epitaxy is the lateral boundary between the c-Si and poly-Si areas: Poly grains tend to grow into the c-Si areas and thus reduce the lateral resolution with respect to the resolution of the mask. Even worse, this boundary is electrically not well defined and can introduce undesired leakage currents. To overcome this problem, shadow masks have been introduced, which provide an undercut of the mask layer to separate the c-Si and the poly-Si areas by a physical gap. Frequently, a Si_3N_4/SiO_2 mask is employed, which is structured by RIE in a first step and then treated with an isotropic etchant that selectively attacks the lower lying SiO_2 layer to create the undercut. Because the second step is usually a wet chemical process (HF or BHF), the achievable resolutions are limited.

We could show that a defined undercut can be created thermally in a simple SiO_2 mask [7]. The basic mechanism is the same that is exploited for the thermal desorption of a natural oxide prior to MBE growth. A Si atom from the substrate has to diffuse to the SiO_2 surface to create SiO, which desorbs at high enough temperatures: $Si + SiO_2 \rightarrow 2\ SiO\uparrow$. In our experiments it turned out that at about 900 °C, when this reaction sets in, the surface mobility of Si atoms in the epi-windows is unexpectedly high, which leads to a significant mass transport. Since Si wets SiO_2, a surface flow of Si atoms toward the flanks of the SiO_2 mask occurs. These act as sinks because of the thermal desorption of SiO that consumes one Si atom for every SiO_2 molecule desorbed. Since the main source for the additional Si atoms is the exposed Si surface, SiO_2 desorption is more pronounced where the SiO_2 flanks are in contact with the Si substrate. This leads to the desired undercut, as is illustrated in Fig. 2.

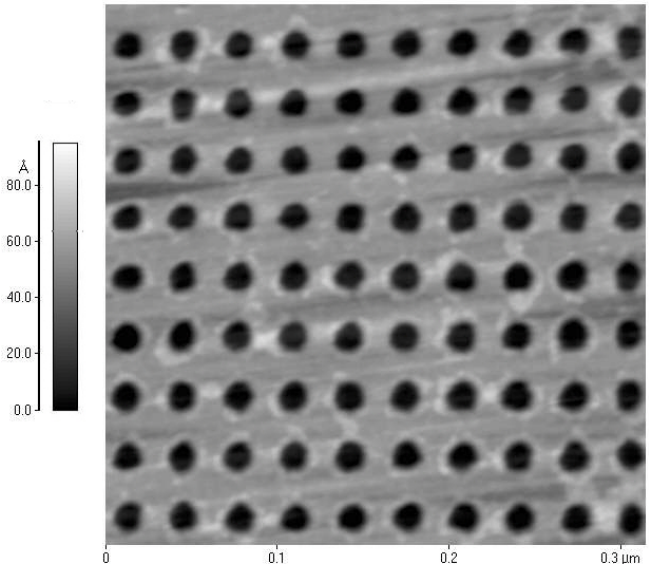

Fig. 3: E-beam lithographically structured dot-array with 150 Å diameter dots transferred into an SiO_2 layer by reactive ion etching.

It shows a cross sectional TEM micrograph of an array of SiO_2 wires, which had a rectangular cross section before the thermal treatment. The trapezoidal shape revealed in the figure is caused by the described mass transport at 950 °C in the UHV atmosphere of the MBE chamber, and can be fine-tuned by adjusting the temperature and the duration of the annealing step.

By proper exploitation of this mechanism we expect to be able to create shadow masks with lateral dimensions much smaller than had been possible so far. Figure 3 shows as a precondition a dot mask with hole diameters of 150 Å fabricated by e-beam lithography and RIE. The next step will now be to thermally create a shadow mask that leaves the upper diameter of the windows untouched, while producing the negative slope of the flanks. This way SiGe or Ge quantum dots could be deposited in an organized, and thus addressable, way.

2.2 Nanometer-length Schottky gates

Based on the five-layer transistor FET process with Schottky gate and implanted Ohmic contacts, which has been presented in the last report, the main emphasis was now put on the implementation of Schottky gates structured by e-beam lithography. Initially, we employed a single layer of PMMA for the lift-off process of the Pd/Au Schottky gates. With this simple process the parameters for mark recognition and exposure where derived. We also optimized the mesa separation of the devices, which is a critical process in Si because the surface is not naturally depleted as in most III-V materials. It turned out that mesa structuring prior to gate deposition is beneficial, especially when the gates overlap slightly with the mesa flanks. This way, complete pinch-off without any spurious parallel channel could be achieved. Figure 4 shows in the upper part SEM micrographs of a complete transistor without gate pad (right hand side), and of the gate region (left hand side) of a transistor with a 100 nm gate. The lower part shows the I-V characteristics of this device, which demonstrates the excellent pinch-off behavior at a gate voltage of –0.3 V. Due to the high Schottky barrier of 0.9 eV for Pd on n-Si, forward-bias voltages up to 0.4 V could be applied without significant leakage currents. The rather small absolute current levels are due to the relatively large gap between source and drain, which adds series resistance, and the relatively low carrier concentrations of this particular device, which was still based on a single-sided doping supply layer. The new double-sided doped layer sequences and a mask redesign with reduced source/drain gap will significantly improve these shortcomings.

After demonstrating the capability of our e-beam system to produce 100 nm gates with a single layer approach, multi-layer resist schemes were implemented to reduce the Ohmic resistance along the metal gate structure. This is important for high-frequency applications, and is usually achieved by gates with a T or Γ shaped cross sections. This way the contact area, and thus the effective gate length, can be kept in the nanometer range, whereas a low Ohmic resistance is achieved by the lateral expansion of the cross section above the contact area.

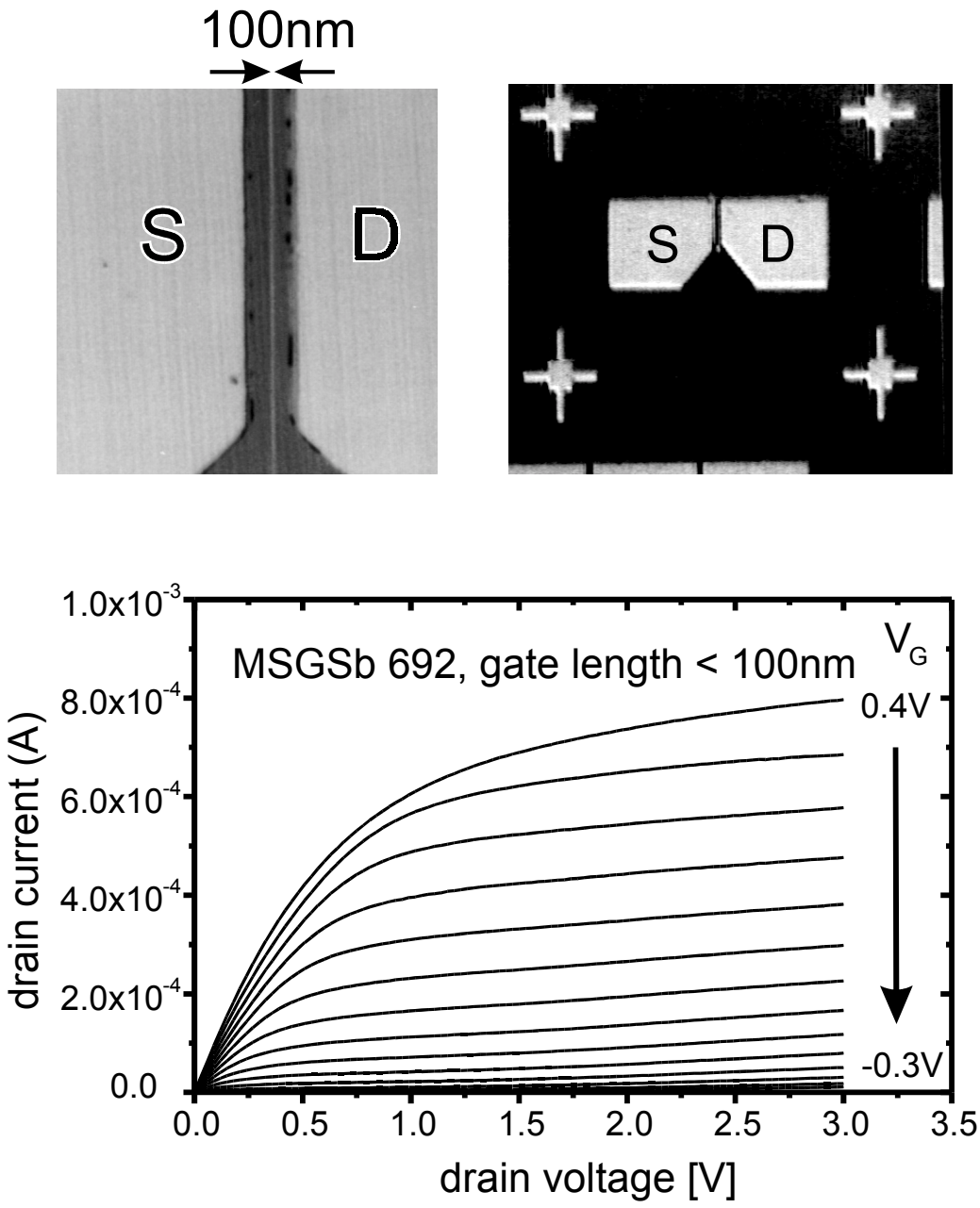

Fig. 4: SEM micrographs and I-V characteristics of a Si/SiGe MODFET with 100 nm gate.

Figure 5 shows an example of a T gate fabricated this way. The process involved three layers of resist, namely low sensitivity PMMA layers in the contact area and as a top resist, and a high sensitivity copolymer in between. e-beam exposure consists of three lines written with different doses: The middle line defines the contact area, which yields about 150 nm gate length in the depicted example. The two outer lines define the wings of the T, and were kept at a low enough dose to expose the copolymer, but not the PMMA layers. This scheme creates a negative flank due to the insensitive upper PMMA layer and such allows for easy lift-off even of gate films whose thickness approaches that of the three layer resist system. Further improvements aim now toward higher aspect ratios by employing thicker resist layers. This requires an optimization process, because thicker layers are concomitant with reduced resolution.

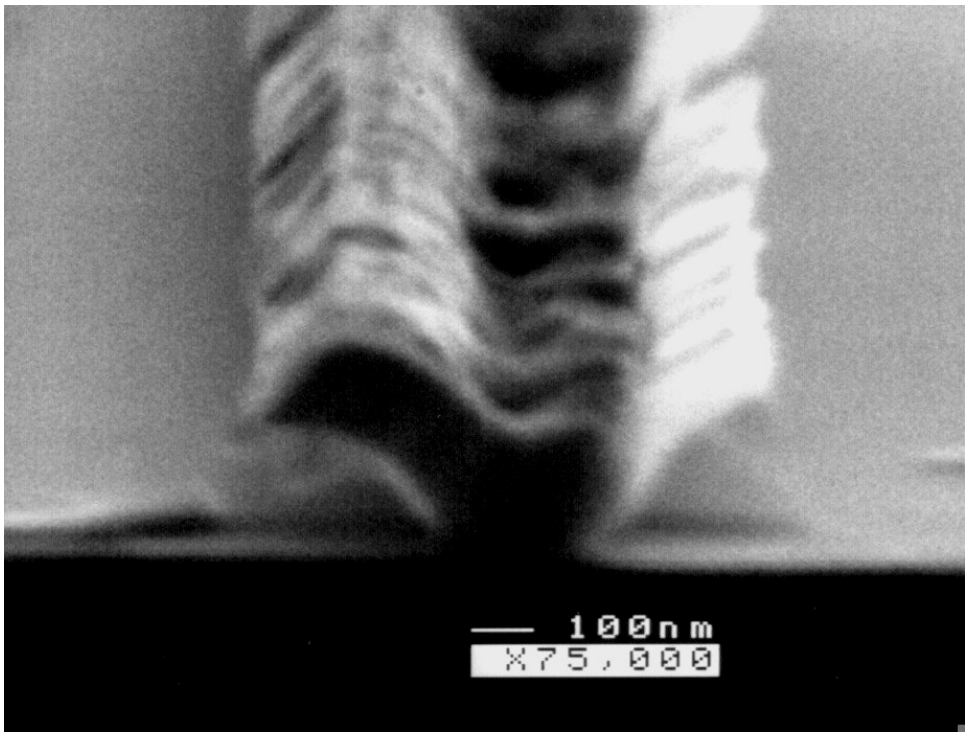

Fig. 5: Cross section of a T gate with a gate length of 150 nm.

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