BASICS AND TECHNOLOGY OF ELECTRONIC DEVICES

PROCEEDINGS OF THE SEMINAR
"GRUNDLAGEN UND TECHNOLOGIE ELEKTRONISCHER BAUELEMENTE"
IN GROSSARL / PONGAU
ORGANIZED BY THE SOCIETY FOR MICROELECTRONICS
(GESELLSCHAFT FÜR MIKROELEKTRONIK – GMe)

19 March 1997 – 22 March 1997

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GESELLSCHAFT FÜR MIKROELEKTRONIK

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FORSCHUNGSFÖRDERUNGSFONDS FÜR DIE GEWERBLICHE WIRTSCHAFT

BUNDESMINISTERIUM FÜR WISSENSCHAFT UND FORSCHUNG

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Seminar Program

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Preface

Almost exactly twenty years ago, from 30 March through 2 April 1977, the first Austrian microelectronics technology seminar took place in Grossarl, Salzburg, under the title "*Technologie in der Mikroelektronik*" ("*Technology in Microelectronics*"). A long series of biennial seminars followed, the first of which were organized by a group of institutes at the Technical University Vienna. Later, after the Society for Microelectronics (*Gesellschaft für Mikroelektronik*; GMe) had been founded in the mid-1980s, the GMe coordinated the Grossarl seminars.

The Society for Microelectronics is based on a concept designed by Fritz PASCHKE and by Norbert ROZSENICH and Hermann BODENSEHER as the key representatives of the Austrian Ministry for Science and Research. The main goal of the Society is to promote microelectronics research and technology at Austrian universities and to establish links to the Austrian industry. The GMe is essentially financed by the government and supports all relevant microelectronics activities at Austrian universities. The relatively small budget of the GMe prohibits the full sponsoring of research projects; nevertheless, the GMe supplements other research funding sources by providing contributions for creating and maintaining laboratory infra-structure. In addition to support for other technological activities in the fields of design, sensors, and optoelectronics, the main goal of the GMe in recent years was the support of the two cleanroom centers at the Technical University Vienna and at the University Linz, respectively, where internationally competitive technological equipment has been made available to researchers and students.

This development strongly affected the scope and target of the Grossarl seminars: While the first seminars were a rather sealed-up Austrian only affair, with an occasional foreign guest speaker, the scope has changed to the style of an international workshop, with the aim to maintain contacts to and cooperations with foreign universities and with the industry. The number of invited guest speakers was therefore increased, and the number of short contributions by Austrian academic groups was limited. In this year's program, five of the seven invited speakers are industrial researchers. A panel discussion is planned along with the technical presentations, where aspects of research management at academia *and* industry will be discussed.

This year, the proceedings will be published in English (although most of the presentations are to be held in German). This takes into account the large number of international requests we received for the proceedings of the latest seminar in 1995. We hope that the proceedings thus will promote the impact of our seminar and that they may contribute to an even better international cooperation of the Austrian microelectronics researchers.

Prof. Dr. Erich GORNIK
President of the GMe

Univ.-Doz. Dr. Karl RIEDLING
Secretary General of the GMe

Microwave and Millimeterwave Sensors Based on Flip-Chip and SAW Technology

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Wireless sensing plays an important role in industrial automation, domestic systems and transportation. Microwave and millimeterwave sensors offer high resolution and reliable operation in rough environments. Novel attractive sensor modules for the 24, 61 and 77 GHz frequency bands are feasible by the use of flip-chip (FC) and Surface Acoustic Wave (SAW) devices.

Drahtlose Sensorik spielt eine wichtige Rolle in der industriellen Automatisierung, im privaten Haushaltsbereich und in der Verkehrstechnik. Mikrowellen- und Millimeterwellen-Sensoren bieten hohe Auflösung und arbeiten selbst unter rauhen Umgebungsbedingungen zuverlässig. Der Einsatz von Flip-Chip- und Oberflächenwellen-Bauelementen ermöglicht die Realisierung neuartiger, attraktiver Sensormodule für die Frequenzbereiche bei 24, 61 und 77 GHz.

1. Introduction

Multiple wireless sensor functions will be implemented in future railroad and automotive traffic management systems [1], in the field of industrial process automation [2] and in domestic environments [3]. A particular advantage of microwave sensors is their robustness with regard to variable environmental conditions, such as dirt and temperature. Microwave technology is opening up important commercial applications [4], including

- position and speed measurements for railroad vehicles,
- forward-looking radar and park distance control for cars,
- liquid-level sensing for industrial process control,
- presence detection and object recognition for intelligent domestic systems,
- vehicle identification and traffic monitoring systems,
- on-line diagnosis of turbine engines in power engineering.

Up to 100 GHz, high-resolution sensors can be operated in the ISM (industrial, scientific, medical) frequency bands at 24.0 - 24.25 GHz and 61.0 – 61.5 GHz. For automotive radar, the range 76.0 – 77.0 GHz is designated. Higher frequencies offer better resolution and small antenna size; however, technical realization usually becomes more expensive with increasing frequency, which stands in contrast to the low-cost requirements in high-volume sensor applications.

2. Flip-Chip Technology

The engineering potential of microwave sensors can be better and more cost-effective utilized by combining the specific advantages of different component and material technologies. Among other things, this results from the fact that the different and partly competing technologies in many cases offer complementary technical properties. The combination of these features into a functionally optimized microwave system requires reliable and reproducible assembling technologies [5].

At very high frequencies, a conventional SMD production, being used in high-volume consumer electronics (e.g. satellite receivers), encounters technical limitations. The mechanical dimensions of the package and the related parasitic electrical effects (e.g. phase shift, attenuation) are no longer negligible. Even when using wirebonded chips, additional compensation networks are needed. Generally, the lack of reproducibility, caused by varying interconnection length and coarse placement accuracy, often requires expensive circuit tuning. Although recently developed adaptive bonding techniques [6] can correct rough mismatching, they do not solve the problem of attenuation and radiation of wirebonds and are tuning methods themselves.

These constraints are overcome by using flip-chip assembly, which provides extremely short connections. As shown in Fig. 1, the microwave devices are directly connected face-down onto a ceramic or glass substrate. Small gold bumps with a typical diameter of 50 µm are providing the contact. The substrate, processed in thin film technology, includes all passive structures. Before flip-chip bonding, the bumps are applied to the substrate. The flip-chips are then connected to the substrate with thermocompression.

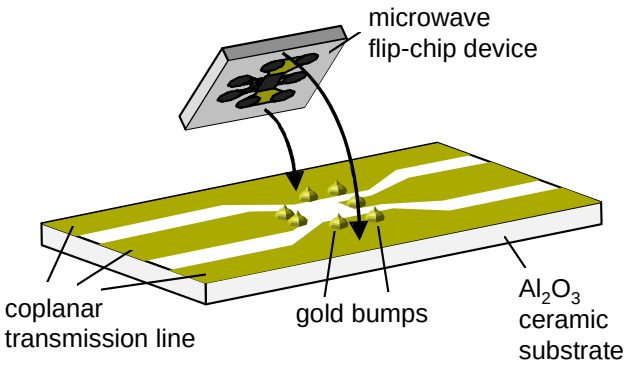

Fig. 1: Flip-chip bonding of microwave devices.

Flip-chip technology has been used in the production of digital circuits (e.g. ball grid arrays, FC soldering) for some time now, whereas FC bonding of microwave and mm-wave devices is still new. The technological basis for this progressive technique is currently in development [7 – 9].

FC bonding demands no special chip devices. By using a coplanar design, via holes are avoided. Besides the advantages of coplanar circuits at millimeterwaves, their design requires sophisticated field simulation [10] and experimental work. The main critical effects are the ohmic losses and the dispersion of coplanar waves [11]. In addition, parasitic modes (surface waves and parallel plate modes) could be excited. These parasitics exhibit a strong dependency on the chosen coplanar configuration (backside metalliza-

tion, inner conductor width, gap width, width of ground metallization, dielectric constant, substrate height), but can be minimized in a proper circuit design.

3. Flip-Chip Sensor Modules

Different chips, ranging from diodes and discrete HEMTs [12] to MMICs [13, 14] have been used in the development of new flip-chip sensor modules at 24, 61 and 77 GHz. The results illustrate the excellent performance of flip-chip assembly.

Figure 2 shows a single stage K-band amplifier. The active flip-chip device is a discrete GaAs PHEMT chip (Siemens T409D). The transistor chip is very small (300 x 300 μm^2). The amplifier module (12 x 6 mm^2) is realized in coplanar waveguide with a inner conductor width of w = 130 µm and a gap width of g = 65 µm on a 635 µm thick alumina substrate. A tapered transition connects the amplifier input and output to coaxial ports. The bias network incorporates radial inductors. The simulated and measured gain curves S21(f) are plotted in Fig. 3. At the center frequency, a maximum gain of 9 dB is obtained. Experimental characterization of 10 identical flip-chip amplifier modules proved a very high circuit reproducibility.

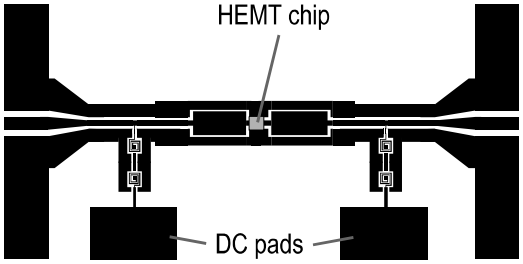

Fig. 2: K-band FC amplifier.

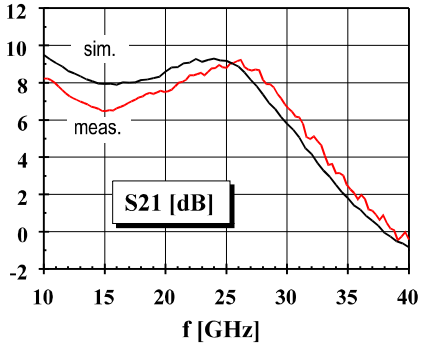

Fig. 3: Simulated and measured gain (S21).

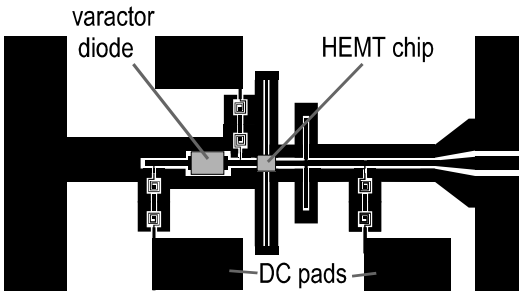

Fig. 4: K-band VCO module.

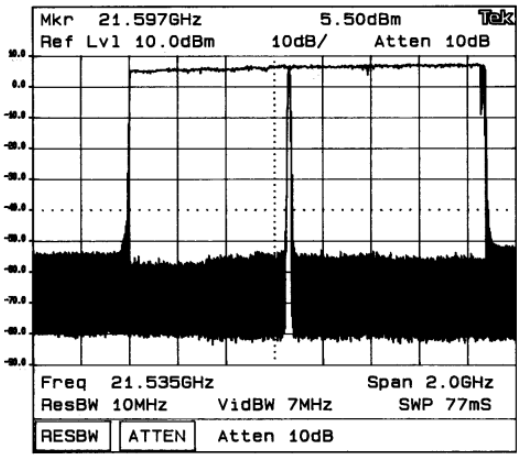

Fig. 5: Swept VCO output spectrum.

The K-band VCO, depicted in Fig. 4, is a reflection-type oscillator also utilizing the Siemens T409D chip. The size of the module is 12 x 6 mm^2. In the VCO design, we optimized for maximum reflection gain (S11) and moderate transmission (S21) in order to get a broad tuning bandwidth and small load pulling. Sweeping of the VCO is obtained by using a varactor tuning diode in a serial feedback configuration. The assembled FC VCO achieved a sweep bandwidth of 1.5 GHz and an output power of +5 dBm (Fig. 5).

By cascading the VCO, a buffer amplifier and a receiver, a compact K-band flip-chip FMCW sensor is realized (Fig. 6). A simple coplanar single diode detector receiver, depicted in Fig. 7, has been built. Through radial inductors, the sensor signal d(t) is taken from the detector DC pad, while interdigital capacitors (IDCs) provide the DC decoupling of the VCO, the buffer amplifier and the receiver.

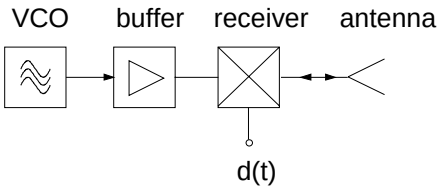

Fig. 6: Schematic of a FMCW sensor.

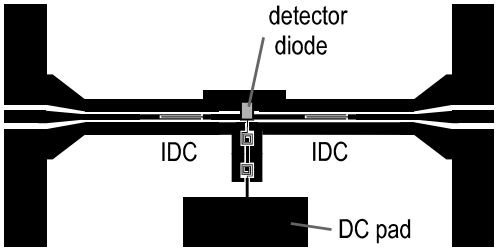

Fig. 7: Flip-chip detector.

Similar sensor modules for millimeterwave frequencies are in development. Figure 8 shows the photo of a 77 GHz flip-chip oscillator (chip size $2.4 \times 0.9 \times 0.1$ mm³). The GaAs MMIC VCO [15] incorporates the oscillator and two additional buffer stages. The chip is connected to the alumina substrate by a total of about 20 bumps with additional bumps for mechanical stabilization. The assembled FC VCO module includes the transition to a W-band coaxial connector. Typical VCO output power is +3 dBm (Fig. 9).

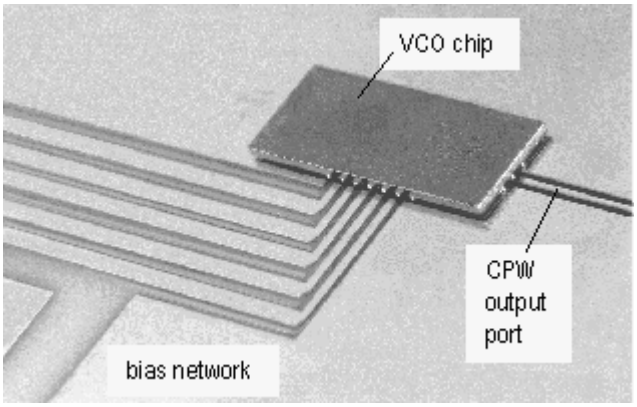

Fig. 8: 77 GHz flip-chip VCO.

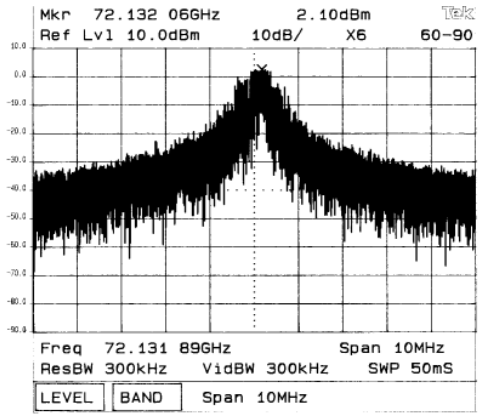

Fig. 9: VCO output spectrum

4. FMCW Sensor with SAW Reference

For commercial microwave applications, inexpensive sensors are needed. The FMCW principle is well established for radar distance measurements, because it offers high sensitivity and is thus suitable for high distance measurements and objects with low reflectivity. However, the performance of a FMCW sensor is limited by the sensor hardware: Typical effects, such as drifting, aging, nonlinearity and noise of the VCO will cause phase errors and thus limitations in measurement sensitivity and accuracy [16].

The basic idea behind a new patented FMCW sensor concept is that the measured distance is compared with an internal reference length [17]. To accomplish this, the IF section of the microwave sensor incorporates a highly precise reference path (Fig. 10) — a small 2.45 GHz SAW delay line [18]. Phase effects occur in the target path and in the reference path in an analogous way. These phase errors are detected and adaptively compensated *by software*. With the internal SAW reference, a self-calibration of the sensor hardware is achieved, which proved to work excellent for precise distance measurements at 24 GHz [19].

In the millimeterwave range, oscillator phase noise is a crucial sensitivity limitation in FMCW sensors [20]. For high-distance measurements, a good phase noise behavior is essential. Currently, monolithically integrated oscillators do not fulfill this requirement. The phase noise level of chip VCOs is typically at about -70 dBc/Hz @ 1 MHz (see Fig. 9). The corresponding limited coherence length of the radar signal is equivalent to a marked reduction in sensor sensitivity with respect to distant objects.

The stabilization of chip VCOs with a feedback loop is very critical and necessitates considerable additional hardware costs. As a cost-effective alternative, the phase noise related deterioration in system dynamics can be eliminated with the aid of the SAW reference. A possible sensor topology of a millimeterwave FMCW sensor with SAW reference is depicted in Fig. 11. A small part of the millimeterwave VCO signal is down-converted to the IF level and drives the 2.45 GHz reference path. Target and reference signal are fed into the DSP section, which removes all phase errors [17].

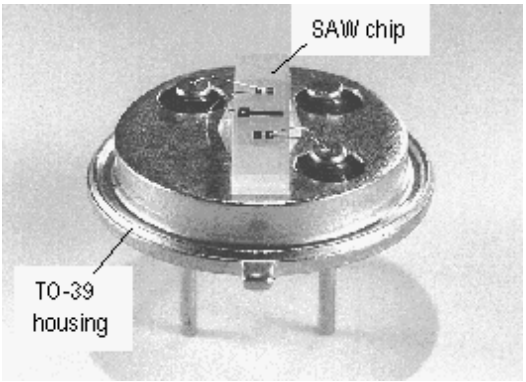

Fig. 10: High-Precision 2.45 GHz SAW reference.

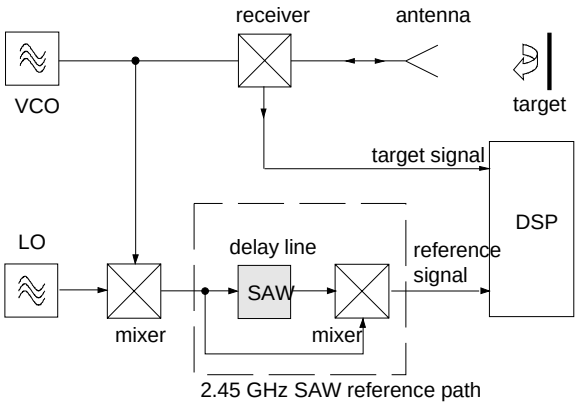

Fig. 11: FMCW sensor with SAW reference. Phase errors are compensated by software.

In experiments, performed with noisy millimeterwave MMIC VCOs, the reference technique proved to significantly enhance the dynamic range of the FMCW sensor, particularly for long-distance targets. Figures 12 and 13 illustrate the effect of phase errors on the FFT echo spectrum corresponding to a target at 100 meter distance. Due to these phase errors, the raw target echo is spread over a wide bandwidth. After phase error compensation, the same echo is compressed to a narrow peak.

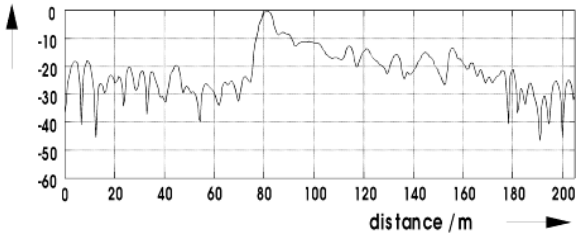

Fig. 12: Raw target signal (100 m distance).

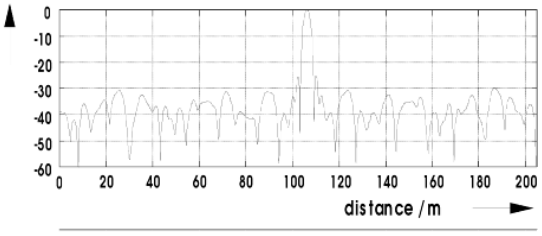

Fig. 13: Same target signal after phase error compensation.

The SAW reference obviates expensive demands on the quality of the oscillators, thus low-cost MMICs or planar Gunn elements can be used — an important prerequisite for opening up large-quantity commercial millimeterwave applications, such as 77 GHz automotive radar.

5. Conclusion and Outlook

New modules for microwave and millimeterwave sensor applications have been developed. It has been demonstrated that sensors can be significantly improved by utilizing the specific features of FC and SAW devices, while cost and size is reduced. The reported sensor modules prove the feasibility and attractiveness of flip-chips. To establish coplanar FC modules into high-volume production, however, further efforts are needed with respect to advanced production processes for thin-film ceramics with integrated bumps and airbridges.

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Development of a 35 GHz Radar Sensor

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Experimental results with two different 35-GHz Doppler radar units are reported in this contribution. The system consists of a planar GaAs transferred electron oscillator and an InGaAs-mixer diode. The oscillator is a MESFET-like structure with a negatively biased Schottky-gate. A stationary high-field domain is formed underneath the gate and acts as a transit-time-independent broadband negative differential resistance. To achieve mixing with high sensitivity at zero bias the energy barrier of the diode must be made low. The mixer diode used in this module consists of 0.18 µm InGaAs with 38 % In content and $1 \cdot 10^{17}$ cm^{-3} Si n-type doping. This yields an energy barrier of 0.3 eV. With the first design a sensitivity of 1 mV/µW has been obtained.

1. Introduction

Millimeter-wave radar sensor systems especially suited for automotive applications were intensively developed during the last few years [1], [2]. Combination of a low-cost technology together with advanced electrical characteristics and high reliability is a cornerstone requirement for an application in the automotive industry [3], [4]. Since the microwave front-end unit is the key unit determining the system's performance and cost, it is the most crucial part of the whole system. Two different 35 GHz low-cost RF front-end Doppler units suited for automotive applications have been constructed. The homodyne unit consists of both receiving and transmitting corporate-fed microstrip patch array antennas, a microstrip directional coupler, a monolithic GaAs FECTED oscillator, and an integrated single Schottky diode mixer. The autodyne configuration uses only one antenna and the FECTED as a self-oscillating mixer. Inexpensive microstrip technology has been used, which yields a good compromise between cost factor and technical performance.

2. System Configuration

The block diagram of the front-end unit is shown in Fig. 1. The output power of the oscillator is fed into the transmitting antenna. At the mixer diode the reflected signal from the receiving antenna is combined with the LO signal provided by the 10 dB directional coupler. The amplified IF signal is fed into a signal processor. This configuration is suitable for both Doppler CW (continuous waveforms) as well as FM (frequency-modulated) CW radar systems.

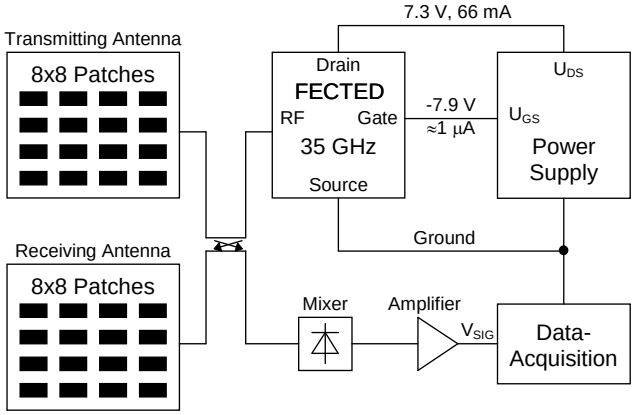

Fig. 1: Block diagram of the front-end unit using homodyne detection.

Further cost and size reductions of the module have been obtained with a simplified system configuration as shown in Fig. 2. In this design the FECTED (field effect controlled transferred electron device)-oscillator acts as a self-oscillating mixer [5] thereby sparing the mixer diode as well as the directional coupler and the second antenna. In this mode of operation the reflected signal received from the antenna changes the effective load impedance of the oscillator resulting in changes of both oscillator power and frequency which can be detected as bias current variations. A bandpass amplifier is used to separate the small bias current variations from the large DC current.

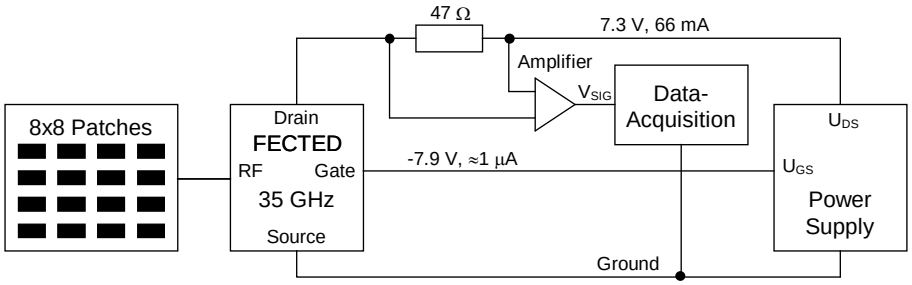

Fig. 2: Block diagram of the simplified front-end using autodyne detection.

3. Antennas

Two linearly-polarized corporate-fed microstrip patch array antennas have been designed for this system. The first one is a 4x4 array antenna with 16 degrees beamwidth and 17.5 dB (isotropic) power gain. The second one is a 8x8 array antenna with 8 degrees beamwidth and 21.5 dB (isotropic) power gain. The VSWR of both prototypes is below 2. A relatively inexpensive RT/duroid 5880 (a trademark of Rogers Corp.) substrate material of 0.254 mm thickness has been used for the fabrication of the antennas and the 10 dB directional coupler. The passive part has been made using standard photolithography and etching-technology, and has been covered by a gold film in order to minimize losses. A more detailed description of the antennas is given in [6]. Fig. 3 shows a photograph of the 8x8 array antenna module.

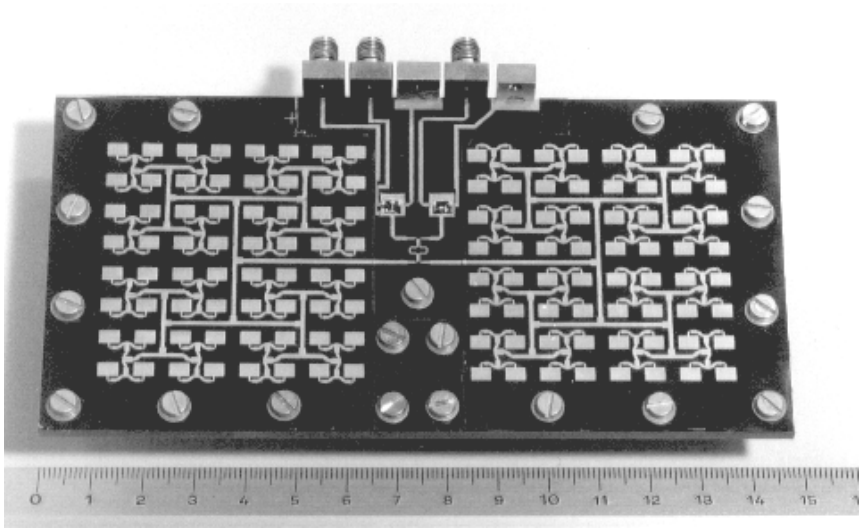

Fig. 3: Photograph of the front-end unit with 8x8 array antenna

4. Oscillator

In order to minimize costs a special planar Gunn diode has been used instead of a sophisticated transistor oscillator. This approach relaxes the demands on the resolution of the lithography. The device is called FECTED (Field Effect Controlled Transferred Electron Device) and is described elsewhere in this report. The device and the circuit have been fabricated on a 4x5 mm^2 GaAs chip with standard processing technologies. With the FECTED oscillator mounted in the sensor front-end an output power of about 4 mW at 34 GHz with an efficiency of 0.8 % has been measured. Further details of the FECTED have been published in [7].

5. Mixer Diode

5.1. Voltage sensitivity

The voltage sensitivity of a detector diode is defined as the output voltage generated by the diode into the load circuit divided by the RF-power absorbed in the diode. The goal of the optimization procedure is to make this sensitivity as large as possible [8].

The voltage sensitivity, β_v, of a circuit with load resistance R_L is given by

$$\beta_v = \frac{0.0005}{\left(I_s + I_0\right)\left(1 + R_j / R_L\right)\left[1 + \left(\omega C_j\right)^2 R_s R_j\right]} \left[\frac{\mathrm{mV}}{\mu\mathrm{W}}\right].$$

I_s..... reverse saturation current
I_0 ..... bias current
C_j..... junction capacitance of the diode
R_s..... series resistance
R_j ..... dynamic resistance (= q/nkT (I_s+I_0)).

It is necessary to minimize both the junction capacitance and the series resistance. The capacitance of the diode can be decreased if the size of the junction diameter is reduced. To obtain low series resistance the conductivity of the bulk material should be as high as possible, the current path through the material should be as short as possible and a good ohmic contact (low resistivity) is needed.

It is well known that large LO power is needed to minimize conversion loss of a GaAs Schottky mixer diode. This is a consequence of the high barrier height of about 0.7 eV of GaAs Schottky diodes. For a typical set of parameters for 10 µm x 10 µm Schottky barrier diodes (f = 35 GHz, n = 1.4, R_s = 10 Ω, C_j = 70 fF, R_L = 1 MΩ) the maximum of the sensitivity β_v can be calculated from the above equation. If the detector should be used without bias current, which simplifies circuitry, then $I_0 = 0$ and the saturation current I_s has to be in the range of 10^{-6} A. This corresponds to a barrier height of approximately 0.22 – 0.25 eV. However, the barrier height can be reduced if $In_xGa_{1-x}As$ is used. With increasing x the energy gap of the semiconductor is lowered from 1.42 eV (x = 0; i.e. GaAs) to 0.33 eV for x = 1 (InAs). With decreasing energy gap the barrier height of the Schottky contact is also reduced. With $In_{0.38}Ga_{0.62}As$ the desired barrier height can be adjusted.

5.2. Diode fabrication

The diodes have been fabricated using epitaxial layers of $In_{0.38}Ga_{0.62}As$ grown by metal organic vapor deposition (MOCVD) on semi-insulating GaAs substrates. In order to grow good quality $In_{0.38}Ga_{0.62}As$ layers on GaAs a graded buffer layer is needed to compensate the difference in lattice constants between InGaAs and GaAs. The Indium content is increased from 0 to 38% in steps of 5% in this layer. The first active layer grown is an n^+-layer doped $6 \cdot 10^{18}$ cm^{-3} with a thickness of 0.8 µm. On top of this layer a 0.19 µm thick n-layer with $2 \cdot 10^{16}$ cm^{-3} doping concentration has been grown. The ohmic contact is recessed to the n^+-layer and the connection to the Schottky-contact on the top is led over a SiO_2-bridge.

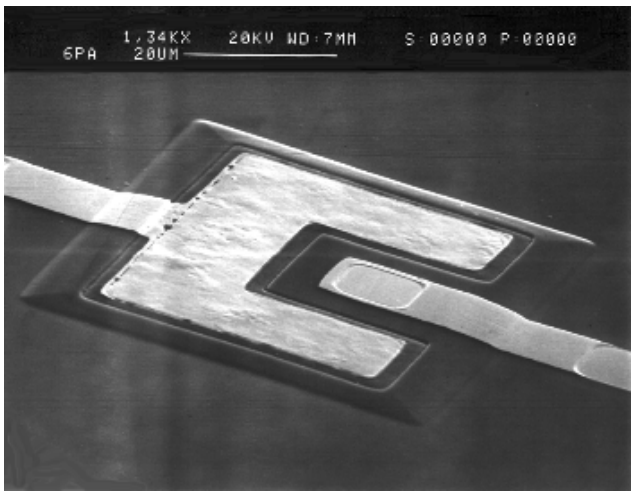

Fig. 4: SEM picture of the InGaAs Schottky diode

In Fig. 4, a SEM picture of the diode is shown. With the first design a sensitivity of 1 mV/µW has been obtained.

6. Results

Both front-end units have been tested with a target moving at a constant speed of 0.37 m/s from a distance of 2 meters towards the antenna. In the case of homodyne detection the amplified mixer signal V_{SIG} shown in Fig. 5 corresponds almost perfectly to the theoretic Doppler signal which is a harmonic function for constant target velocity. With a triangular corner reflector at a distance of 22 m, a signal amplitude of 100 mV after an amplification by a factor of 305 has been measured.

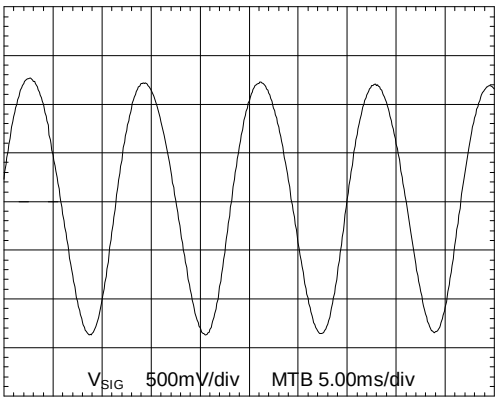

Fig. 5: Amplified (x 305) mixer signal from the homodyne configuration target velocity ... 0.37 m/s

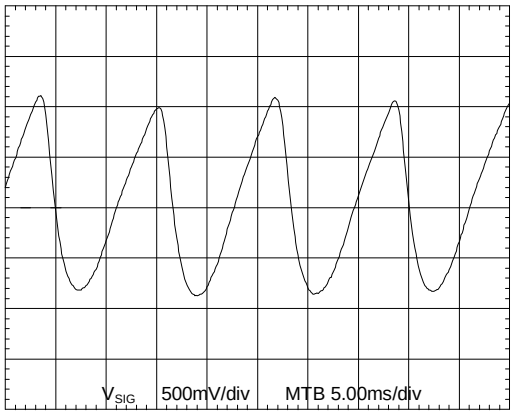

Fig. 6: Amplified (x 305) drain current modulation in the autodyne configuration, target velocity ... 0.37 m/s

For the autodyne configuration the detection range is much shorter because the reflected power received by the antenna must be sufficient to modulate the oscillator's output power. This modulation is highly nonlinear but periodical with half the wavelength as can be seen in Fig. 6 where the drain current modulation measured at a shunt and amplified is displayed.

7. Conclusion

Two different inexpensive configurations of the microwave part of a 35-GHz Doppler radar sensor system have been presented. The described approaches make it possible to achieve acceptable system performance with low-cost technology. The front-end with two antennas and the mixer diode has an operational range of at least 25 m. It is expected that this distance can be enhanced by optimizing the system components without increasing the transmitted power. A further cost reduction can be achieved by monolithically integrating the system on a single chip. The autodyne configuration has less sensitivity and higher noise level but it is the simplest and therefore cheapest approach.

Acknowledgments

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Konzepte der Gassensorik und ihre Umsetzung in neuen Produkten

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Weltweit besteht ein ständig steigender Bedarf, Schadstoffe in der Luft oder in Abgasen technischer Prozesse zu überwachen und darauf aufbauend elektronisch gesteuerte Regelsysteme zu schaffen. Zielgröße ist ein der Informationsverarbeitung zugängliches elektrisches Signal, das möglichst selektiv die Art und zugleich die Menge der zu detektierenden Schadstoffkomponente anzeigt. Für Konzentrationen im Spurenbereich erweisen sich potentialbildende Wechselwirkungen auf festkörperelektrochemischer Basis oder die hohe Sensitivität von Halbleiterschichten als geeignet, da sich deren Ladungsträgerkonzentration bei Einwirkung reduzierender Gaskomponenten ändern kann.

Zur ersten Gruppe gehören die als Rauchgas- oder Abgassonden eingesetzten Gassensoren vom Typ der Lambdasonde zur Steuerung einer schadstoffarmen Verbrennung, z. B. in Heizungsanlagen, auch in Kraftwerken oder im Verbrennungsmotor, indem durch Rückkopplung des Sensorsignals die Einstellung eines optimalen Treibstoff-Luftgemisches erreicht wird.

Die zweite Gruppe der Halbleitersensoren hat wohl erstmals im Taguchi- oder Figaro-Sensor eine Massenanwendung erfahren. Hier wird eine mit elektrischen Zuleitungen versehene dünne geeignet dotierte SnO_2-Schicht auf einem bis zu ca. 400 °C geheizten Keramikträger als Sensorelement genutzt. Obwohl an der Luft ein großer Sauerstoffüberschuß gegeben ist, rufen reduzierend wirkende Gasbestandteile, z. B. H_2, CO, CH_4 oder andere Kohlenwasserstoffe, auch Alkohole, durch Elektronenübertragung eine Leitfähigkeitserhöhung hervor, die als Sensorsignal ausgewertet werden kann. Bei geeigneter Dotierung ist auch NO_x detektierbar, worauf sich technische Lösungen z.B. für die Luftklappensteuerung in Fahrgast-Innenräumen stützen. Von Nachteil ist die beschränkte Langzeitstabilität und Feuchte-Querempfindlichkeit des Sensorsignals bei derartigen SnO_2 -Schichten.

Um diese Nachteile zu vermeiden, wurden bei Siemens Dünn- und Dickschichtverfahren zur definierten Abscheidung von Oxidsystemen, z.B. von $SrTiO_3$ oder Ga_2O_3 entwickelt, die auf Grund ihrer höheren thermischen Stabilität erst bei höherer Temperatur, z. B. zwischen 650 und 950 °C infolge partieller Sauerstoffabspaltung bzw. durch Sauerstoffausbau aufgrund einwirkender reduzierender Gasbestandteile halbleitend werden. Derartige Oxidschichten sind thermodynamisch stabil und das Sensorsignal, bedingt durch die hohe Betriebstemperatur, weitaus weniger feuchteempfindlich. Kurze Ansprechzeiten von < 10 ms werden beim $SrTiO_3$ auf Grund hoher Diffusionskoeffizienten von Sauerstoffleerstellen im Perowskitgitter erreichbar, sodaß eine zylinderselektive Steuerung von Verbrennungsmotoren und die daraus resultierende beträchtliche Absenkung des Schadstoffausstoßes in greifbare Nähe gerückt sind. Ga_2O_3-Sensoren erweisen sich auf Grund ihrer stabilen Kennlinie und hohen H_2-Empfindlichkeit zur

Steuerung von Kleinfeuerungsanlagen als geeignet. Ihr Einsatz läßt außerdem Anwendungen in CH_4-Gaswarngeräten oder als Alkoholtester erwarten.

Zukünftige Entwicklungen betreffen selektive Sensoren für einzelne Gase, z. B. bei CH_4- oder CO-Detektion aus Sicherheitsgründen die Eliminierung einer Ethanol-Querempfindlichkeit. Weiterhin steht die Schaffung von Sensorarrays auf der Tagesordnung. Integriert mit mikroelektronischen Schaltkreisen lassen sich durch Variation von Gestalt und Anordnung der Elektrodenstrukturen im Bereich ultradünner Schichten verschiedene Ladungstransportmechanismen mit ihren unterschiedlichen Sensitivitäten für bestimmte Gase dahingehend nutzen, daß feinste Geruchsunterschiede aufgelöst werden können (elektronische Nase). Derartige Produkte sind gegenwärtig von einer reproduzierbaren Massenfertigung noch relativ weit entfernt. Wichtig sind vor allem die Standzeiten. Schließlich ist die Nutzung subtiler Halbleitereffekte im offenen System einer vielfach aggressiven, durch Staub und andere undefinierte Einflüsse geprägten Umgebung keineswegs trivial.

Miniaturized Sensor Systems

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The acceptance of sensor concepts by industrial equipment producers requires an optimization of the sensor design for the specific application. We developed miniaturized thermal flow sensor designs for very different applications like a novel gas meter, for the investigation of the air intake of combustion engines and an extremely sensitive version for monitoring the flow of excess liquor cerebrospinalis during hydrocephalus treatment. In the field of biosensors, good sensor specifications are not sufficient for broad acceptance by the analytical equipment industry. The needs of a complete analytical process have to be considered by the sensor developer. For such purposes we established a cheap technology for the production of miniaturized fluid handling modules based on dry photoresists [1]. The flexibility of this technology allows the realization of complex structures needed for analyte preprocessing.

1. Introduction

Because of their inherent advantages as low analyte consumption, quick response, and cheapness, miniaturized sensors are very attractive for biomedical and many other applications. Sensors intended for example for the survey of industrial processes or for the monitoring of biomedical systems must fit perfectly into the specific system for doing their job as good as possible. These biosensor systems have to fulfill many different tasks as establishing the right environment for the sensor functioning, handling of the analytes, linking the sensor signal to the information processing equipment. Only a complete miniaturized sensor system will be acceptable for applications outside the research labs.

Beside such system aspects, the sensor element itself must match to the specific requirements of the intended use as good as possible. As a consequence, in some cases completely different manufacturing procedures have to be used even for sensors based on the very same technological concept. The presented examples of miniaturized thermal flow sensors are good examples to demonstrate this influence.

2. Experimental

2.1. Dry film resist technology for miniaturized analyte handling modules

Dry films resists are available as etching resists and for solder masks (i.e. VACREL®). The patterning of each resist layer is a three-step process: lamination, exposure, developing (Fig. 1). The achievable aspect ratio is approx. 0.5, e.g. grooves with a width of 100 µm can be formed if the layer thickness does not exceed 50 µm. The walls are not perpendicular to the surface but undercut at an angle of 15°. If structures higher than 100 µm are desired, the process can be repeated using the same mask. We showed that

three-dimensional structures can be realized without special bonding techniques. The complete process is illustrated in Fig. 1.

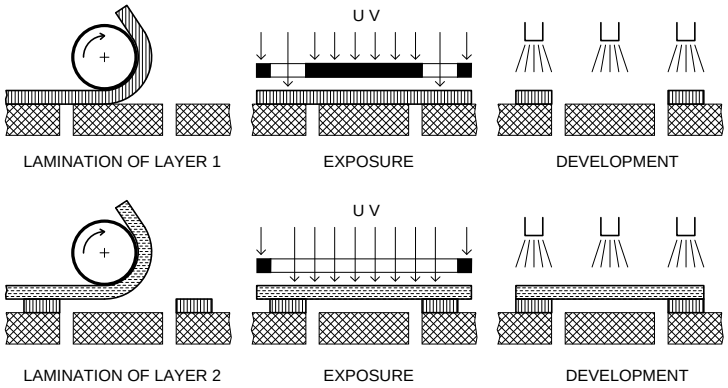

Fig. 1 : Dry resist based manufacturing of a flow channel

The resist material must be cured after patterning of the last layer. This process consists of a temperature step and a final exposure to UV light.

Many biosensors require perfect mixing of the analyte and some added agents to produce accurate results. Miniaturized flow channels obstruct the mixing of fluids because of their inherent laminar flow profiles. We designed a miniaturized Moebius-type mixer [2] which on the one hand enhances the useful flow range and on the other hand reduces the required dead volume.

2.2. Miniaturized flow sensors

2.2.1. Micro Flow Sensor Treatment of Hydrocephalus

This sensor (Fig. 2) is a part of a miniaturized all-silicon device for the aid of patients suffering from hydrocephalus [3]. This device should measure the intracranial pressure and automatically opens a shunt for excessive liquor cerebrospinalis if required. The flow sensor serves for continuous monitoring and should detect reverse flow too. The flow sensor was placed on a thin film membrane borne by a micro-machined Si structure for highest flow sensitivity. A special mask alignment equipment that is capable for mask adjustment related to structures at the backside of the wafer is needed for the sensor manufacturing. This equipment is now available at MISZ laboratories. The desired flow detection limit for this application, namely 50µL/h was experimentally verified. It is planned to implement similar sensors in controlled drug delivery devices.

2.2.2. A sensor for the study of the air Intake of combustion engines

The air intake rate of a combustion engine is one of the key parameters needed for optimizing the combustion process. To investigate the dynamic behavior of a suction system, a useful flow sensor must offer quick response, high sensitivity, recognition of flow direction, and a wide dynamic range. Miniaturized thermal anemometers, based on thin film Ge thermistors, show a good compromise of the mentioned characteristics and changing of the direction of flow could be achieved using two temperature sensors placed symmetrically to a thin film platinum resistor that represents the hot wire. Thanks to miniaturization a response to changes of flow within one ms was obtained.

Prototypes of such flow sensors were successfully tested under simulated suction system conditions.

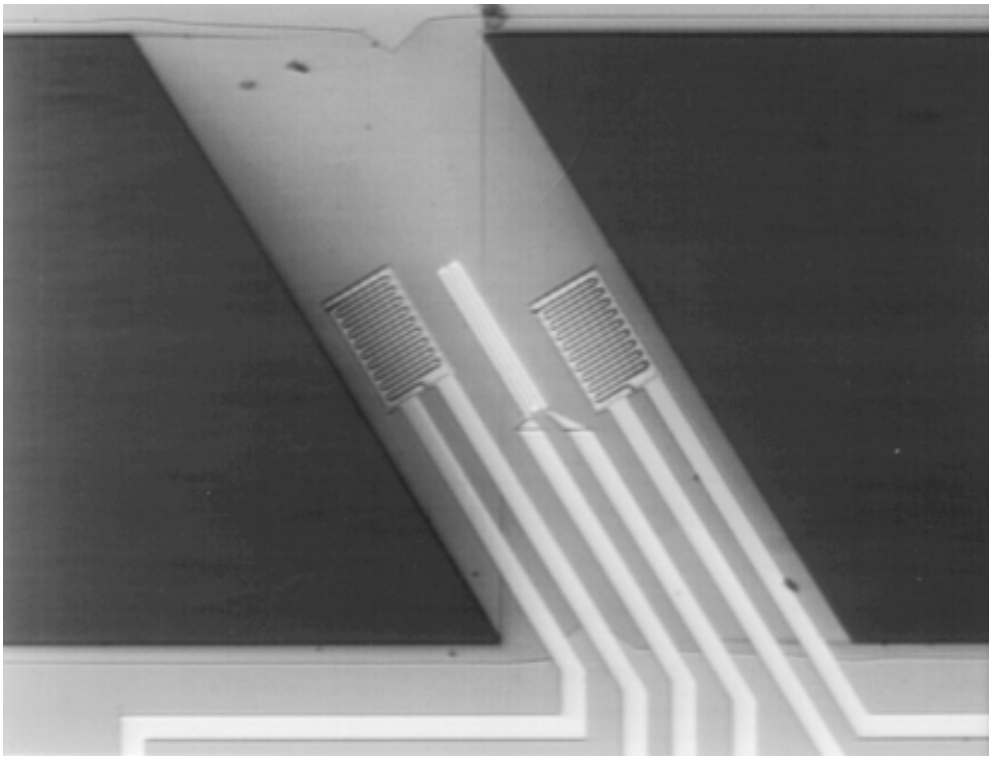

Fig. 2: A thermal flow sensor placed on a SiN_x micro bridge. Flow channel width measures 1 mm. A thin film platinum resistor of 750 Ω is located in the mid of two thin film Ge thermistors with a resistance of 56 kΩ.

2.2.3. Miniaturized thermal flow sensors for a novel gas meter

The gas meter concept uses the fluid oscillator principle, which is based on oscillations of the flow velocity field inside an especially shaped flow channel. The frequency of the oscillations increases in the range 0.1 to 100 Hz with increasing flow. The oscillation frequency can be measured best with a pair of thin film thermistors.

There are some remarkable requirements for this applications: high reliability for long term, service free operation (typical six to ten years), low power consumption for long term battery powered operation, high sensitivity at low gas velocities, miniaturized shape for undisturbed flow and simple incorporation, appropriate resistance values and good pairing tolerance for simple data acquisition circuits. On the other hand, there are no restrictions concerning the absolute accuracy and long term drift of the sensor elements. After an extensive evaluation of the technological alternatives the producer of the gas meter decided to use miniaturized self heated Ge thermistors placed on micromachined membranes on silicon chips as the key element for flow detection. The design issues were minimum Si area and high thermal resistance for high flow sensitivity at low power consumption.

3. Conclusion

Miniaturized biosensors normally require an integrated analyte processing module to be an acceptable sensor system for utilization. Dry film photoresists offer the possibility to develop integrable fluid handling components in a very convenient way if modest miniaturization is sufficient. To optimize the design of a miniaturized sensor for integrability into a specific system is another successful way to make use of it. The presented miniaturized thermal flow sensors are examples for that concept.

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Modellbildung für einen optischen Kohlenstoffsensor

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In der vorliegenden Arbeit wird ein Modell zur theoretischen Herleitung des Auswertealgorithmus für einen neuartigen Kohlenstoffsensor beschrieben. Das modellierte Meßverfahren dient zur Bestimmung der Konzentration von Kohlepartikeln in einem pulverförmigen Medium. Es beruht auf der Auswertung von Reflexionsmessungen, die in Kombination mit einer speziellen mechanischen Probenpräparation durchgeführt werden.

1. Einleitung

Für die kontinuierliche Überwachung des Kohlenstoffgehalts von Flugasche in einem Kohlekraftwerk wurde am Institut für Allgemeine Elektrotechnik und Elektronik in Kooperation mit der EVN (Energieversorgung Niederösterreich AG) ein optischer Kohlenstoffsensor entwickelt. Flugasche ist ein feinkörniges graues Pulver, in dem kleine Kohlepartikel eingelagert sind. Die Messung des Kohlenstoffgehalts erfolgt nach dem Reflexionsprinzip in Kombination mit einer speziellen mechanischen Probenbehandlung [1-4]. Bei dem bereits in der Praxis eingesetzten Prototyp ist der Meßablauf automatisiert. Die Flugascheprobe wird geebnet, gepreßt und durch Andrücken einer drehbaren Glasplatte einem oberflächlichen Reibeprozeß unterworfen, bei dem sich das Reflexionsvermögen der Probe ändert. Aus Reflexionsmessungen vor und nach dem Reibevorgang läßt sich durch Anwendung eines speziellen Auswertealgorithmus der gesuchte Kohlenstoffgehalt berechnen. Dieses zur Auswertung der Meßsignale (Fotodiodenströme) notwendige Berechnungsverfahren wurde mit Hilfe des nachfolgend beschriebenen Modells ermittelt (Dissertation A. Schneider, in Arbeit). Aus Platzgründen wird das Modell nur in seinen Grundzügen beschrieben.

2. Modellbildung

Im Modell wird das Volumen der geebneten Flugascheprobe aus sehr kleinen Würfeln zusammengesetzt gedacht. Das Grundmaterial der Flugasche (Mischung verschiedener Oxide) wird durch transparente, lichtstreuende Würfel repräsentiert, während die Kohlepartikel durch schwarze, lichtabsorbierende Würfel modelliert werden (Fig. 1). Die relative Anzahl der schwarzen Würfel in einer Flugascheprobe wird mit a bezeichnet, wobei

$$0 \le a \le 1 . \qquad (1)$$

Unter Zugrundelegung dieser Modellvorstellung läßt sich das Reflexionsvermögen des unendlich ausgedehnten Halbraumes durch Aufsummieren der Reflexionsbeiträge aller Würfel mit einer Potenzreihe berechnen. Man erhält das Ergebnis:

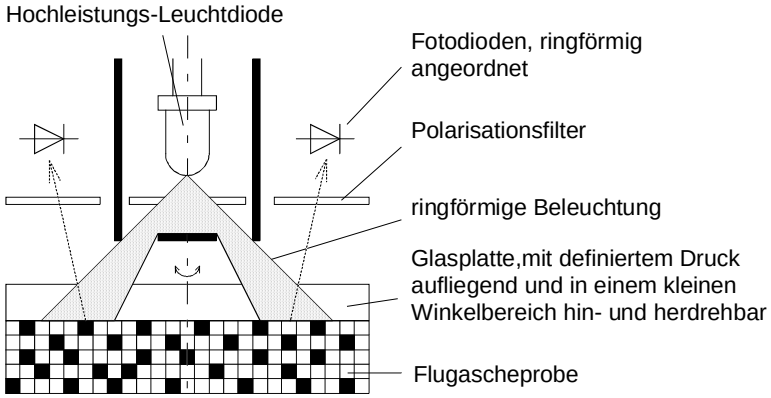

Fig. 1: Prinzipschema der optischen Meßanordnung und der im Modell aus sehr kleinen Würfeln zusammengesetzten Flugasche.

$$R = \frac{1-\sqrt{1-((1-a)/(1+a))^2}}{(1-a)/(1+a)} \tag{2}$$

Dieses Resultat stimmt mit dem Ergebnis der bekannten Kubelka-Munk-Theorie [5] über die diffuse Reflexion an pulverförmigen Substanzen überein. Im Idealfall (synthetische Flugasche) kann die Größe a mit dem Kohlenstoffgehalt C in der Flugasche identisch gesetzt und aus der obigen Gleichung (2) als Funktion des gemessenen Reflexionsvermögens R direkt berechnet werden. Das Würfelmodell hat den Vorteil, daß es erweiterungsfähig ist. Es kann auch zur theoretischen Beschreibung der Reflexionsänderung durch einen Reibevorgang (siehe Einleitung) verwendet werden. Unter der Annahme, daß schwarze Würfel doppelter Größe in Würfel normaler Größe zerfallen, ergibt die Theorie folgenden Ausdruck für die Abnahme des Reflexionsvermögens:

$$\Delta R = \frac{1-\sqrt{1-((1-a)/(1+a/2))^2}}{(1-a)/(1+a/2)} - \frac{1-\sqrt{1-((1-a)/(1+a))^2}}{(1-a)/(1+a)} \tag{3}$$

Leider zeigt sich in der Praxis, daß in der Flugasche von Kohlekraftwerken nicht nur die Kohlepartikel absorbierend wirken, sondern auch dunkle Eisenoxidpartikel vorhanden sind. Der Eisenoxidgehalt F ist somit eine zusätzlich zu bestimmende Größe. Um beide Unbekannte (C und F) berechnen zu können, wurde ein weiteres Modell entwickelt. Es stützt sich auf die Tatsache, daß die Eisenoxidpartikel wegen ihrer Härte bei einem Reibeprozeß nicht zerkleinert werden (im Gegensatz zu den Kohlepartikel). Dieses Modell liefert einen Auswertealgorithmus, bei dem nicht nur die Differenz ΔR des Reflexionsvermögens vor und nach einem Reibeprozeß, sondern auch der Absolutwert des Reflexionsvermögens R am Ende des Reibevorganges benützt wird:

$$\Delta R = \frac{1-\sqrt{1-x_F^2((1-C')/(1+C'/2))^2}}{x_F(1-C')/(1+C'/2)} - \frac{1-\sqrt{1-x_F^2((1-C')/(1+C'))^2}}{x_F(1-C')/(1+C')} \tag{4}$$

$$R = \frac{1-\sqrt{1-x_F^2((1-C')/(1+C'))^2}}{x_F(1-C')/(1+C')} \quad \text{mit} \quad x_F = \frac{1-F}{1+F}, \quad C' = \frac{C}{1-F(C+F)}, \tag{5}$$

wobei gilt: $0 \le C+F \le 1$.

3. Ergebnisse

Das Modell beschreibt für eine mittlere Partikelgröße die wirkliche Situation beim Messen von realer Flugasche ausreichend gut, wenn folgende Bedingungen eingehalten werden:

a.) definierter Anpreßdruck der Glasplatte an die Flugascheprobe

b.) konstanter Drehwinkel der Glasplatte

c.) gleichbleibende Anzahl von Drehungen pro Messung

Mit den vom Sensor erhaltenen Meßwerten ΔR und R (abgeleitet aus dem Fotodiodenstrom der optischen Meßanordnung nach Fig. 1) werden aus den oben angeführten Gleichungen (4) und (5) die unbekannten Größen C und F berechnet. Die aus dem Modell resultierenden Zusammenhänge sind im Fig. 2 dargestellt.

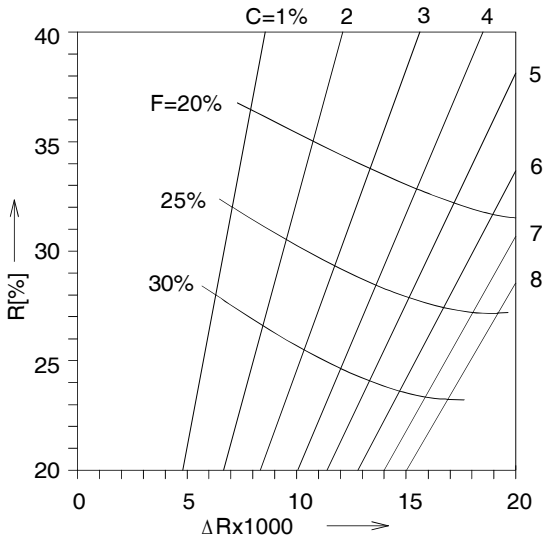

Fig. 2: Graphische Darstellung des aus dem erweiterten Würfelmodell resultierenden Ergebnisses. Aus den beiden Meßwerten R und ΔR resultiert der Kohlenstoffgehalt C und der Eisenoxidgehalt F.

Der mit dem Modell ermittelte Auswertealgorithmus wurde bei einem in der Praxis (Kraftwerk Dürnrohr) eingesetzten Prototyp eines Kohlenstoffsensors angewendet. In Fig. 3 ist ein Vergleich der Sensorresultate mit Kohlenstoffkonzentrationen, die durch chemische Analyse der Flugasche im Labor erzielt wurden, dargestellt.

Danksagung

Wir danken der Firma EVN (Energieversorgung Niederösterreich AG), insbesondere Herrn Dr. A. Aumüller, für die Förderung dieses Projekts (EVN 018/45113619).

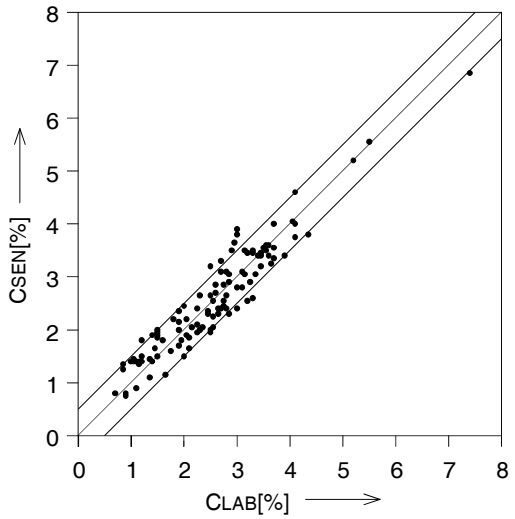

Fig. 3: Vergleich von Sensormeßwerten und Laboranalysewerten, wobei die Sensormeßwerte mit Hilfe des aus dem Würfelmodell entwickelten Auswertealgorithmus berechnet wurden. Anzahl der Proben: 110.

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Three-Dimensional Photolithography Simulation

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An overall three-dimensional photolithography simulator is presented, which has been developed for workstation based application. The simulator consists of three modules according to the fundamental processes of photolithography, namely imaging, exposure/bleaching and development. General illumination forms are taken into account, and the nonlinear bleaching reaction of the photoresist is considered. Electromagnetic light-scattering due to a nonplanar topography is treated by solving repeatedly the Maxwell equations within the inhomogeneous photoresist. The development process is simulated with a cellular based surface advancement algorithm.

1. Introduction

Among all technologies photolithography holds the leading position in pattern transfer in today's semiconductor industry. The reduction of the lithographic feature sizes towards or even beyond the used wavelength and the increasing nonplanarity of the devices place considerable demands onto the lithography process. The large cost and time necessary for experiments make simulation an important and especially cost-effective tool for further improvements. However, a rigorous description of the fundamental physical effects governing sub-micrometer-photolithography places considerable demands onto the modeling, whereby a three-dimensional simulation becomes necessary.

We present an overall three-dimensional photolithography simulator consisting of three modules. Each module accounts for one of the fundamental processes of photolithography: imaging, exposure/bleaching, and development.

2. Imaging Simulation

The imaging module describes the illumination of the photo-mask. The light propagation through the optical system and the light transmission through the photo-mask has to be simulated. The output of the imaging module is the aerial image which is the light intensity incident on top of the wafer.

Our aerial image module is based on a vector-valued extension of the scalar theory of Fourier optics [1]. The photo-mask is assumed to be laterally periodic and infinitesimal thin with ideal transitions of the transmission characteristic. The piece-wise constant transmission function is real-valued (zero or one) for binary masks, in case of phase-shift masks it is complex-valued with module less than one. For the simulation of general illumination forms like annular and quadrupole the aperture is discretized into mutually independent coherent point sources. The resulting image on top of the wafer due to one coherent point source can be expressed by a superposition of discrete diffraction

orders. Due to the assumed periodicity of the photo-mask this superposition corresponds to a Fourier expansion, whereby the diffraction orders are homogeneous plane waves with amplitudes given by the vector-valued diffraction theory [1].

3. Exposure/Bleaching Simulation

The exposure/bleaching module simulates the chemical reaction of the photosensitive resist. The light propagation within the optically nonlinear resist as well as electromagnetic (EM) scattering effects due to a nonplanar topography have to be modeled. The result of the exposure/bleaching module is the latent bulk image.

According to Dill's 'ABC'-model [2] the exposure state of the photoresist is described by the concentration of the photoactive compound (PAC). The PAC concentration constitutes the bulk image. As it is transferred into the resist by light absorption the EM field inside the photoresist has to be determined. Because the bleaching rate is negligible as compared to the frequency of the EM field, we apply a quasi-static approximation, i.e., we assume a steady-state field distribution within a time step and solve repeatedly a time-harmonic version of the Maxwell equations with a linear but spatially inhomogeneous permittivity.

Our solution of the Maxwell equations [3], [4] corresponds to the three-dimensional extension of the differential method. This method was originally developed for the simulation of diffraction gratings [5] and was later adapted for two-dimensional photolithography simulation [1]. The strategy behind the differential method is briefly described as follows: First, the dependency of the EM field on the lateral coordinates is expressed by Fourier series. Insertion of these expansions into the Maxwell equations transforms the partial differential equations into a system of ordinary differential equations. Above and below the simulation domain analytical expressions can be found for the incident, reflected, and transmitted light. Matching these expansions with the Fourier series valid inside the photoresist yields decoupled boundary conditions for the top and the bottom of the simulation domain. Hence, we have to solve a two-point boundary value problem [6]. This is accomplished with a newly developed algorithm [4], [5], that is based on the memory saving "shooting method" [6]. Once the ordinary differential equation system is solved, the obtained field coefficients are transformed back to the spatial domain to calculate the absorbed EM field intensity as necessary for the Dill model.

4. Development Simulation

The development of the photoresist is modeled as a surface-controlled etching reaction [2]. We use Kim's 'R'-model [7] to relate the bulk image to a spatially inhomogeneous etch or development rate. This development rate is stored on a tensorproductgrid, because the differential method requires a laterally uniform spaced grid to apply the numerically highly efficient Fast Fourier Transform (FFT). For the simulation of the time-evolution of the development front the recently proposed cellular-based topography simulator of [8] has been extended to read the development rate from the tensorproductgrid [4]. The basic idea behind this surface advancement algorithm is to apply a structuring element along the exposed surface which removes successively resist cells of the underlying cellular geometry representation. Within the scope of lithography

simulation the shape of the structuring element depends on the precalculated development rate multiplied by the chosen time step.

5. Simulation Results

To demonstrate the capability of our approach we simulated contact hole printing over a planar and a stepped topography. In Fig. 1 we show the aerial image obtained by the vector-valued approach used for our imaging module. Conventional I-line illumination with a numerical aperture of NA = 0.5 and a partial coherence factor of S = 0.7 was used. Nine coherent point sources were needed to account for the partial coherence.

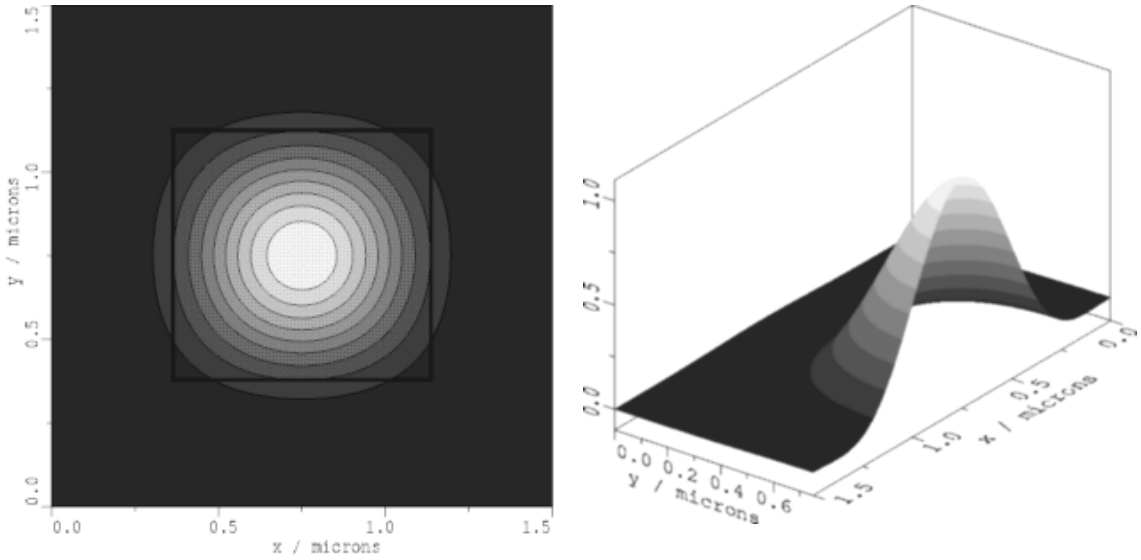

Fig. 1: Aerial image of a 0.75 mm x 0.75 mm wide contact hole.

In Fig. 2 contour plots of the PAC are shown in the upper two figures and the developed photoresist profiles in the lower two figures. The exposure-dose was 120 mJ/cm^2 and the development time was 50 sec. The simulation parameters were for the Dill-model no = 1.65, A = 0.55 μm^{-1}, B = 0.045 μm^{-1}, C = 0.013 cm^2/mJ and for the Kim-model R1 = 0.25 μm/sec, R2 = 0.0005 μm/sec, R3 = 7.4 (cf. Table IV in [7]).

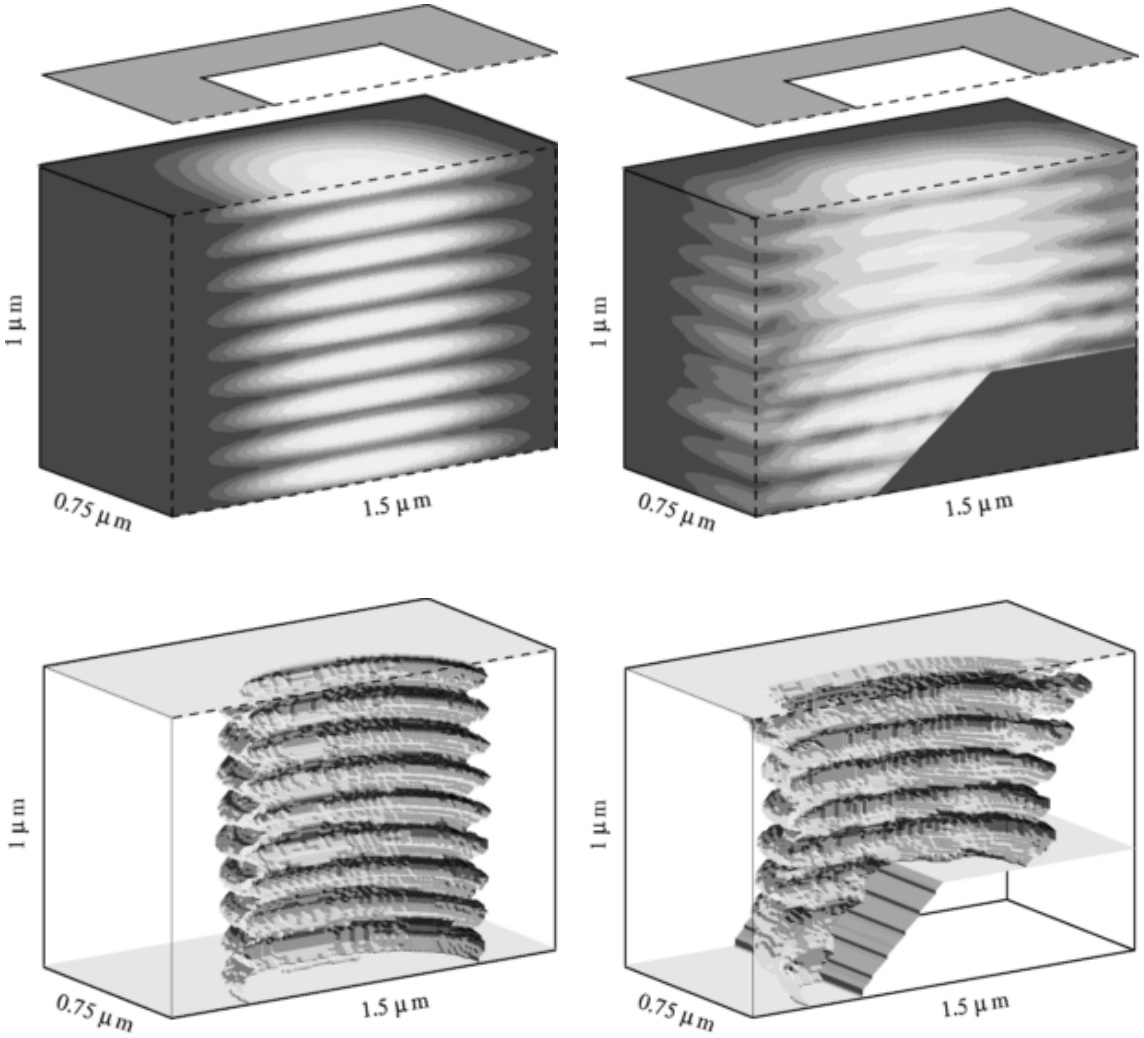

Fig. 2: Bulk image and developed resist profile over a planar and a stepped substrate.

The oval contours are caused from standing waves within the photoresist, which result from substrate reflections. Due to the lateral variation in optical thickness the regular shaped bulk image and resist profile of the planar topography is distorted in case of the stepped topography. Furthermore, the opening for the stepped substrate is wider than for the planar substrate. Hence, the effective diameter of the contact hole depends on the nonplanarity of the wafer topography.

Acknowledgment

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Single Quantum Dots as Scanning Tunneling Microscope Tips

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We report the use of single quantum dot structures as tips on a scanning tunneling microscope (STM). A single quantum dot structure with a diameter of less than 200 nm and a height of 2 µm was fabricated by reactive ion etching. This dot was placed on a 40 µm high mesa and mounted on the tip of a STM. The topography of large structures such as quantum wires or gold test substrates is clearly resolved with such a tip. To check the transport properties of the tip, quantum dot arrays were fabricated on resonant tunneling double barrier structures using the same process parameters. Conventional tunneling spectroscopy clearly resolved the 0D states in our samples. Using a metal substrate as second electrode such STM tips can be used to perform high resolution energy spectroscopy on single dots and free standing wire structures.

1. Introduction

Recent advances in micro fabrication technology such as lithography, etching and epitaxial regrowth enabled a reduction of the dimensions of semiconductor devices in a way that tunneling processes in low dimensional systems (1D, 0D) can be studied. First experiments on 1D-1D and 1D-0D tunneling processes were carried out in ultra small, pillar shaped double barrier resonant tunneling diodes (DBRTDs) by Reed et al [1]. On such samples, the resonance structures in the tunneling current were assigned to resonant tunneling processes between 1D states in the emitter region and 0D states inside the quantum well defined by the two barriers [2]. In similar experiments, based on asymmetric DBRTDs, charging effects were also observed [3], [4]. Using a shallow etching process in combination with a side-gate, it was possible to adjust the 0D confinement by varying the gate voltage. The observed resonance structures in the tunneling current were assigned to Coulomb blockade effects [5], [6] as well as to ionized donor atoms [7]. Focused ion beam implantation can also be used to define structures containing quantum dots [8] . Using triple barrier RTDs as starting structure, tunneling processes in coupled quantum dot structures have also been investigated experimentally [9] and theoretically [10] – [12]. The fine structure of the current-voltage characteristic [13] in the above experiments can be explained by strong coupling between 1D subbands in the contact region and 0D states inside the quantum dots.

As main problem for all above sample structures, the formation of contacts to the quantum dots is difficult and requires planarization techniques and recess etching. Using the metal tip of a scanning tunneling microscope [14] as a mobile contact to single wires or quantum dots, however, this problem is overcome and even local tunneling spectroscopy on single wires can be performed [15], [16].

2. Experimental

In this paper we report an inverse approach to the above experiments and replace the metal tip of the STM by a single quantum dot on a high mesa. To test the resolution of such a tip, the topography of a gold substrate and also of a large quantum wire array was scanned. To check the electrical quality of the tip, conventional tunneling spectroscopy on double barrier resonant tunneling diodes was employed. The 0D states are clearly resolved in our samples demonstrating that such STM tips are an easy way to establish contacts to single dots and free standing wire structures.

To fabricate the tips, electron beam lithography on a double layer of PMMA / PMMA-MA copolymer resist, metallization and lift off were used to define a single gold dot on a GaAs substrate. Optical lithography and RIE (Ar, $SiCl_4$ and SF_6) was then used to define the mesa supporting the dot. Residual photoresist is also removed by this step. The mesa is then etched further by RIE (Ar, $SiCl_4$) processes using the small gold dot as etch mask to produce a thin pillar with 200 nm diameter and 2 µm height (Fig. 1).

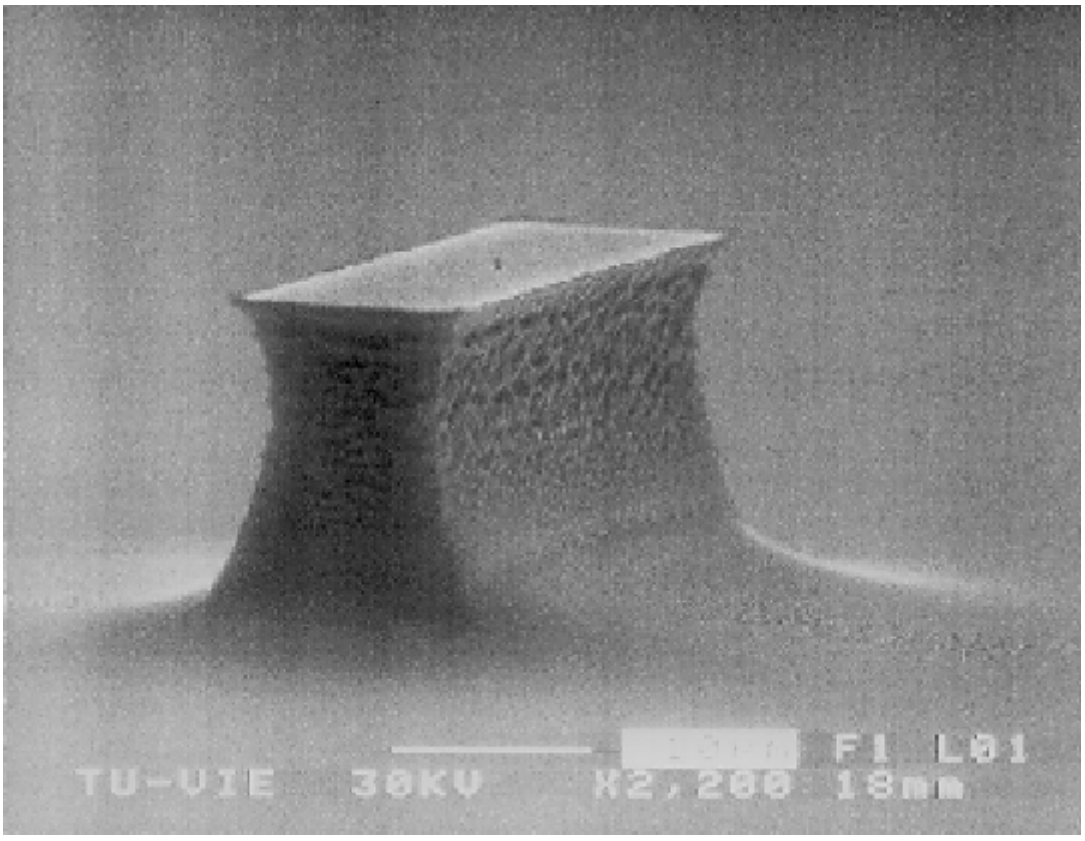

Fig. 1: The supporting mesa was defined by optical lithography and RIE. On top of it a single gold dot can be seen defined by electron beam lithography, metallization and lift off. The dot mask is etched into the mesa by further RIE processing to form a single quantum dot. This structure is then used to replace the metal tip of a STM.

This structure was mounted on the STM and used as a superfine STM tip to scan an array of wet chemically etched quantum wires. The result of this experiment is shown in Fig. 2.

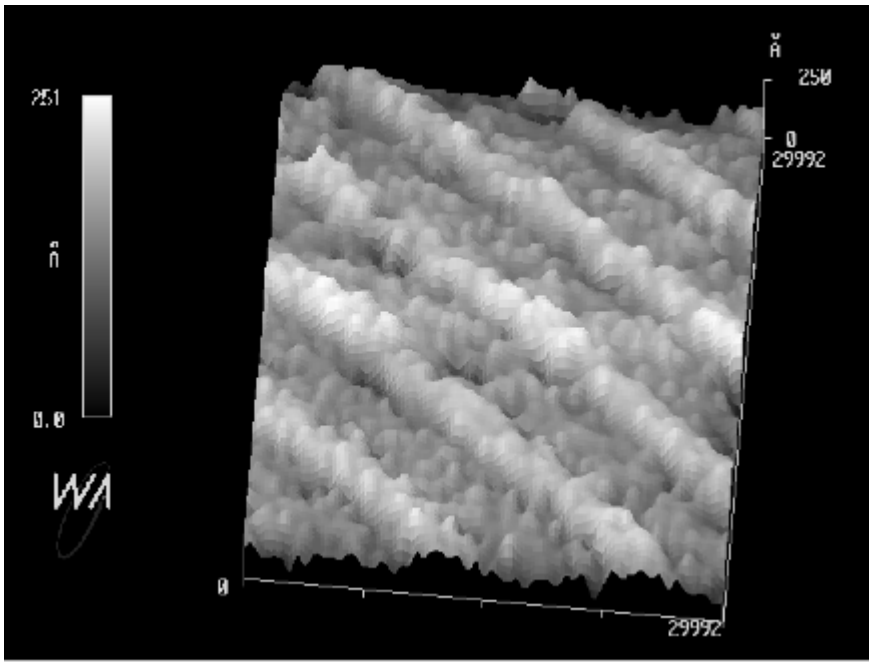

Fig. 2: Wet chemically etched quantum wires scanned with a STM. An etched quantum dot on a high supporting mesa was used as the tip of the STM.

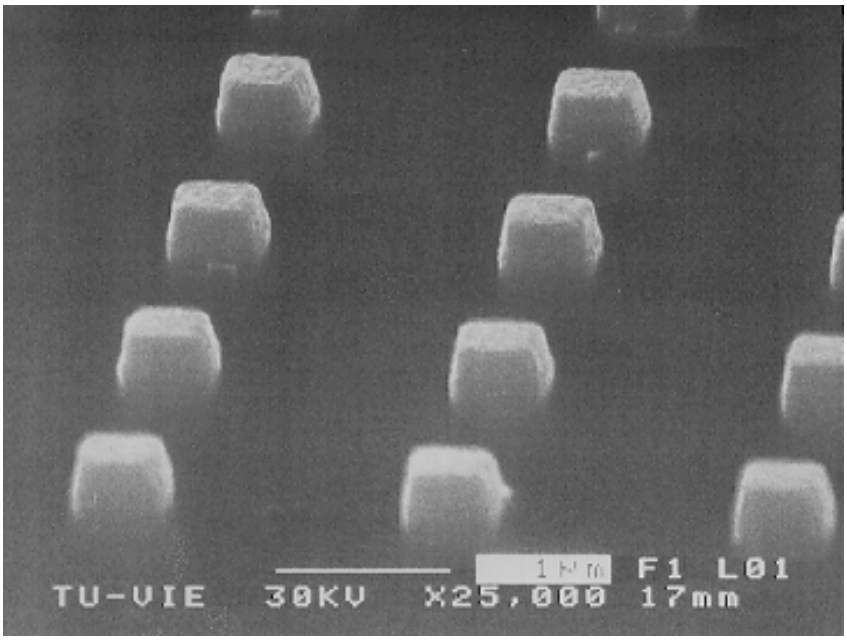

Fig. 3: Top contacts of quantum dots after planarization and recess etching by RIE. The metallized top contacts were used as an etch mask and form together with a second metallization a common top electrode for standard tunneling spectroscopy measurements.

To demonstrate that 0D levels are formed in the etched quantum dot we applied the same fabrication technology to standard RTD structures. An array of quantum dots planarized with resist, recess etched and metallized to form a top contact is shown in

Fig. 3. A bias voltage was applied to the quantum dots and the current through the dots was measured in liquid Helium by standard tunneling spectroscopy. Fig. 4 shows the obtained results. Resonant tunneling between 0D states and energy levels in the double barrier can clearly be seen in the current / voltage characteristic around -0.15 V, -0.35 V and -0.7 V. The resonances around -0.15 V are much better resolved in the derivative of the I/V characteristic.

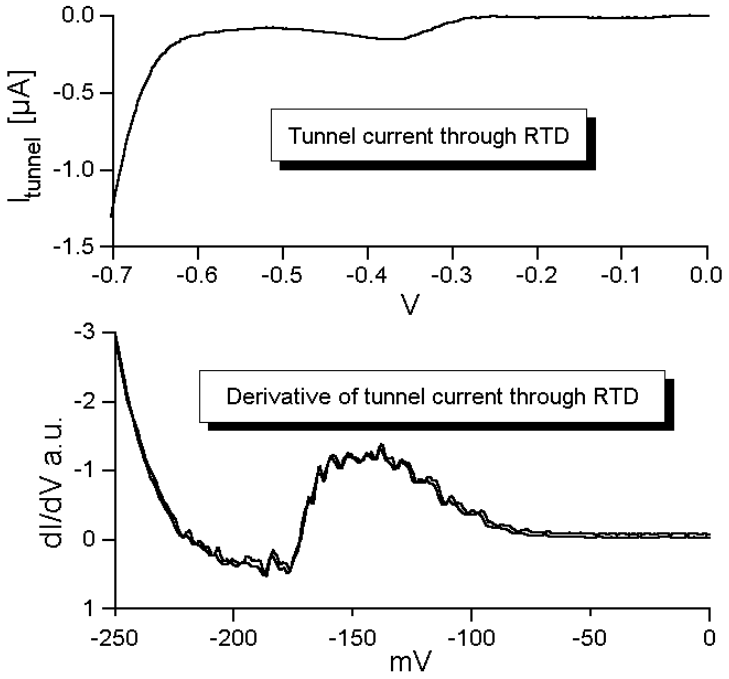

Fig. 4: Top image: IV characteristic of a RTD quantum dot array. Resonant tunneling through energy levels in the double barrier can be clearly resolved at bias voltages of 0.35 V and 0.7 V. Bottom image: Resonant tunneling through 0D energy levels can clearly be resolved in the derivative of the I/V characteristic around a bias voltage of 0.15 V. Similar resonances are also found at 0.35 V and -0.7 V.

3. Conclusion

In summary, we have used a single quantum dot structure as the tip of a STM. It was found that quantum dot structures with a diameter of less than 200 nm and a height of 2 µm form a very fine tip also suitable of scanning topographic profiles of other nanostructures such as quantum wires. Tunneling processes between low dimensional states on reference samples were also investigated in this configuration. For this purpose, quantum dot arrays were fabricated on resonant tunneling double barrier structures using the same process parameters than for the STM tips. In the RTD dot arrays, 0D states are clearly resolved by conventional tunneling spectroscopy. Thus, our method provides a simple way to for tunneling spectroscopy on single quantum dots, provided the STM is operated at low temperatures. As our STM can be operated in liquid helium [16], further experiments are in progress.

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Nanostructuring of Semiconductors

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Periodic nanostructure patterns based on molecular epitaxy grown CdZnSe/ZnSe single quantum wells and Si/SiGe heterostructures have been defined by holographic lithography or electron beam lithography and fabricated by reactive ion etching. The CdZnSe/ZnSe structures exhibit photoluminescence emission down to the smallest investigated lateral width of 80 nm. For the narrow wires a spectral red shift of the photoluminescence emission up to 8 meV is observed which is explained by a partial elastic strain relaxation of the biaxial compressively strained CdZnSe quantum well layer after the patterning process. Detailed calculations of the inhomogeneous strain status and the piezoelectric effect of the partially relaxed wire structures and the resulting band gap changes were performed and compared with the experiment. The large area Si/SiGe periodic wire structures were investigated by high resolution x-ray diffraction.

1. Introduction

The realization of semiconductor nanostructures is relevant for future electronic devices, optical emitters and the investigation of basic physical properties. In II-VI semiconductors the realization of wide band-gap blue-green diode lasers [1], [2] initiated the interest in light emitters from nanostructures. In such a nanostructure it is expected that low threshold laser structures can be realized.

In Si/SiGe heterostructures the investigation of nanostructures is driven by the miniaturization of today's integrated circuits and the potential of the Si/SiGe material system to increase the performance of such devices. Both material systems mentioned consist of strained layers, and the investigation of strain relaxation effects due to the formation of laterally patterned nanostructures is needed for practical implementations.

The purpose of our Si/SiGe study was to find a reliable etching procedure for the fabrication of Si/SiGe sub-micron structures. There are previous reports in the literature that in particular the sidewall steepness of SiGe embedded in Si is much worse than that of silicon. The etched Si/SiGe structures were then structurally characterized by x-ray diffraction.

2. Sample preparation

The II-VI and Si/SiGe heterostructures were both grown by molecular beam epitaxy in Linz. The CdZnSe/ZnSe single quantum well (QW) heterostructures consist of a 1.1 µm thick, fully relaxed ZnSe buffer on top of the GaAs (001) substrate (grown by W. Faschinger). A 10 nm CdZnSe layer forms the QW and a 100 nm ZnSe layer acts as a cap. High density periodic patterns were defined either by holographic or electron beam lithography. In the case of e-beam lithography, well defined arrays of 40 x 40 μm^2 with

wires and dots of different lateral size were written into a 150 nm thick polymethylmethacrylate (PMMA) resist layer. The lateral distance between individual pattern arrays is 150 µm. After deposition of a 40 nm thick titanium layer, a lift-of process was used to produce the metallic structures on top of the sample with area filling factors between 0.5 and 0.15. These patterns were transferred into the QW structure by reactive ion etching (RIE).

During the RIE process the sample is exposed to a reactive gas plasma which contains active species that etch the material by chemical reactions. A CH_4/H_2 gas mixture (1:6 volume ratio) with a high frequency power of 90 W (corresponding to a DC bias of 450 V) at a pressure of 3.3 Pa (25 mTorr) is used for the II-VI compounds. The surface morphology and the lateral sizes of the etched structures were investigated by scanning electron microscopy (SEM). A typical SEM micrograph for small wires is shown in Fig. 1.

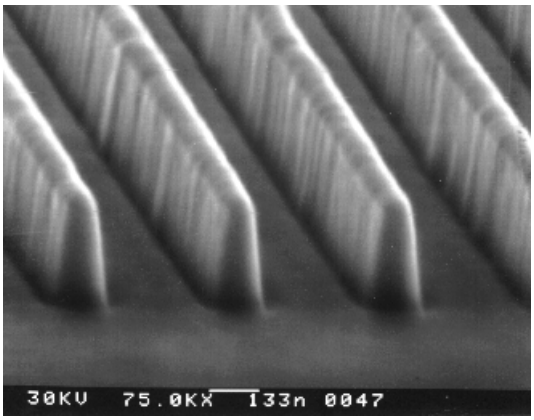

Fig. 1: Scanning electron microscopy image of CdZnSe/ZnSe wire structures defined by electron beam lithography and fabricated by reactive ion etching with a CH_4/H_2 gas mixture.

The damage which is introduced during RIE was also investigated by Auger electron spectroscopy (AES). For this purpose ZnSe, ZnTe, CdSe and CdTe epilayers were grown by molecular beam epitaxy and treated by reactive ion etching in CH_4/H_2 admixtures of different compositions and analyzed by AES with depth profiling. It was found that the CH_4:H_2 ratio has great influence on the chemical composition of the sample surface layer. For CH_4:H_2 ratios of about 1:7, the lowest deviation from stoichiometry and the lowest incorporation of oxygen and carbon was found [11].

Si substrates and Si/SiGe multiquantum well layers (Ge content: about 20%, 10 periods, Si layer width: 20.5 nm, and SiGe layer width of 1.8 nm) were laterally patterned using holographic lithography (λ = 458 nm) by reactive ion etching. The period of the wires is about 400 nm, the wire width about 200 nm. The etching depth is about 200 nm. The etching gases consisted of a mixture of SF_6 and CH_4 (90%/10% mixing ratio) using the following parameters. The rf-power was 30 Watt, the pressure 40 mTorr, the flowrate of SF_6 was 50 sccm, and for CH_4 it was about 2.5 sccm. (The corresponding parameters for the Si/SiGe MQW samples were the same). The remaining photoresist was taken off by an oxygen plasma. The surface morphology of the samples was investigated by scanning electron microscopy. The structural parameters were studied by different x-ray diffraction techniques, as described below.

3. Optical investigations

Low temperature (T = 1.9 K) PL measurements were performed with an x-y mapping set-up with a spatial resolution of 30 μm (determined by the laser spot diameter). The $Cd_{0.2}Zn_{0.8}Se$ QW embedded in ZnSe barriers (with a low temperature band gap E_g = 2.820 eV) was resonantly excited with an Ar^+ ion laser at an energy of 2.708 eV (457.9 nm) with about 100 W/cm^2. The PL spectra of the $Cd_{0.2}Zn_{0.8}Se$/ZnSe wires and dots with lateral dimensions between 80 and 1000 nm are shown in Fig. 2. The width of the PL emission line from the 2D reference mesa on the same sample is about 8 meV, a value which is essentially caused by alloy fluctuations in the ternary CdZnSe layer. Thus the splitting between free and bound excitons cannot be resolved.

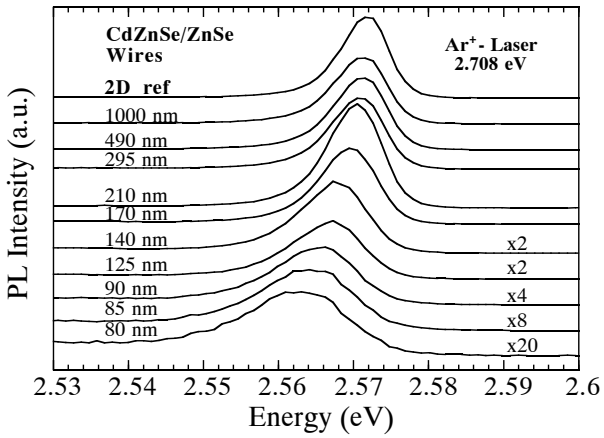

Fig. 2: Photoluminescence spectra of CdZnSe/ZnSe wire structures for lateral width of 80 to 1000 nm at 1.9 K. In addition the 2D quantum well reference spectrum on the same sample piece is shown.

Figure 3 shows the peak position of the PL line for wire and dot structures with lateral width between 80 and 1000 nm. A significant red shift occurs for wire sizes below 300 nm and dot sizes below 500 nm which is about 8 to 10 meV for the smallest wires and dots, respectively. The observed red shift will be discussed and compared with calculated band gap changes due to strain relaxation below.

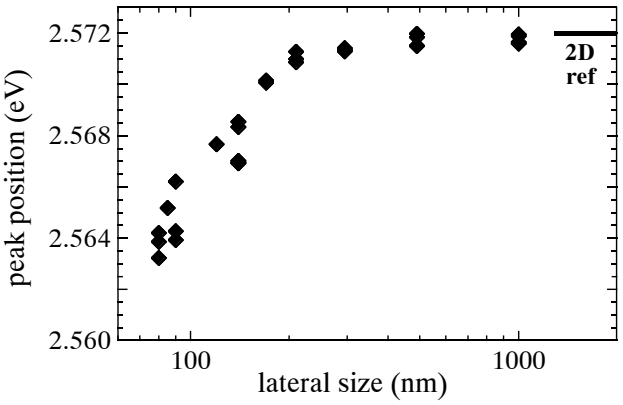

Fig. 3: Photoluminescence peak position of wire structures between 80 and 1000 nm for a resonant excitation energy of 2.708 eV (457.9 nm).

4. Strain Relaxation and Band-Gap Changes

Due to the formation of free perpendicular surfaces during the lateral patterning, the strained layers are able to relax partly. This is shown in Fig. 4 schematically for a thin wire structure. In order to calculate the detailed strain distribution of the wire structures, we follow an analytical method outlined by Faux and Haigh [3] but adopted it for our [110] oriented wires. This method solves the Airy stress equation by a Fourier series ansatz. The advantage of this method is that it is analytic, the disadvantage (as compared e.g. to finite element methods) is that only simple geometries can be treated with a restricted range of boundary conditions.

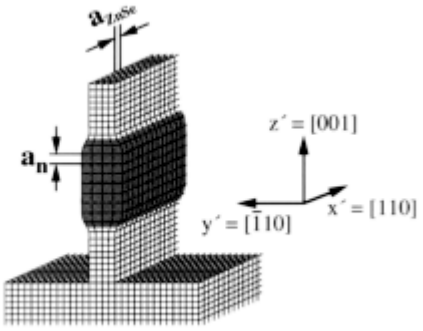

Fig. 4: Schematic strain relaxation of a laterally thin, partly relaxed CdZnSe/ZnSe wire.

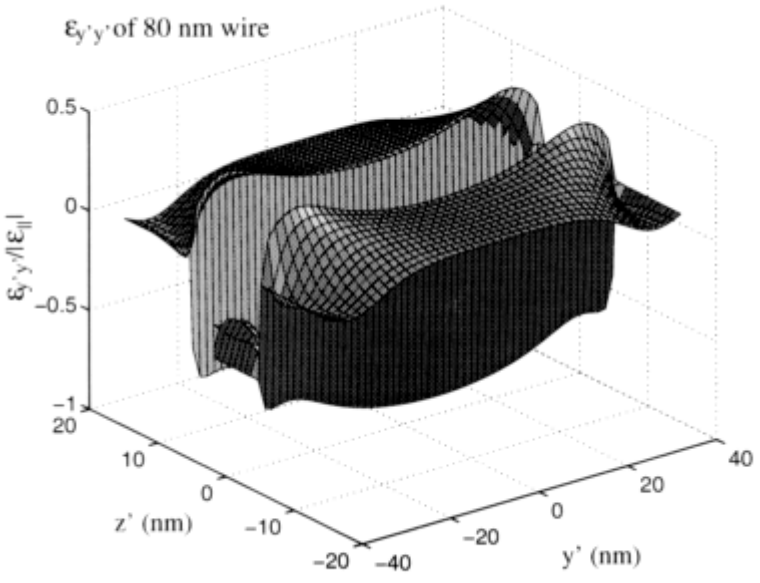

Fig. 5: Strain component $\varepsilon_{y'y'}$ for the wire cross section y´z with the y´ direction in the quantum well plane but perpendicular to the wire and the z direction along the growth direction.

Figure 5 shows the calculated strain distribution $\varepsilon_{y'y'}$, for a 80 nm wide wire of our CdZnSe/ZnSe structure, where the coordinate y´ in the epitaxial plane is perpendicular to the wires. The magnified displacements (by a factor 20) characterized by $\varepsilon_{y'y'}$ and ε_{zz} are shown in Fig. 6 for the wire cross section (the y´z-plane). It is clearly visible that the distortions are largest at the free surfaces. The shear component $\varepsilon_{y'z}$, which characterizes the deviations from a rectangular grid, is largest at the interface between the CdZnSe well and ZnSe barrier layers close to the free surface.

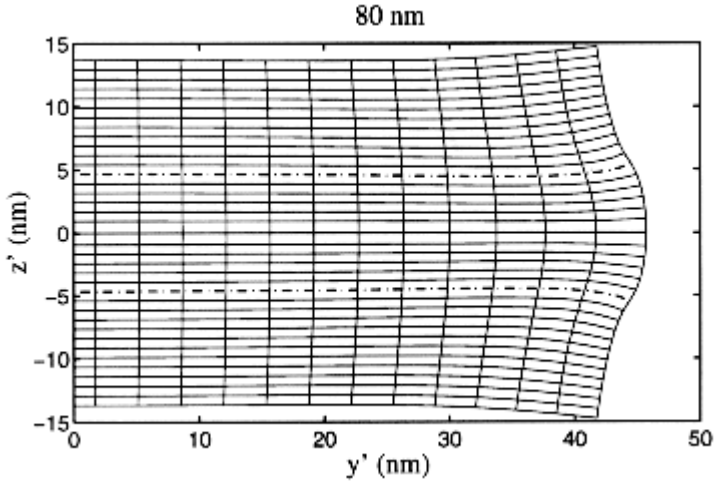

Fig. 6: The displacement, magnified by a factor 20, according to the strain components $\varepsilon_{y'y'}$ and ε_{zz} for the wire cross section (y´z-plane).

In <110> wires the non-uniform lattice deformation induces a piezoelectric polarization field [4], [5], [8]. The piezoelectric effect is directly connected with the shear components (shear strains ε_{jk}, $j \neq k$) as these describe the distortions of the cubic crystallographic cell. The potential distribution due to the piezoelectric were calculated accordingly for our wire structure with a width of 80 nm. The potential difference between upper and lower interface along the z-direction is about 12 meV. This bending of the quantum well potential and the associated electric field leads to a Stark effect which shifts the energy levels in the center of the well only by about 0.5 meV. Compared to the observed red shifts and the changes of the band gap due to deformation potential coupling, the effects due to piezoelectric coupling will be only important at still smaller wire structures.

Due to the lateral wire confinement by RIE patterning in 80 nm structures, the eigenstate energies inside the CdZnSe well change by less than 0.5 meV for electrons and 0.4 meV for heavy holes. These additional lateral confinement energies (blue shifts) are much smaller than the experimentally observed red shifts and will not give a relevant contribution.

The band gap changes due to the elastic strain relaxation in the wire structures are much more important. For the conduction band, the strain induced energetic shifts are easily calculated as no splitting of degeneracies due to a tetragonal or orthorhombic distortion of the lattice occurs. Only the hydrostatic component of the lattice affects the position of the CB edge [6]. The situation for the VB is more complicated as even in the 2D QW system (tetragonal distortion without the presence of shear strain components), the four-

fold degeneracy (Γ_8, including spin) of the cubic T_d crystal symmetry is removed. The energy levels of the valence band for cubic systems can be described by the k·p perturbation approach [7]. The effects of strain, confinement or other distortions can be included in the Hamiltonian of the system by using perturbation theory [10]. The deformation potential parameters a_v, b and d as introduced by Bir and Pikus [9] describe the energetic changes due to hydrostatic, tetragonal and shear deformations of the lattice, respectively. The solutions for the 6x6 Hamiltonian are obtained by numerical diagonalization for a given set of strain components which itself depends on the y´-z position inside the wire cross section. The resulting variation of the band gap over the cross section of the 80 nm wire is shown in Fig. 7.

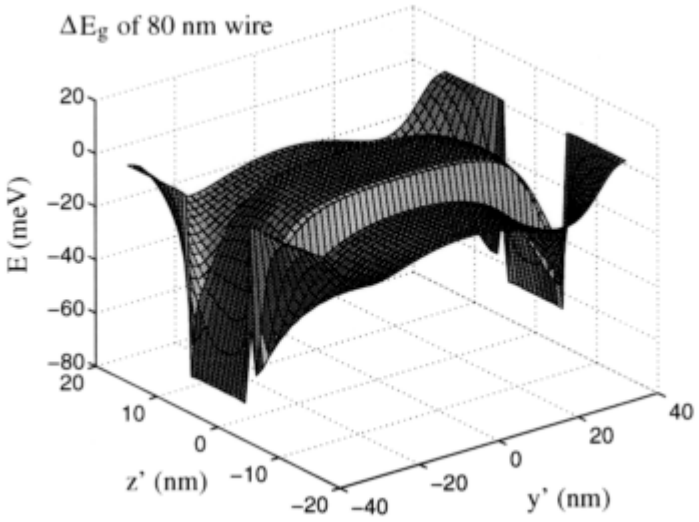

Fig. 7: Variation of the band-gap on the wire cross section (y´z-plane) for lateral wire width of 80 nm.

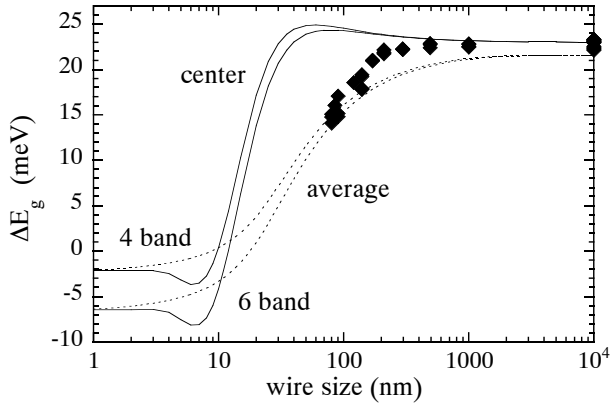

Fig. 8: Comparison of the calculated energy gap shift, averaged over the wire cross section, with the photoluminescence peak position for lateral wire width between 80 and 1000 nm. For comparison the gap in the center of the wire is shown for 6-band and 4-band calculation.

The calculated band gap changes of about 8 meV for the 80 nm wire structure are comparable with the experimentally observed PL line width of the 2D reference area on the sample. It is thus not expected to resolve any splitting of lines, but just a broadening and shift. It is also unknown how the PL emission efficiency is correlated with the spatial position in the wire structure. This efficiency depends on the RIE induced damage near the free surfaces as well as on the carrier diffusion after generation by incident laser beam. In Fig. 8 the calculated averaged energetic band gap shift is compared with the experimentally observed spectral red shift of the PL emission and gives a quantitative agreement.

5. X-Ray Investigations

The structural parameters of the Si/SiGe multiquantum well layers were studied by employing x-ray diffraction techniques, like double and triple crystal diffractometry. In Fig. 9a and b (311) ω-scans are shown for two Si-wire samples, with identical period (glancing angle exit diffraction). For the sample shown in Fig. 9a, the etching time was 13 min, for the sample shown in Fig. 9b it was 17 min. Since the number of wire satellites in Fig. 9b is somewhat larger, the structural quality of the periodic wire structures has certainly been improved.

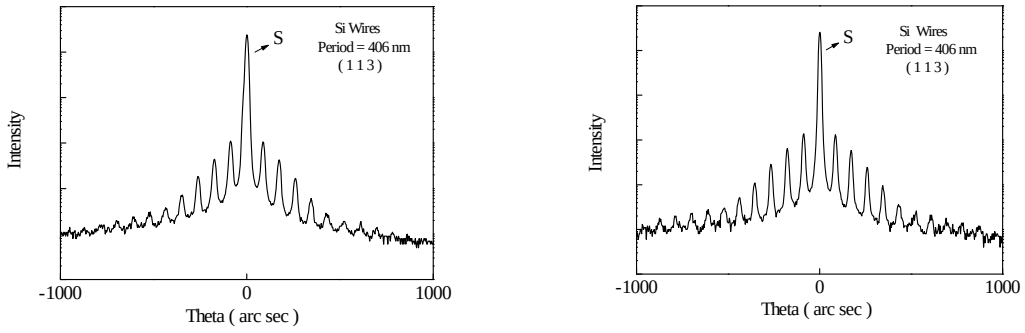

Fig. 9: ω-scans (113 reflection) of Si wire structures (area filling factor 0.5, period 406 nm) for RIE exposure times of 13 and 17 min, respectively)

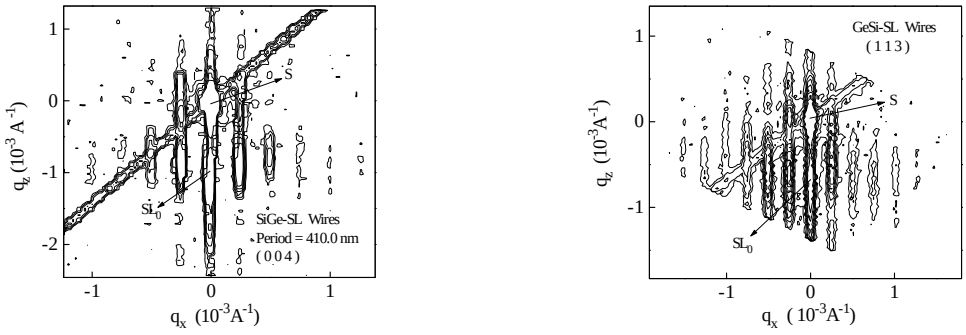

Fig. 10: (004) and (113) reciprocal space maps of a Si/SiGe wire structure (period 410 nm).

Reciprocal spacemaps around the (004) and the (311) reflection were recorded for the etched Si/SiGe multilayer samples (sample code: SiGe 46, which was grown by Stefan Zerlauth in the SiGeC MBE apparatus in Linz) as shown in Figs. 10a and 10b. Not only the MQW structure was etched through, but also part of the Si-buffer layer has been etched, as evidenced from the satellites accompanying the substrate peak marked by S. The MWQ structure gives rise to a superlattice peak (SL_O) which is accompanied along the q_X-direction by wire satellites. The period from the wire satellites is about 410 nm. A strain analysis based on these data will be performed.

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Unconventional Nanostructuring Approaches

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This paper describes two rather unconventional approaches towards nanostructuring: The first approach uses a novel type of material — two-dimensional crystalline protein layers, the so-called S-layers — in lieu of a photoresist. These layers not only promise an exceedingly high intrinsic lateral resolution due to their structure and nanometer-range thickness, they may also play a key role as geometrically and physicochemically precisely defined immobilization matrices in the binding of functional molecules (e.g. enzymes or antibodies) in bioanalytical sensors, as supporting layers for functional lipid membranes (for example, in ion sensitive field effect transistors), or as intermediate layers for binding ligands in the design of resists for nanostructure lithography.

The second approach presented here is unconventional not due to the technology used but with regard to the devices that are to be created: An array of silicon columns, which are prepared by electron beam lithography and anisotropic plasma etching, is to serve in a space experiment as a "brush" for cosmic particles, which are to be trapped between the columns and subsequently analyzed with an atomic force microscope. This contribution describes the preparation of large uniform arrays of photoresist columns with a high aspect ratio, which constitutes the first step for the preparation of the silicon or quartz structures proper.

1. Patterning of Monolayers of Crystalline S-layer Proteins on a Silicon Surface by Deep Ultraviolet Radiation

1.1. Introduction

Surface layers referred to as *S-layers* are two-dimensional crystalline protein layers with the unique capability to recrystallize with perfect uniformity at liquid surfaces or on solid supports such as silicon wafers, even if the surface exhibits a demanding three-dimensional topography. They are ideal patterning structures for supramolecular engineering due to their high molecular order, high binding capacity, and perfect uniformity. In particular, the recrystallization of S-layer subunits on substrates suitable for micro- and nanofabrication, such as silicon, gallium arsenide, or gold, allows the application of S-layers as patterning structures for molecular manufacturing.

S-layer proteins form the outermost cell envelope component in many archaeo- and eubacterial strains [1]. The center-to-center spacing of the morphological units is in the range of 3 to 30 nm, the thickness of the S-layer is in the 10 nm range. Basic research

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on the structure, chemistry, and morphology of S-layers has shown that the inner face is often net negatively charged and more corrugated in comparison to the outer face, which shows a neutral charge characteristic and a smooth topography. We have used the S-layer of *Bacillus sphaericus* CCM 2177 in the DUV patterning experiments described in this work [2]. This S-layer exhibits a square lattice symmetry with a lattice spacing of 12.8 nm (Figs. 1 and 2).

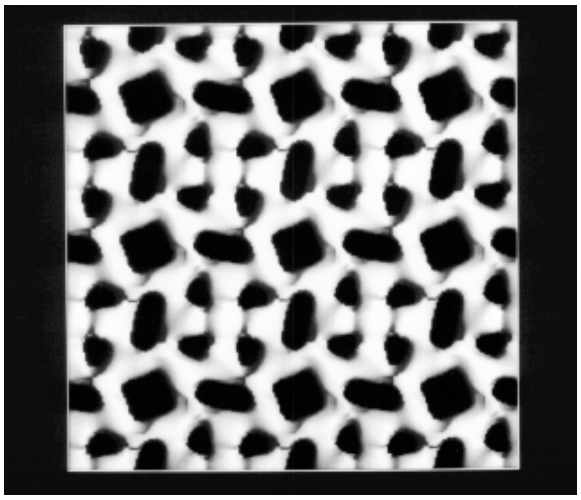

Fig. 1: A computer image reconstruction of an S-layer (square lattice 12 nm, thickness 8 nm).

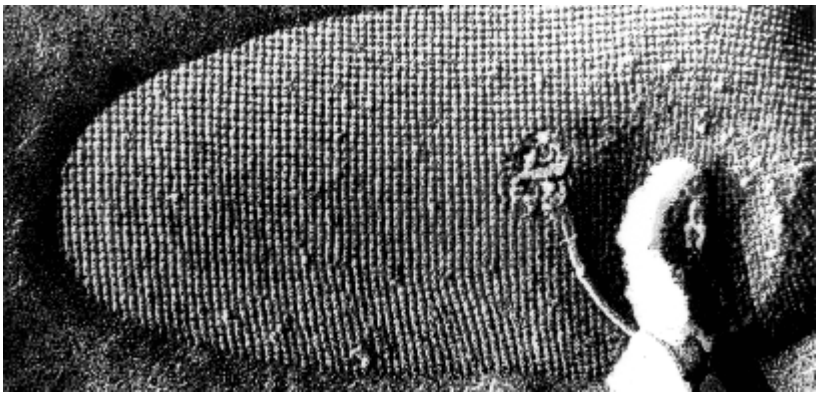

Fig. 2: TEM image of cell surface proteins from Bacillus Sphaericus CCM 2177.

1.2. Experimental

Polished silicon wafers with a native oxide layer (orientation (100)) and hydrophobic characteristics were used as substrates for the recrystallization experiments. The preparation of the S-layers has been described in detail in Ref. [2].

Line and square patterns were transferred onto the S-layer by exposing the protein monolayer to deep ultraviolet ArF and KrF excimer laser radiation (193 and 248 nm, respectively) through an e-beam structured quartz mask with etched antireflective chromium. The S-layer lattice was completely removed by one pulse of ArF radiation with a

dose of 70 mJ/cm^2. The step height between exposed and unexposed areas was approximately 8 nm, which is in perfect agreement with the thickness of the S-layer as determined by scanning force microscopy. In contrast, the S-layer was only carbonized but not ablated even at a dose of ten KrF laser pulses (with 110 mJ/cm^2 per pulse). These results show that the protein adsorbs at least ten times less at the KrF wavelength, compared to the ArF line. Thus we conclude that the energy of the photons at 248 nm is not sufficient to crack the chemical structure of the S-layer. Interference patterns in the S-layer created by the exposure to ArF radiation indicated a gap of 50 – 80 nm between the mask and the S-layer due to a thin intermediate water film.

In our latest results, we succeeded in using the S-layer as the top layer in a two layer resist system. As bottom-layer resist, a spin coated novolak AZ 1350 SF (Kalle Hoechst) was used. This resist film was prepared with a thickness of about 600 nm on a polished silicon wafer after vapor phase HMDS adhesion promotion. It is well known that this resist material may be patterned by KrF excimer laser radiation (248 nm).

The pattern transfer process comprised two steps: First, the S-layer on top of this sandwich system was structured as described above with an excimer laser DUV ablation technique with only one shot at 193 nm (ArF) radiation (with 70 mJ/cm^2). Subsequently, the wavelength was changed to 248 nm (KrF), and the novolak resist at the bottom was ablated with 5 shots at 80 mJ/cm^2 by blank exposure, where the patterned top resist served as a mask material. This is possible because the energy of the photons at 248 nm is not high enough to ablate the top protein resist. The technique presented here yielded very steep sidewalls in the resist material as shown in Fig. 3. The width of the lines is 600 nm, and the width of the gaps, 250 nm.

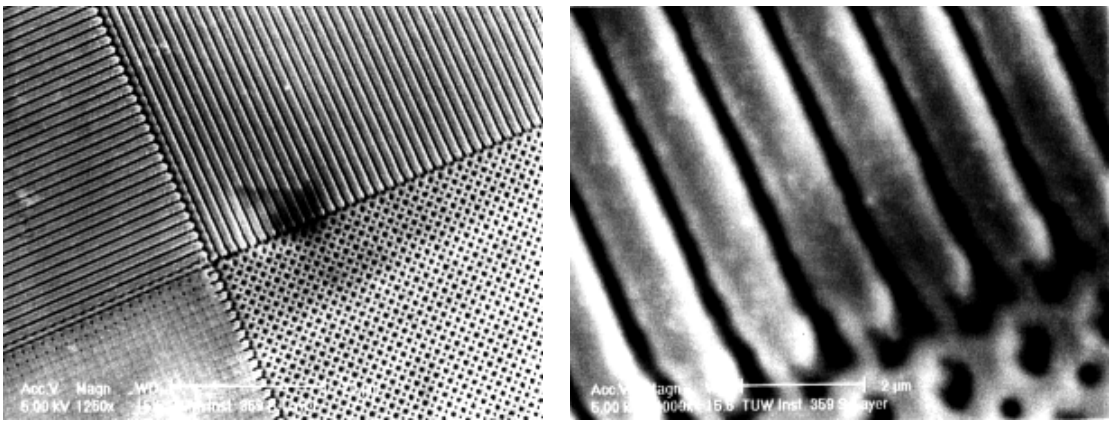

Fig. 3: Scanning electron micrographs of a patterned S-layer/novolak resist assay.

1.3. Conclusion

Many scientific and practical applications of S-layers require a specific patterning with structures down to the sub-micrometer range. DUV radiation proves to be a particularly feasible approach for the pattern transfer because it does not deteriorate the unique properties of S-layer lattices as immobilization matrices for functional macromolecules. A further application of structured S-layers could be the selective growth of embryonic neuronal cell tissue, which could establish a biocompatible interface between microelectronics circuitry and organic cells.

This work has shown that S-layers might be introduced as a novel resist material in microelectronics technology. Practical applications will require some form of reinforcement of the S-layers in order to enhance their resistance against the usual plasma etch processes (Fig. 4). This may be done by coupling additional ligands to the S-layers, or by depositing compounds of heavy metals [4 – 6].

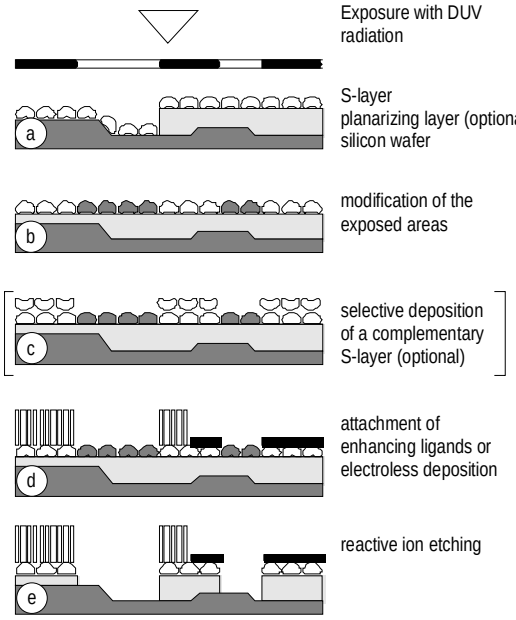

Fig. 4: Schematic illustration of patterning an S-layer recrystallized on a silicon wafer.

2. Micro-Technology of Densely Spaced Non-Conventional Patterns

Regular arrays of sub-0.5 µm tips are of increasing interest, for example, as field emitters, calibration structures, or, in our particular case, as collector surfaces for sub-µm dust particles in a space experiment. This contribution describes the preparation of 1 x 1 cm^2 arrays of columns with a high aspect ratio and a diameter in the sub-micrometer range using a chemically amplified polymer resist (CAR) and electron beam lithography (Fig. 5).

One of the prerequisites for an optimized transfer of the structures by plasma etching from the resist layer into an inorganic substrate (for example, silicon or SiO_2) is a uniformly structured, relatively thick resist layer with close to perpendicular sidewalls, as shown in Fig. 5. This requires a careful optimization of the deposition, exposure, and pre- and post-exposure resist processing. In the experiments reported here, a single film of a three-component negative-toned Novolak CAR (Kalle Hoechst AZ PN 114) has been used. Although the high sensitivity of this resist type makes it very attractive, particularly for electron beam exposure, it causes problems with the control and the uniformity of the critical dimensions. It also requires a careful compensation of proximity effects during electron beam exposure if the pattern dimensions decrease below 0.5 µm, and an optimized resist processing. The most critical factor in resist processing turned out to be the post-exposure delay, which must be less than a few minutes.

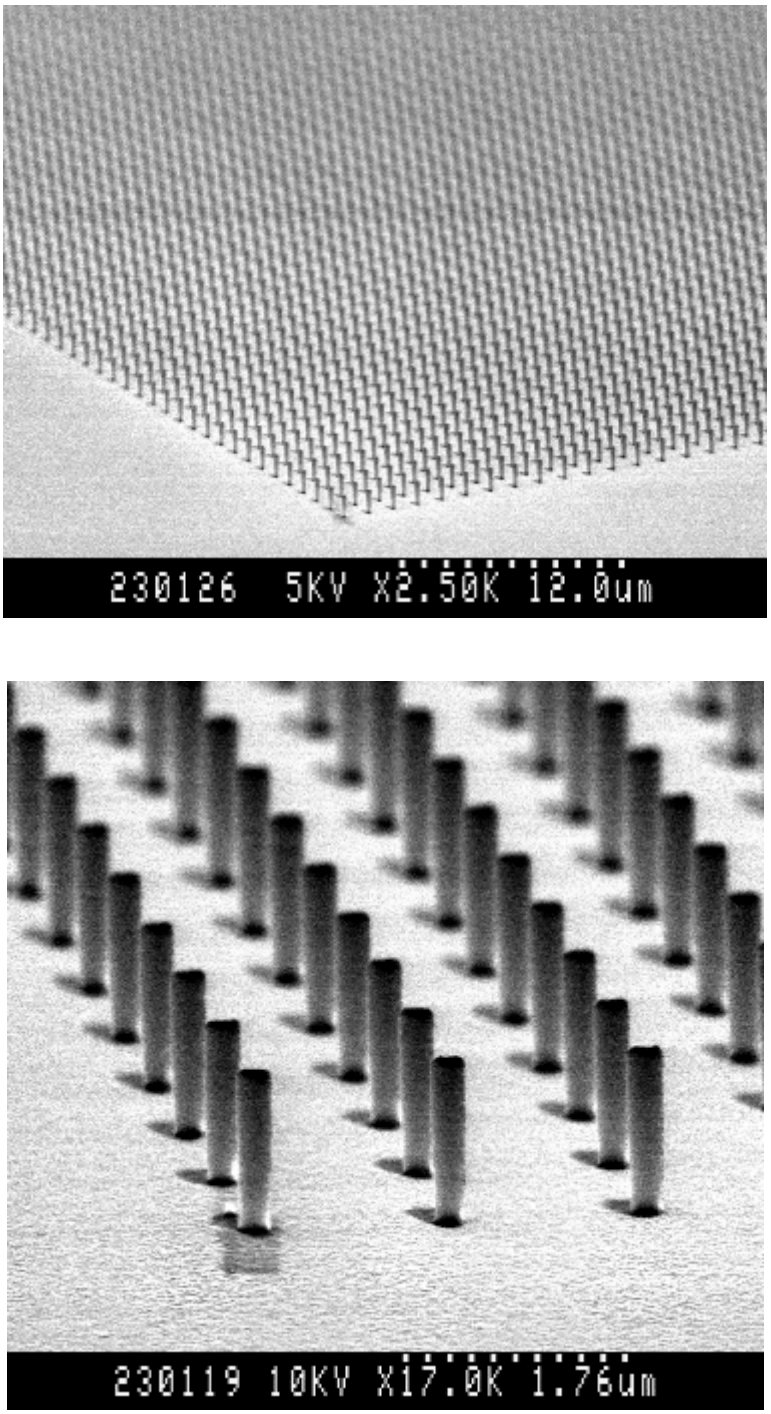

Fig. 5: An array of 1.5 µm high and 150 nm diameter resist pillars (aspect ratio 10:1). The period is 1.0µm.

Although a simulation of the exposure process is indispensable for controlling the proximity effects, the optimization of the entire process heavily depended on experimental work. This is true because the complexity of the three-component resist system and the lack of an exact model of the resist response prohibit a comprehensive simulation.

Acknowledgment

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An Object Oriented Approach to the Management of Models

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The object oriented **M**odel **D**efinition **L**anguage (MDL) for the selection and definition of algorithms or models is presented in this contribution. A number of basic algorithms and parameter types provided by the Algorithm Library can easily be extended by user defined algorithms and C++ classes describing new parameter types. MDL allows to add and/or modify new model algorithms of simulators by defining them on the input deck without recompilation. Model algorithms stored in object libraries or input deck libraries can easily be used by several independent programs.

1. Introduction

Almost any simulator has to provide the functionality to choose from different algorithms or models specialized for solving specific problems dependent on the actual simulation task or user commands. To support model developers in continuously improving these simulators by adding new model algorithms, it is essential to separate these models from the rest of the simulator code and to provide a simple modular mechanism to define, test, and archive them. Therefore the Algorithm Library was developed, which provides an object oriented approach to the programming and handling of model algorithms and the **M**odel **D**efinition **L**anguage (MDL). These algorithms are stored in libraries of object files or ASCII files containing input decks and can easily be reused by other programs or as parts of other algorithms. Automated extraction of log- files and debug information and a report containing information about available algorithms and their documentation is supported.

2. Model and Program Structure

Algorithms provided by the Algorithm Library are represented by C++ classes derived from the base class "`Model`" or its subclasses representing various specific model types [1]. The thereby defined inheritance tree is used to classify the various model algorithms and for run time type checking of expressions defined on the input deck. `Model` classes encapsulate the algorithm itself, private data values used to evaluate the algorithm, an interface containing the required input and output parameters, and the documentation.

New parameter types can be instantiated by specializing the template class "`Parameter`" with an arbitrary C++ class describing the parameter value. This parameter class contains a reference to its value, a default value, the name and the documentation of the parameter. Methods to link several parameters together manage their value references to point to a value shared between them including a run time type

check. For each of these parameters a set of operators and functions can be specified which can be used in calculations defined on the input deck as well as in algorithms defined in C++.

A different approach to support the development of models is presented in [5], where the modeling language PMDL is introduced. The PMDL compiler provides a subset of the C language extended by data types and expressions dealing with mesh data and the automated generation of the Jacobian matrix. In distinction to this the Algorithm Library is designed to support libraries of arbitrary user defined data types and algorithms without any specialization.

A basic set of predefined algorithms and parameter types providing all standard C++ data types and basic operations on them, is already provided by the Algorithm Library. These can be extended at any time by additional user defined libraries of further algorithms and parameter types or by using the Model Definition Language.

An instance of a specific algorithm can be generated by forwarding the model type name to the Algorithm Library or by giving an instance name for the algorithm. In this case the actual class type is determined at run time by parsing the input deck. To evaluate the algorithm, its class instance is connected to an interface providing the necessary parameter values.

A minimal program using the Algorithm Library to evaluate a single algorithm may be structured as following:

1. Initialize the Algorithm Library by parsing the input deck.
2. Create the interface containing all parameters and the required model type.
3. Request a model instance from the Algorithm Library and link it with a specified parameter interface.
4. Repeat as necessary: Compute the values of the input parameters.
   Evaluate the model.
   Use the resulting parameter values for further computations.
5. Delete the interface and the model instance.

Steps 1–3 should take place during the initialization phase of the program because they require the rather time consuming parsing and interpretation of the input deck. Once the internal data structures of the Algorithm Library are assembled, the additional time consumption caused by the usage of the Algorithm Library are typically between 5 – 50 % depending on the complexity of the models.

3. Model Definition Language

The Algorithm Library contains a parser for the Model Definition Language which allows to:

- Define the actual algorithms to be used for a specific task.
- Define the default parameter values of a certain model instance.
- Define global parameters.

- Define new algorithms consisting of previously defined models and calculations with global and local parameters. Arbitrary loop and condition expressions can be expressed by using special model classes.
- Request a report describing all available algorithms, their interfaces and the thereby defined model hierarchy.
- Request a report describing the actually used algorithms and/or parameter values for a specific model instance.

4. Example

To give a short example for the usage of the Model Definition Language, a simple carrier mobility model is defined by combining a lattice scattering model with a carrier-carrier scattering model using the Mathiessen rule. The interface for all carrier mobility models (class name `MobilityModel`) contains among others the parameters `temp` (lattice temperature in $[K]$), `mu` (the resulting carrier mobility in $[cm^2 V^{-1} s^{-1}]$) and `np` (the product of the electron and hole densities in $[cm^{-6}]$). It is assumed that an abstract class `MobilityModel` which defines the interface for all carrier mobility models and the following simple lattice scattering and carrier-carrier scattering models are already contained in a Model Library or defined in a previously scanned input deck file:

Lattice Scattering [2]:

$$mu = mu0 \cdot \left(\frac{temp}{300} \right)^{-alpha}$$

Carrier-Carrier Scattering [3]:

$$mu = \frac{1.428 \cdot 10^{20}}{\sqrt{np} \cdot \ln\left(1 + 4.54 \cdot 10^{11} \cdot (np)^{-1/3}\right)}$$

Listing: Input deck defining a new carrier mobility model for electrons

```
CombinedModel LC_Mobility : MobilityModel {
   Model LatticeScatteringMobility "LSMob";
   Model CC_ScatteringMobility    "CCSMob";

   // new default values for some sub models
   Parameter " LSMob"."mu0" = {{1448}};
   Parameter " CCSMob"."alpha"  = {{2.33}};

   link Interface."temp" to "LSMob"."temp";
   link Interface."np" to "CCSMob"."np";

   calc "MatthiesenRule" {
      Interface."mu" = 1/("LSMob"."mu" + 1/ "CCSMob"."mu");
   }

   EvaluationOrder "LSMob", "CCSMob", "MatthiesenRule";
}

// Specify the actual Mobility Model Type to use
Model "MobilityModel" = LC_Mobility;
```

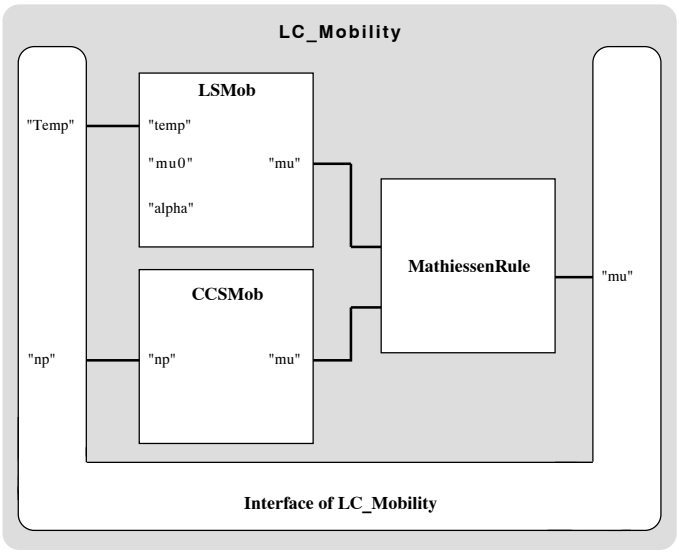

Fig. 1: Block diagram of the new carrier mobility model

5. Conclusion and future aspects

By using the model library a clean interface is introduced between modularized algorithms and the rest of the program. These algorithms can easily be replaced by newly defined ones during run time without any additional coding efforts within the simulator. Due to the relatively low run time performance losses and the great simplifications in introducing new algorithms into existing simulators, the Algorithm Library is a valuable tool for simulator and model development and their daily usage.

Acknowledgment

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AMIGOS: Analytical Model Interface & General Object-Oriented Solver

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To accurately simulate modern semiconductor process steps, a simulation tool must include a variety of physical models and numerical methods. Increasingly complex physical formulations are required to account for effects that were not important in previous generations of technology. As a specific example, the oxidation coupled with impurity diffusion mechanisms as well as chemical reactions are not well understood, and thus flexibility in definition of models is highly desirable. An object oriented approach has been applied to implementing a 1-2-3D PDE solver, which uses an analytical input interface in the manner of Mathematica, Mathcad, Mathlab, etc. but is highly optimized for high performance semiconductor modeling.

1. Introduction

The development of new complex physical models and its practical realization requires a large expenditure of time. To reduce this amount of developing time we analyzed the requirements for a general solver carefully and separated the common features such as modeling for physical definitions, parameter and model library, grid-adaptation, numerical solver, simple front-end controller as well as geometry and boundary definition. As a result we developed AMIGOS that translates a mathematical formulation of any discretized coupled partial differential equation system into a highly optimized model, which will then be passed to a nonlinear numerical solver that can handle different physical models on various grids as well as interfaces and boundaries.

AMIGOS also provides several layers of access to the variety of users. For example, a process engineer (user-mode) may need only to select a model appropriate for the process step to calculate (e.g. diffusion coupled oxidation), modify the process parameters (e.g. duration, temperature, material characteristics, etc.) and defines the geometries and boundaries the process should be calculated on. On the other hand, at a lower level (developer-mode) a model developer may need to modify existing equations by adding several parameters, mathematical terms or equations, or even develop a completely new model. In contrast with previous generation of software none of the described modes needs access to and modification of the source code. In developer mode the user may choose between a one-pass or two-pass concept. The one-pass concept requires no recompilation and supports fast testing possibilities of the developed model. After finishing the test and calibrating phase the user may switch to the two-pass concept where all his modifications are translated to C code and are linked to a model library for high performance calculations on large simulation domains.

2. Design of AMIGOS

In difference to similar algorithms working with the so called ‘operator on demand’ concept [1], AMIGOS is completely independent of the kind of discretization since the model developer himself can formulate a discretization of his choice (e.g. Bernoulli discretization which is very important for semiconductor device simulation). There are no restrictions whether using scalar, field or even tensor quantities within a model and, if desired, any derived field quantity can be calculated, too. Furthermore, the user can influence the numerical behavior of the differential equation system, since he has complete control of the residual vector and its derivative (e.g. punishing terms, damping terms, etc.). Even interpolation and grid-adaptation formulations can be used within a developed model and can thus be very well fitted to the special problem. To illustrate the powerful possibilities of AMIGOS we will introduce a rigorous model of the moving grid problem arising from thermal oxidation within a semiconductor process step in the example below.

The object-oriented extension provides an efficient and versatile means to represent the organization of AMIGOS in an easy to grasp manner regarding to its complexity.

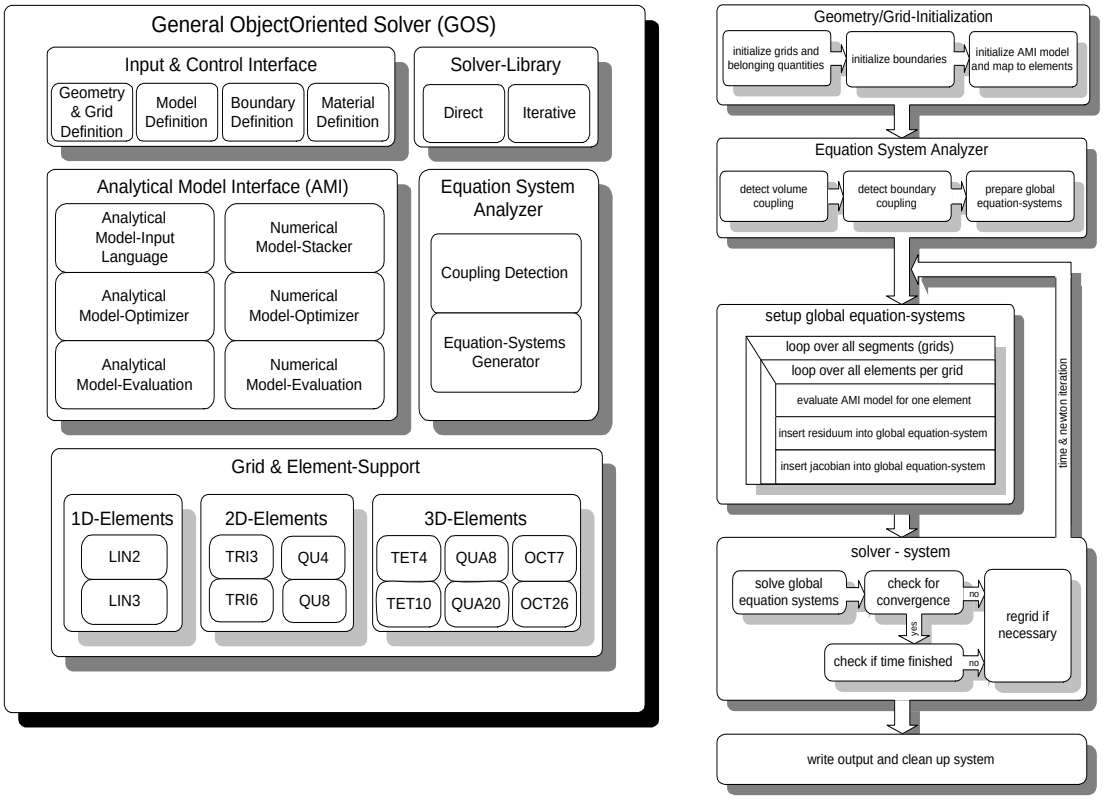

Fig. 1: Structural design and flow chart of AMIGOS

3. Example: A rigorous oxidation model

The evolution of isolation techniques and the progressive miniaturization in semiconductor devices makes it necessary to develop new and much more complex models to exactly describe the behavior of the thermal oxidation processes.

The profusion of different requirements such as chemical reactions and its resulting volume expansion as well as the mechanical stress and pressure calculations leading from elastic over viscoelastic to viscous behavior coupled with the oxidation diffusion and its recombination with Silicon represents just the modeling problem of the calculation process. In addition to these problems comes the effect that the order of magnitude varies between a few nanometers to a hundreds of nanometers which is impossible to solve without accurate grid-adaptation.

Using AMIGOS we were able to develop a model which takes all these effects into account solving a coupled differential equation system according to a total lagrangian formulation concerning nonlinear grid deformation (Fig. 3).

The idea of our model is to simulate the interface between Si and SiO_2 by a trap function depending on a generation/recombination model of oxygen and silicon. Thus we can distinguish between different mechanical material characteristics depending on the value of the trap function. So it can be managed that within one single grid several different mechanical models can be calculated.

At the free silicon surface oxygen diffuses into silicon and the chemical reaction transforms it to SiO_2. Because of a volume ratio of $Si:SiO_2$ from 1:2.2 the volume expands. At the same time the mechanical behavior changes continuously from elastic within silicon to viscous within SiO_2 which leads to the typical deformation of the silicon block (Fig. 2). The advantage of this model approach is that in contrast to conventional modeling no regridding is necessary, because the maximal volume ratio of a single grid-element is also just 1:2.2 and the grid quality can be preserved.

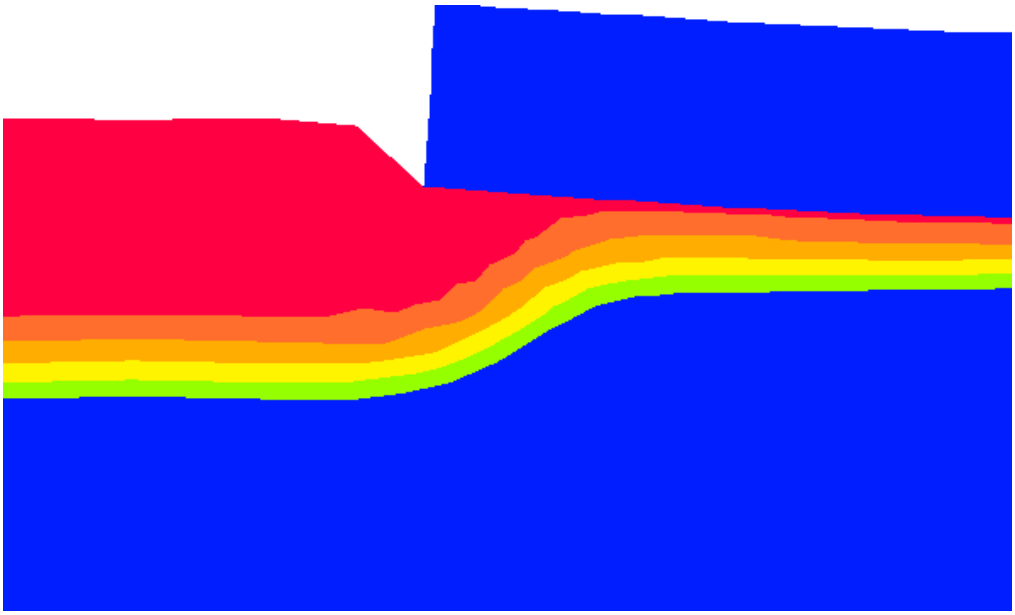

Fig. 2: Simulation result of a LOCOS

The mathematical formulation of the model:

recombination ratio of Si/O2:

$$R_o = k_o\left(1 - SiO_2\right) \cdot O$$

diffusivity of oxygen:

$$\frac{\partial O}{\partial t} = div[D \cdot grad(O)] - 2R_o$$

generation ratio of SiO2:

$$\frac{\partial SiO_2}{\partial t} = R_o$$

momentum conservation:

$$\frac{\partial p}{\partial x} - \mu \cdot (\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2}) = 0$$

$$\frac{\partial p}{\partial x} - \mu \cdot (\frac{\partial^2 v}{\partial x^2} + \frac{\partial^2 v}{\partial y^2}) = 0$$

continuity condition:

$$\frac{\partial u}{\partial x} + \frac{\partial v}{\partial y} = k_p \cdot R_o$$

The representation of the differential equations using AMIGOS's mathematical input language:

```
MODEL Oxidation = [X,Y,P,O,SIO2];
{
   source FiniteElementDiscretation(2,3)
   dt    = t.t0 - t.t1;    dX    = X.t0 - X.t1;
   dO    = O.t0 - O.t1;    dY    = Y.t0 - Y.t1;
   dSIO2 = SIO2.t0 - SIO2.t1;
# the discretized operators
   L(xsi,eta) = [ [dNdx(xsi,eta)  ,      NULL     ]
                  [     NULL      ,  dNdy(xsi,eta)]
                  [dNdy(xsi,eta)  ,  dNdx(xsi,eta)]];
   Nabla(xsi,eta) =[[dNdx(xsi,eta)]
                    [dNdy(xsi,eta)]];
   f(x,y)  = [[x,0]
              [0,y] ];      # ... function of diffusivity of oxygen
   param Dx,Dy;             # ... diffusivity of oxygen

# the stiffness matrix for diffusion
   K = w_1 * detJ * Nabla(xsi_1,eta_1)^T * f(Dx,Dy) *
Nabla(xsi_1,eta_1);
   K1 = w_1 * detJ * Nabla(xsi_1,eta_1)^T * Nabla(xsi_1,eta_1);
   Kt[i,i] = w_1 * detJ * K1[i,i];

   Ro[i] = ko*(1-SIO2[i])*O[i];          # ... recombination ratio
   resO = K * O + Kt * dO/dt + Kt * Ro;   # ... residual of O2
equation
   resSIO2 = Kt * dSIO2/dt - a * Kt * Ro; # ... residual of SiO2
equation
#----------------- the mechanical equations -------------------------
-#
   param E_Si,n_SiO2,n_Si,G_Si,G_SiO2,K_Si,K_SiO2
   G = (1-SiO2) * G_Si + SiO2 * G_SiO2;
   Kappa = (1-SiO2) * K_Si + SiO2 * K_SiO2;
   D1 =    [      [ 4/3 , -2/3 , 0 ]D2 = [   [1 , 1 , 0]
                  [-2/3 ,  4/3 , 0 ]         [1 , 1 , 0]
                  [ 0   ,   0  , 1 ]];       [0 , 0 , 0]];
   D = Kappa * D2 + G * D1;  m = [[1][1][0]];
# the mechanical stiffness matrices
   B(D) = w_1 * detJ * L(xsi_1,eta_1)^T * D * L(xsi_1,eta_1);
   Q = -1 * w_1 * detJ *L(xsi_1,eta_1)^T * m * N(xsi_1,eta_1);
   H[i,i] = detJ / (1.0E7-n_SiO2*1.0E10); # ... punishing term

   resM = B(D) * [[dX][dY]] + Q * P;# ... residual of momentum
   resP = Q^T * s + H * P +         # ... residual of continuity
          coppl * detJ * w_1 * 1.2/(1+1.2*SiO2) * dSIO2;
   gridcrit = N(xsi_1,eta_1) * dSIO2;        # ... the grid criterion
# ... the total residual vectorto be solved for
   residuum = [[resM][resP][resO][resSIO2]];
```

Fig. 3: The modeling equations and their formulation within AMIGOS's input language

4. Conclusion

With AMIGOS we have developed a powerful model development tool which supports the major interests of numerical engineering. The consequent progress in semiconductor device fabrication makes it necessary that simulation tools have to become increasingly flexible to keep up the pace of advance. First steps are taken to fulfill these requirements.

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Point and Extended Defects in Ion Implanted Silicon

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1. Introduction

Ion implantation is central to almost all silicon device manufacture. It provides the capability of close control of the amount of dopant incorporated and the ability to create grossly non-equilibrium dopant profiles. Unfortunately, all ion implantation creates some damage in the silicon lattice, this can range from low concentrations of atomic displacements to total amorphisation dependent on the dose, energy and mass of the implanted species. In order to restore the electronic properties of the silicon, some form of annealing always follows the actual process of ion implantation. Consequently we have to consider the entire ion implantation thermal anneal cycle when examining the defect population which may effect subsequent device performance.

Taking silicon device manufacture in general, we are interested in three types of defect: point defects which can act as recombination centres, point defects which can act as generation centres and extended defects which have pronounced recombination/generation activity when decorated with impurity atoms. Extended defects can also provide the mechanisms for junction shorts and anomalous diffusion. Let us first consider the role of recombination/generation centres in the device environment.

2. Recombination-Generation Models

It is important to remember that the electrical activity of an impurity depends not only on its chemical nature but also on its exact siting in the lattice. Similarly, displaced silicon atoms contribute to the electrical activity as vacancies or interstitials, or as a result of complexes formed such as the oxygen-vacancy A-centre.

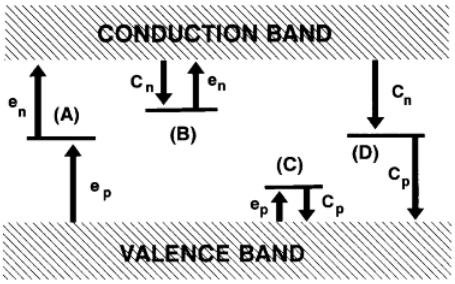

Fig. 1: The classic Shockley-Hall-Read representation of : A) a generation centre, B) an electron trap, C) a hole trap, D) a recombination centre. where arrows show the direction of electron transfer.

Process A) defines the generation lifetime in a material or a device region and technologically is by far the most important process in integrated circuits design for signal processing or data storage. For example, it is the key parameter in setting the refresh rate required for dynamic RAM. Although most text books emphasise process D), recombination, which is often the dominating factor in defining the minority carrier lifetime, it is of relatively little significance in signal processing devices. It is, however, of major significance in power semiconductors and in opto-electronic devices (solar cells, LEDs and opto detectors). The processes B) and C) can contribute to noise in devices but in the present context have more significance in our detection of the presence of deep states by techniques such as DLTS. It is important to note that a mid-gap defect can behave as a recombination centre, a generation centre or as a trapping state. Its role depends much more on the environment it finds itself in than on the physical characteristics of the defect. For example, the same state could well be a generation centre in the depletion region and a recombination centre in the bulk.

3. Annealing

The objective of annealing ion implanted silicon is to remove the implant damage. In many cases this needs to be done without redistributing the impurities and so there is always a conflict between total removal of defects (which may require a larger thermal budget) and restricting the movement of dopants. This is a particularly critical problem when very shallow junctions are required (as in ULSI) or where complex doping profiles need to be established (as in varactor diodes, for example). If the diffusion process and the defect removal process have very different activation energies, there will be advantages in using long low temperature anneals or short high temperature anneals (RTA) dependent on whether the defect removal activation energy is greater or less than the diffusion activation. The concept is illustrated in Fig. 2.

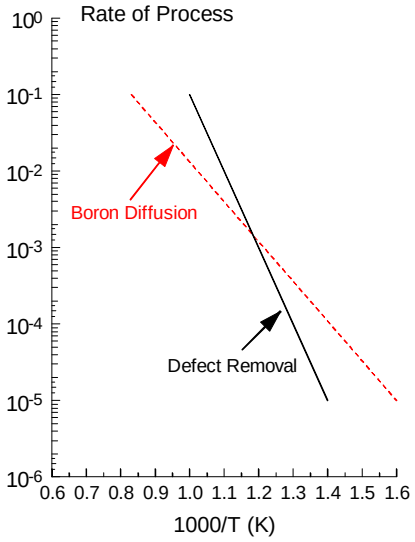

Fig. 2: Arrhenius plot of relative process rates occurring during annealing.

Unfortunately, the choice of annealing schedule is complicated by a number of factors among these is the simple observation that several defect species are important in optimum device operation. They have quite different annealing kinetics which include de-

fect reactions during annealing resulting in the formation of new species. The other major complication is that the diffusion rate of some dopant species, the classic example of which is boron, is dramatically affected by the presence of defects, particularly silicon self interstitials. These factors make generalisations difficult and indeed detailed anneal schedules tend to be process/device specific.

4. Extended Defects

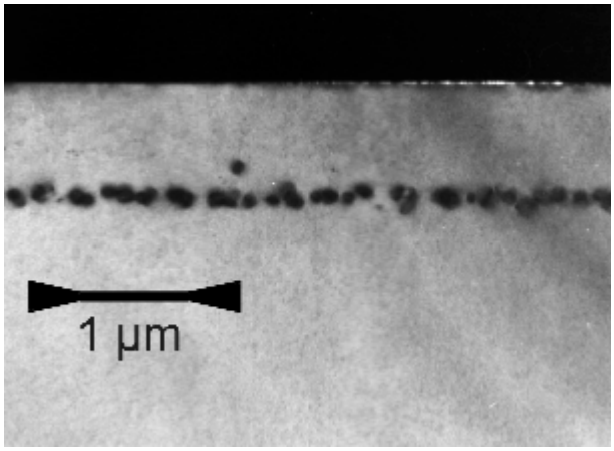

Fig. 3. Cross-sectional TEM image of end of range dislocation loops in amorphised/ regrown silicon.

Heavy implants will, in general, produce a significant excess of silicon self-interstitials. The anneal process will tend to remove these to stable locations. Ideally this should be the surface of the semiconductor where they will simply form one or more additional atomic layers of silicon. If the dynamics of the anneal process are such that they cannot reach the surface, they will form dislocations. Figure 3 shows a silicon layer which has been amorphised by a germanium implantation and then slowly regrown at 650 °C in a slightly oxidising atmosphere. The growth of a few mono-layer of oxide at the surface creates additional interstitials which prevent the migration to the surface of the excess interstitials in the implanted region and so the self interstitials condense into dislocation loops at the original crystalline/amorphous boundary. If the same annealing schedule had taken place in a reducing atmosphere (hydrogen) no loops would be present. Many other factors influence the formation of dislocations including the abruptness of the transition from damage to crystalline silicon and the presence of inadvertent metallic species.

5. Decoration of Extended Defects

Extended defects are very important in semiconductor device fabrication because of their electrical activity, distortion of the band gap, and because of the local enhancement of diffusion of dopant species (the long established process of so-called pipe diffusion). It is now generally accepted that only undecorated (clean) dislocations have little or no electrical activity. In semiconductors the term “decoration” has come to be used to describe a quite low concentration of atoms at the dislocation as distinct to the metallurgical sense where decoration would imply a visible precipitation of impurity

atom in the vicinity of the dislocation. The strain field of the dislocation enables mobile impurities to move against the concentration gradient and so accumulate an even precipitate in the vicinity of the dislocation. It is this accommodation of mobile impurities which make extended defects so important in semiconductor processing and ion implantation in particular. Ion implantation processing errors can produce extended defects but is also a potential source of metallic contamination which affects the electrical behaviour of the extended defect by low level decoration

Finding such defects is not easy using conventional methods such as TEM, there are simply not enough of them to occur in the average TEM sample volume and so other methods of detection are being explored.

6. Point Defects

As indicated previously, many defect species are produced by implantation and these react to form secondary defects and complexes during annealing. The highest concentration of defects occur in the tail of the implant. This is shown clearly in Fig. 4, which illustrates the evolution of deep states effecting the background doping. This results from a germanium implant into silicon with anneal schedules as shown. Deep Level Transient Spectroscopy (DLTS) and related techniques have been used to study the reactions of these defect species during annealing and in some cases it is possible to relate the electrical fingerprint to the molecular structure of the defects. It is becoming apparent that the presence of impurities in the silicon (oxygen, carbon, hydrogen and transition metals) can have a profound effect on the effectiveness of the annealing schedule.

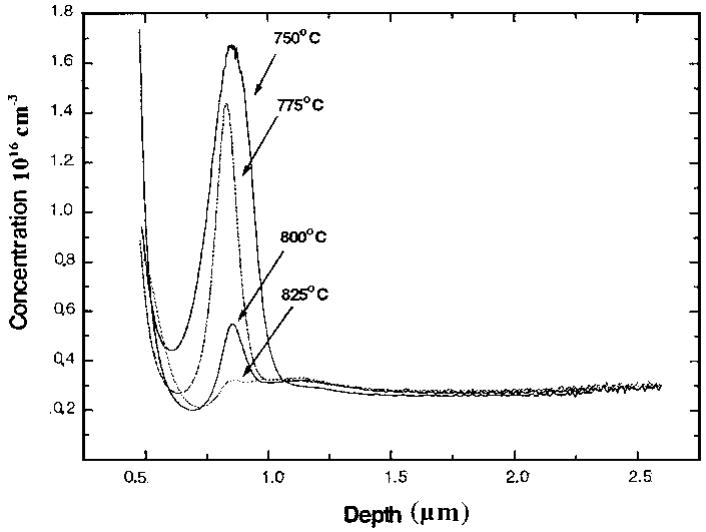

Fig. 4: Apparent electron concentration in n-type silicon ion-implanted with 400 keV germanium with a dose of 10^{15} cm^{-2}. The samples were annealed at the temperatures shown for 10 minutes.

7. The Future

It is only in the last few years that defect management in semiconductor processing has been put on a firm scientific basis. However, new issues can be perceived which have received very little consideration so far. In particular the statistical nature of defect distribution is evident when it is realised that a sub-micron DRAM cell will work well with three point defects in the active region but fail if six are present. These issues and possible diagnostic techniques will be discussed in the talk.

Ge^+ Implantation into Silicon: Behavior of Deep Level Defects

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Implantation-induced defects and their annealing behavior in Si and SiGe have been investigated using deep-level transient spectroscopy. For Ge^+ implantation in silicon three types of defects have been observed: vacancy-related defects which anneal out during annealing up to 600 °C, Ge-related defects which are formed during annealing and disappear at 900 °C, and radiation defects which are generated during annealing and disappear also at 900 °C. For ion bombardment of strained SiGe layers we found a strong influence of the strain on the production, diffusion and annealing of implantation-induced defects.

1. Introduction

Strained Si/SiGe layers can be used to improve the performance of silicon based electronic devices such as heterobipolar transistors and modulation-doped field effect transistors [1]. The Si/SiGe heterostructures are usually grown on Si substrates by molecular beam epitaxy at relatively low temperatures (< 750 °C). However, during the fabrication of a device, a number of ion implantation and high temperature annealing steps would typically follow the epitaxial growth. These processing steps are known to introduce defects or to modify already existing defects and can cause strain relief in the strained layers. At present, the properties of implantation-induced defects and their high-temperature annealing behavior in SiGe layers remain largely unstudied. Implantation-induced defects are also important in the case of ion-beam-synthesized SiGe layers. It has been shown that simple SiGe/Si heterostructures can be fabricated by ion implantation and solid-phase epitaxial regrowth [2].

In the context of these problems, a program was started to investigate implantation induced defects and their annealing behavior by deep-level transient spectroscopy (DLTS). Two aspects have been treated so far. First, the formation and annealing behavior of deep level defects after implantation of Ge^+ into Si, and second, the influence of the mechanical strain on radiation defects.

2. Experimental

Phosphorus-doped CZ-grown Si wafers were implanted with 320 or 640 keV Ge^+ ions with doses up to $3x10^{16}$ cm^{-2} corresponding to a peak Ge concentration of about 3 at.%. Deep level defects were investigated after subsequent isochronal annealing steps in the temperature range 100 – 1100 °C. Rapid thermal annealing (RTA) of the samples was performed by halogen lamp irradiation with 20 s exposure in a nitrogen gas flow. Deep-level transient spectroscopy measurements [3] were carried out using a 1 MHz capacitance bridge, a pulse generator and a liquid-nitrogen-cooled cryostat (77 – 400 K). The

DLTS signal was obtained from the capacitance transient using the lock-in averaging method. Depth profiles of defects were obtained in double-pulse differential mode (DDLTS) [4].

Due to a 4% difference between the covalent radii of Si and Ge atoms the implantation of Ge into Si allowed us to vary the magnitude of the elastic misfit stress. The mechanical strain was investigated by high-resolution x-ray diffraction measurements using a four-crystal monochromator [5]. Some of the strained Ge^+ implanted samples (in the following designated as Si:Ge) were then irradiated with 24 or 70 keV H^+ ions at doses between $1x10^{10}$ and $1x10^{12}$ cm^{-2} to introduce radiation defects. The H^+ implantation energy was chosen such that the radiation defects were placed into the region of the maximum gradient of the Ge concentration. All the ion ranges were calculated with the TRIM code [6]. The radiation defects formed by H^+ irradiation were electrically characterized again by DLTS measurements.

3. Results and discussion

3.1. Deep level defects in Ge^+ implanted Si

Three groups of deep levels have been observed by DLTS in the implanted samples. The first group of defects is observed in as-implanted samples and in samples annealed at low temperatures. Figure 1(a) shows a typical DLTS spectrum of Si implanted with a low dose of Ge^+. The defects are labeled according to their energy position in the gap in eV. Three defects are detected in such samples: E(0.17), E(0.22) and E(0.41). Annealing experiments show that these defect levels are observed up to about 600 °C annealing temperature. The concentration of the defects decreases continuously with the annealing temperature.

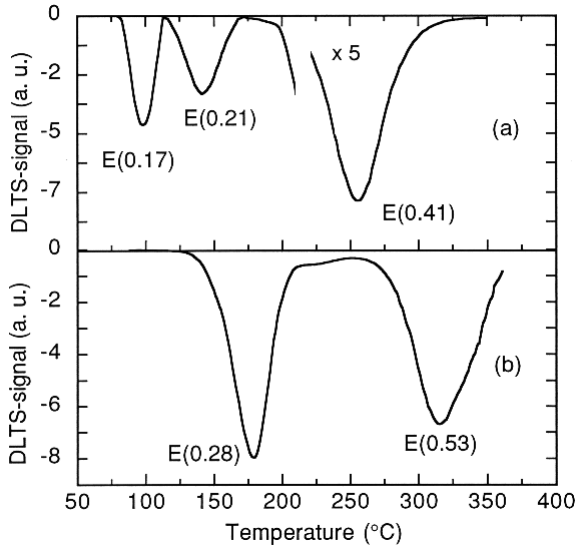

Fig. 1: DLTS spectra of Ge^+ implanted Si (640 keV): (a) dose 10^{11} cm^{-2}, annealing at 100°C; (b) dose 10^{12} cm^{-2}, annealing at 700 °C.

The second group of defect levels is observed after high temperature annealing. Figure 1(b) shows a typical DLTS spectrum of Ge^+ implanted Si after annealing at 700°C. Two new defect levels, E(0.28) and E(0.53), are observed instead of those in as-implanted silicon. The new levels show up at about 500 °C and disappear only after annealing at very high temperatures (> 900 °C). In samples implanted at doses above 10^{13} cm^{-2} an additional minority carrier trap E(+0.17) is observed after 700 °C annealing, which disappears also above 900 °C. The third group of defect levels — two less dominant levels at E(0.40) and E(0.15) — is also observed after high temperature annealing between 700 and 900 °C.

The three levels observed in as-implanted silicon can be attributed to vacancy-related defects: E(0.17): vacancy-oxygen pair, E(0.21): divacancy, and E(0.41): a mixture of the divacancy and the phosphorus-vacancy pair [7]. The position and shape of the defect profiles measured by DDLTS coincides very well with the vacancy distribution calculated by the TRIM code. The profiles are shifted towards the surface as compared with the ion distribution.

The levels E(0.28) and E(0.53) observed in the temperature region 500 – 900 °C can be attributed to defect complexes containing Ge atoms. The position and shape of the profiles of these levels coincide with the profile of the ion distribution according to TRIM. The Ge-related levels are not formed during ion implantation, they are created during the annealing as a result of the recrystallization of amorphous inclusions and the release of Ge atoms from them. This process is accompanied by a sharp decrease of the defect-related mechanical strain.

The levels E(0.15) and E(0.40) observed after high temperature annealing are not related to the implanted species. From the shape of the defect profiles and from the fact that similar levels were observed also in Si^+ implanted silicon it is concluded that the levels are related to radiation defects. The defects are generated during the recrystallization of amorphous inclusions and are not observed after implantation at doses above 10^{13} cm^{-2}.

The main message of our study of deep levels in Ge^+ implanted silicon together with strain measurements for the SiGe technology is that it is possible to obtain SiGe layers after implantation of Ge^+ into silicon and appropriate annealing. The radiation defects can be annealed out completely and the Ge atoms are introduced on regular lattice sites. So far experiments have been performed only with low Ge concentrations (up to 3 at%). Since for doses above the amorphization dose (about 10^{14} cm^{-2}) the annealing of the radiation defects occurs by solid state epitaxial regrowth, higher Ge concentrations are not expected to cause difficulties.

3.2. Influence of mechanical strain on radiation defects

The response to ion implantation is different for a strained SiGe layer and unstrained silicon. This has been found by investigating radiation defects after bombardment with H^+ ions. H^+ bombardment of Si introduces the vacancy-related defect levels E(0.17). E(0.21) and E(0.41) as described above, and in addition, a H-related level E(0.30) [7].

The production rates of these defects are essentially lower in strained Si:Ge samples. The decrease of the defect concentrations in Si:Ge as a function of the stress is shown in Fig. 2. The concentration of the defects was obtained from DLTS and DDLTS measurements, the stress was calculated from the strain in the implanted layer measured by x-ray diffraction [8]. DDLTS measurements have shown that defect profiles are signifi-

cantly broader in Si:Ge samples than in silicon. The annealing behavior of the deep levels is also different for Si and Si:Ge. The annealing of the vacancy-related defects generally takes place in two stages. In the Si:Ge samples the beginning of both stages is shifted towards lower temperatures. The onset for the annealing of the H-related level E(0.30) is also shifted to lower temperatures in the Si:Ge samples.

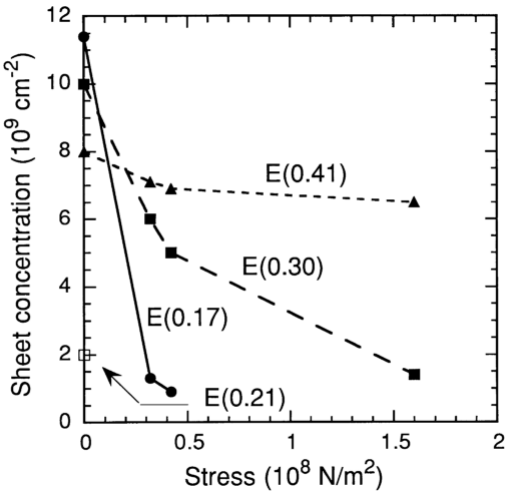

Fig. 2: Concentration of the defects in Si:Ge introduced by H^+ bombardment (70 keV, $5x10^{10}$ cm^{-2}) versus the Ge-related stress calculated from the measured strain. Stress zero denotes the Si reference sample.

The behavior of the radiation defects in Si:Ge cannot be explained by changes in the primary defect production (vacancies and interstitials) during bombardment due to the slightly changed stoichiometry. It is concluded that the Ge-related misfit strain is responsible for the reduced production rates of the observed defects, broadening of the defect profiles and the shift of the annealing stages. The production of primary defects (vacancies and interstitials) during ion bombardment and their behavior afterwards (diffusion, annihilation, capture by impurities, etc.) takes place in a field of mechanical stress. Elastic energy can be transferred to primary defects, thus influencing their behavior and the formation of defect complexes observed by DLTS. A detailed discussion is given in refs. [8] and [9].

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$Si_{1-x-y}Ge_xC_y$ Layers: Growth and Characterization

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We report on the structural and optical properties of silicon-based heterostructures containing ternary $Si_{1-x-y}Ge_xC_y$ alloys. Both single and multiple quantum wells were grown by molecular beam epitaxy and their quality was assessed by x-ray rocking analyses and by photoluminescence (PL) measurements. Optimum growth temperatures with respect to carbon incorporation and layer quality were found to be at around 500°C. We observed well behaved PL signals from $Si_{1-y}C_y$ single layers and Si/ $Si_{1-y}C_y$ multiple quantum wells as well as from $Si/Si_{1-y}C_y/Si_{1-x}Ge_x$ superlattices with carbon concentrations up to 1.7%. For an investigation of the thermal stability of these intrinsically metastable layers, ex-situ annealing experiments were conducted in the temperature range between 500°C and 900°C. Up to about 725°C an improvement of the PL signals both with respect to intensity and linewidth is observed, whereas the amount of substitutional carbon remained unaffected. After annealing at 725°C we observed the narrowest linewidth in a $Si_{1-y}C_y$ single layer reported so far in the literature. At higher annealing temperatures the PL signal decreases, but it takes more than 850°C to observe a decrease of the substitutional carbon concentration in x-ray measurements. The results indicate that carbon containing epi-layers of high crystal quality can be grown by MBE, and that thermal stability is good enough to make the material interesting for device applications.

1. Introduction

It is the outstanding property of Si-based heterostructures to provide the application relevant combination of bandstructure engineering and silicon very-large-scale-integration (VLSI) compatibility. In the past few years most of the basic properties regarding the lattice mismatched $Si/Si_{1-x}Ge_x$ material combination, and especially the effects of strain on the band offsets and bandgaps, have been investigated [1]. It has been found that the band offset at the interface between a pseudomorphic $Si_{1-x}Ge_x$ layer and a Si substrate occurs almost exclusively in the valence bands, whereas a tensilely strained Si layer is required for the implementation of useful conduction band offsets. By employing proper combinations of pseudomorphic and strain-relaxed epi-layers, both tensile and compressive strains can be custom designed, without sacrificing the important advantages of a Si substrate and the basic compatibility with Si technologies.

By exploiting *strain-engineering* as an additional degree of freedom, a wide variety of devices structures have been implemented in the $Si/Si_{1-x}Ge_x$ material system, reaching from heterobipolar transistors (HBT) [2] over p- and n-type modulation-doped field effect transistors (MODFET) [3] to optical detectors in the near infrared, and even light emitters [4]. Nevertheless, so far only the pseudomorphic Si/SiGe HBT has reached production status, whereas other devices with demonstrated superior properties, such as the n-type MODFET, are still restricted to test devices on a laboratory level. The main reason for the much slower development of the MODFET lies in the necessity for strain

relaxed $Si_{1-x}Ge_x$ buffer layers. These have successfully been implemented by several research groups [5] – [7], but defect and morphology control still require further refinement to make them suited for a production environment.

Ternary $Si_{1-x-y}Ge_xC_y$ alloys offer an alternative route to strain-engineering in silicon-based heterostructures, which finally may overcome the problems imposed by relaxed buffer layers: Due to the covalent radii of C and Ge, which are smaller, and larger than that of Si, respectively, both compressively and tensilely strained, pseudomorphic layers can be implemented by proper adjustment of x and y in the active layers of a heterostructure [8]. However, in contrast to the binary $Si_{1-x}Ge_x$ alloys, which are thermodynamically stable for all compositions x, carbon has almost negligible solid solubility in both Si and Ge, but, on the other hand, tends to the formation of stoichiometric SiC. Since strain engineering requires C concentrations of a few percent to provide useful modifications of the band structure [9], non-equilibrium growth conditions at sufficiently low temperatures have to be established. This requires an optimization of the growth parameters to allow sufficiently high C incorporation without excessive degradation of the crystal quality through the undesirable generation of point defects. Also, the surface morphology has to be controlled in order to suppress strain-induced three-dimensional growth.

In the following we report on the progress that has been made in Linz regarding the growth of heterostructures containing ternary $Si_{1-x-y}Ge_xC_y$ alloys. The main emphasis in 1996 has been put on the structural and optical qualities of these layer sequences, which are an essential prerequisite for any further assessment of the future role $Si_{1-x-y}Ge_xC_y$ alloys can play in the field of application-driven band structure engineering.

2. Sample Preparation and Characterization

The ternary $Si_{1-x-y}Ge_xC_y$ alloys were grown in a newly commissioned RIBER SIVA 45 MBE machine equipped with electron beam evaporators for Si, Ge, and C, and dopant effusion cells for Sb (n-type) and B (p-type). High-purity, single crystalline ingots are used for the Si and Ge sources, whereas pyrolytic graphite is used in the carbon evaporator. The fluxes of all three matrix materials are monitored, and feedback-controlled, by a quadrupole mass spectrometer with a cross-beam ion source and PID controllers. The mass spectrometer signals are calibrated by epitaxial growth of $Si_{1-x}Ge_x$ and $Si_{1-y}C_y$ reference layers, the compositions and layer thicknesses of which are determined by x-ray rocking analyses in combination with dynamic simulations. The flux stability, especially of the C source, which is the most critical one because of the small fluxes required, is occasionally checked by quantitative SIMS analysis.

High-resistivity (FZ, $\rho > 1000\ \Omega$cm) Si substrates of 100 mm diameter are chemically precleaned either by oxide removal in 5% HF or by a standard RCA cleaning procedure. Immediately after precleaning the wafers are mounted in 125 mm diameter, all-silicon adapters, a total of six of which can be introduced into the magazine of the load-lock chamber. After pump-down of the load-lock chamber into the 10^{-9} mbar range, the wafers are transferred into the growth chamber, where they are suspended by Mo-clamps underneath a radiative substrate heater made of pyrolytic graphite (PG). Prior to growth, which always commences with a Si buffer layer of 100 to 200 nm thickness, a thermal cleaning step is performed at 900 °C for typically 5 min to remove SiO_2 and possible organic contaminations from the surface. This step can be controlled by in-situ reflec-

tion high energy electron diffraction (RHEED), which reveals a (2x1) reconstruction of the bare Si surface as soon as the amorphous oxide has been flashed off.

The heterostructures are routinely characterized by x-ray diffraction, which yields, as mentioned, in the case of single layers composition and layer thickness. In the case of multiple quantum wells, and superlattices the period length is the primary information derived from rocking measurements. The compositions and the thicknesses of the individual layers can also be extracted by fitting of dynamic simulation curves, however, a certain degree of ambiguity remains. For that reason additional information is useful, such as the composition determined by SIMS analysis, or Rutherford backscattering (RBS). The latter technique is not directly applicable to C, because of the minor backscattering yield from the light elements. Therefore, we are presently trying in collaboration with the University of Padua to exploit a nuclear resonance with broad enough scattering cross section to enhance the back scattering yield to an extent that allows for an absolute, depth resolved evaluation of the carbon content.

For an investigation of the thermal stability of the strained $Si_{1-y}C_y$ layers annealing at temperatures between 500 °C and 900 °C was performed under vacuum either in a furnace or directly in the MBE growth chamber.

Photoluminescence (PL) spectroscopy is a versatile technique, which not only provides information on the band gaps and the band offsets, but is also a sensitive indicator of the overall crystal quality of the layers. This is of special interest for an optimization of the low temperature growth conditions required for the metastable incorporation of carbon, because the PL signal is strongly suppressed, once the density of growth-induced non-radiative recombination centers becomes too high. For our investigations, PL was excited by the 488 nm line of an Ar^+ laser, analyzed in a 0.32 m grating spectrometer and detected by a North Coast Ge detector in a standard lock-in technique. A temperature-variable He cryostat allowed for temperature dependent measurements in the range between 1.6 and 300 K.

3. Experimental Results

Three types of samples were grown for these studies, namely $Si_{1-y}C_y$ single layers, $Si/Si_{1-y}C_y$ multiple quantum wells, and strain compensated $Si/Si_{1-y}C_y/Si_{1-x}Ge_x$ superlattices. In the first two types of samples the band offset is almost exclusively restricted to the conduction band, which is energetically lower in the tensilely strained $Si_{1-y}C_y$ layers due to a strain splitting of the six-fold degenerate, Si-like conduction band. The situation is analogous to strained Si grown on a relaxed $Si_{1-x}Ge_x$ buffer layer and is therefore of special interest for the implementation of n-type MODFETs. Band alignment in the $Si/Si_{1-y}C_y/Si_{1-x}Ge_x$ superlattices, which are interesting for infrared detector applications because of the inherent strain compensation, is more complex: Since the $Si_{1-x}Ge_x$ layers introduce an additional valence band offset, carrier confinement is indirect both in k-space and in real space, with electrons being located in the $Si_{1-y}C_y$ layers and holes in the $Si_{1-x}Ge_x$ layers.

At growth temperatures of around 500 °C the as-grown samples of all three types showed well behaved PL signals. There is presently only one other group worldwide that has published comparable PL spectra from MBE-grown layers [10]. As an example, Fig. 1 shows the spectrum of a ten-period $Si/Si_{0.989}C_{0.011}/Si_{0.9}Ge_{0.1}$ superlattice together with a schematic view of the strain-induced band alignment. Two distinct peaks are observed, which originate from band edge recombination in the vicinity of the $Si_{1-y}C_y$/

$Si_{1-x}Ge_x$ interface, where the wave functions of electrons and holes have finite overlap. The peak at higher energies, labeled SiC-NP, results from the no-phonon transition, whereas the other peak is its TO phonon replica. A NP transition in an indirect gap material is only possible if symmetry breaking mechanisms are present, such as the presence of a heterointerfaces and/or the statistical fluctuations in a random alloy, which is both the case in our layers. The relative strength of the superlattice related peaks can be judged by comparison with the TO replicas originating from the Si layers and from the substrate. Obviously, the quantum wells very efficiently collect electron-hole pairs from the several µm deep excitation volume, and also maintain long enough lifetimes to allow the observation of radiative recombination. The strength of the bandgap PL signal is therefore an important indicator of the crystal quality, since an excessive amount of defects in the layers and at the heterointerfaces associated with non-radiative recombination would quench the PL signal altogether. This is indeed the case, when growth temperatures below 450°C are employed.

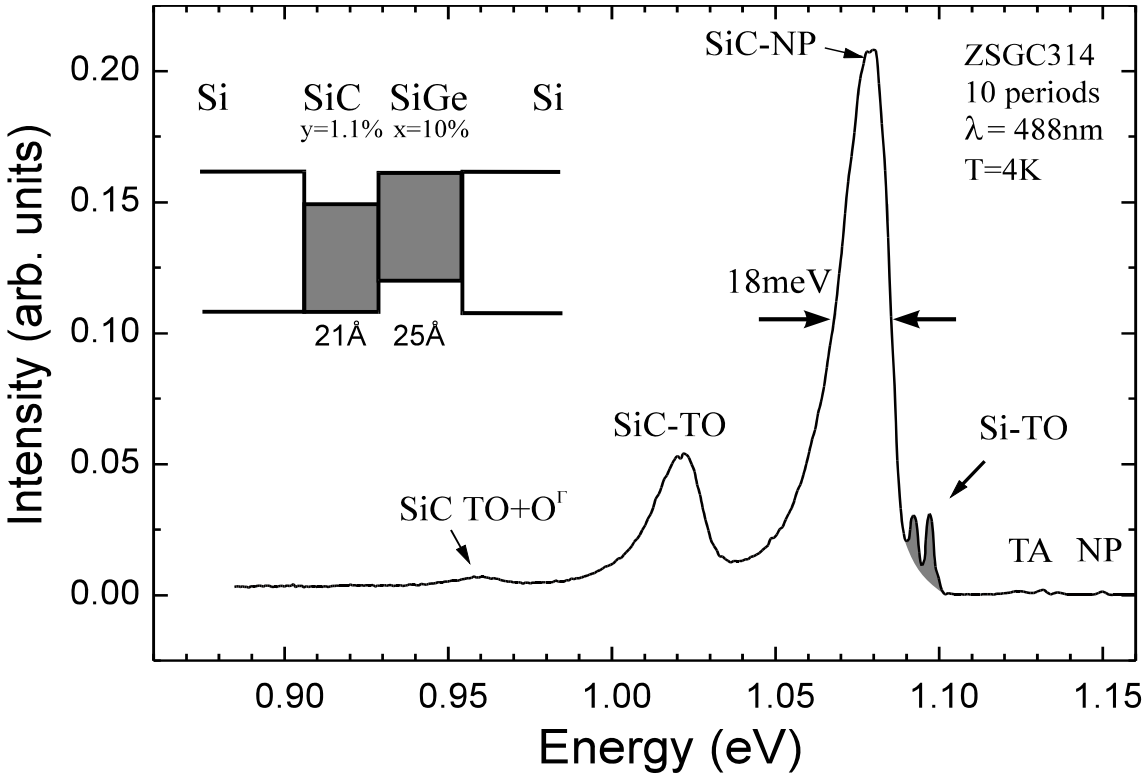

Fig. 1: PL spectrum of a ten-period $Si/Si_{0.989}C_{0.011}/Si_{0.9}Ge_{0.1}$ superlattice. The dominating signals are the no-phonon (NP) band edge recombination from the quantum well section and its TO-phonon replica. The shaded part of the spectrum results from the Si layers and the Si substrate.

Compared to the well established quantum well luminescence from single $Si_{1-x}Ge_x$ layers [11], the PL signal in Fig. 1 is almost a factor of six broader. Since close to a factor of ten higher Ge concentrations are required to induce the same amount of strain that is provided by a given carbon concentration, the statistical fluctuations of both the well width and the well depth are much more pronounced in the case of a $Si_{1-y}C_y$ layer of comparable average strain. In addition possible composition fluctuations from layer to layer may contribute to the line width from a superlattice. For the investigation of

annealing effects we therefore mainly concentrated on single $Si_{1-y}C_y$ layers, which were grown thin enough to remain with the critical thickness limitations, but thick enough to suppress quantum confinement effects. Save for the exciton binding energy, this way the true band gap recombination is measured without any necessity for the correction of confinement energies. In addition, cross checks with the multiple quantum well samples confirmed that the annealing behavior is qualitatively the same.

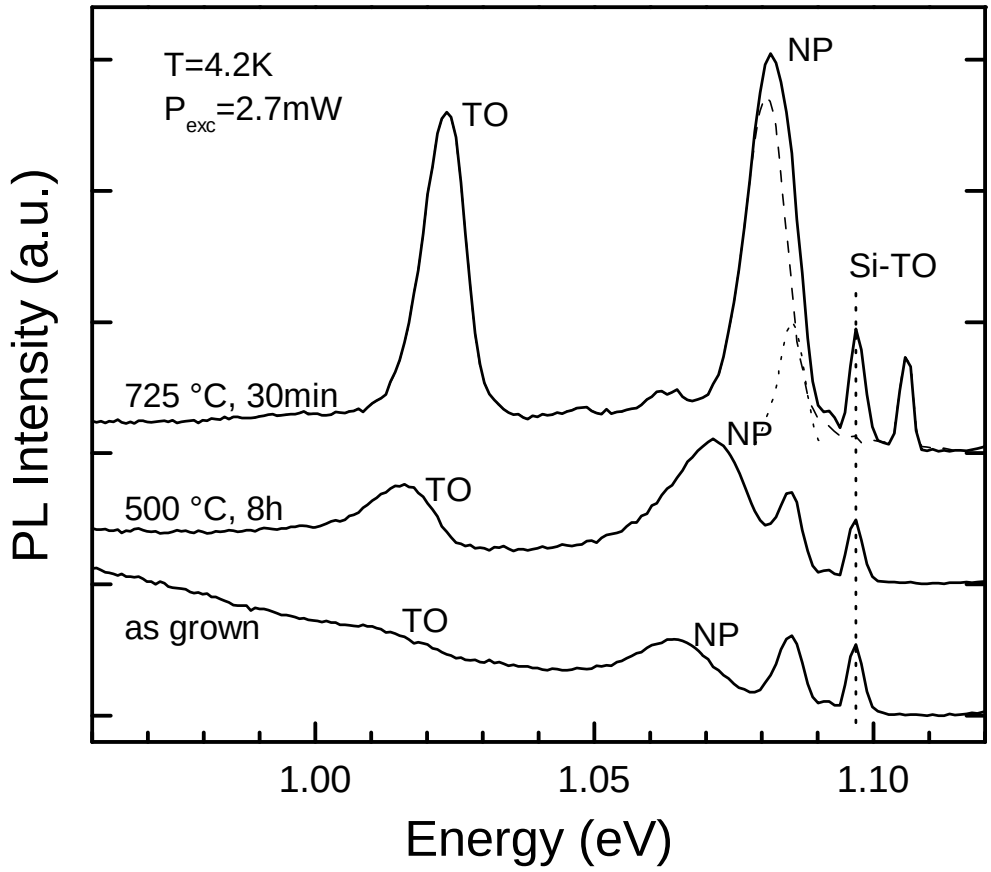

Fig. 2: Evolution of the PL signal of a single $Si_{1-y}C_y$ layer for increasing annealing temperatures. Note the blue shift and the line narrowing.

Figure 2 shows a series of PL measurements from a 100 nm thick $Si_{0.989}C_{0.011}$ layer, which underwent annealing at successively higher temperatures in the range between 500 and 725 °C. There are three main effects associated with annealing: (i) The intensity of the band gap PL signal increases significantly within the range of annealing temperatures shown here. (ii) There is a noticeable *blue shift* of the PL lines amounting to about 15 meV. (iii) The line width after background subtraction becomes much narrower as the annealing temperature is increased. In fact, the linewidth of 8.4 meV in the topmost curve of Fig. 2 is the narrowest observed to date in a $Si_{1-y}C_y$ layer.

Most interesting, the pronounced changes of the PL signal are not associated with a change of the substitutional carbon concentration, as has been checked by x-ray rocking analyses. Only at higher annealing temperatures of >850 °C a loss of substitutional carbon is observed, whereas the PL intensity starts decaying already at about 750 °C.

Since changes of the *average* C concentration can be ruled out, and quantum confinement effects through possible short range diffusion of substitutional carbon can be neglected in the thick layers used here, the development of the PL signal has to have other reasons. To further elucidate these mechanisms, PL measurements of the samples with the highest PL intensity were recorded as a function of the measurement temperature. This is shown in Fig. 3, where the TO-replica of the band gap recombination, which is not affected by spurious signals from the Si substrate, is plotted for measurement temperatures in the range between 4.2 and 20K. The most striking feature of these measurements, which was confirmed by experiments on the quantum well samples, is a *red shift* concomitant with a decay of the intensity as the temperature is increased.

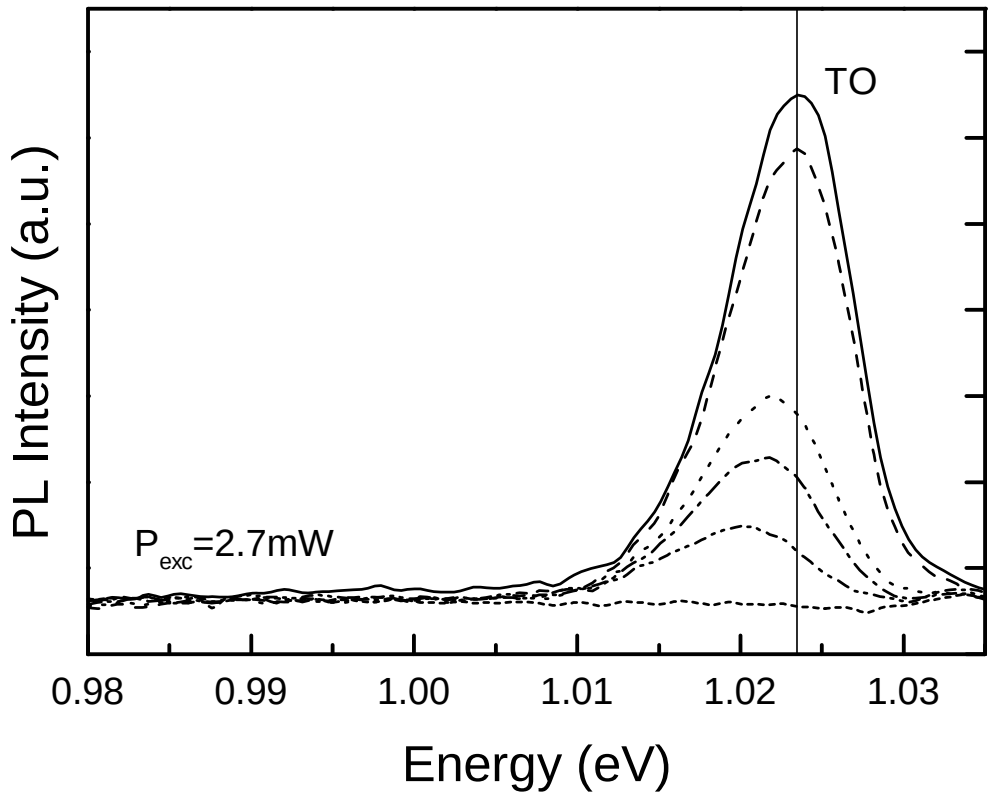

Fig. 3: Red shift of the PL signal with increasing measurement temperature. The TO-phonon replica is plotted here, because it is free of substrate-related signals.

4. Discussion

A consistent interpretation of the annealing effects and of the red shift with higher measurement temperature can be derived, when assuming that the as-grown samples contain non-radiative recombination centers as well as non-statistical fluctuations of the local, substitutional carbon concentration. The latter may be associated with C_2 and C_3 molecules, which are observed in the mass spectrum of the carbon molecular beam, and which are tentatively not completely dissociated at the low growth temperatures employed. Based on these assumptions the following effects will occur during annealing:

(i) At low annealing temperatures (middle curve in Fig. 2, 500 °C for 8 h), non-radiative recombination centers associated with growth defects begin to disappear. This leads to an increase of the PL intensity, but only to a minor decrease of the line width.

(ii) At higher annealing temperatures (upper curve in Fig. 2, 725 °C 30 min) a redistribution of carbon on a local scale occurs, which leads to the dissolution of local carbon accumulations, introduced e.g. by molecular forms of evaporated C. The overall effect is a more homogeneous, statistical distribution of carbon, which causes two effects: First, the PL signal experiences a blue shift, because homogenization of the carbon concentration smears out the local band gap minima in regions of originally enhanced concentration. Second, the line width becomes narrower as the statistical fluctuations become smaller. This interpretation is corroborated by the fact that the ratio between NP signal and TO-replica decreases, which means a reduction of the symmetry-braking alloy fluctuations.

(iii) Although the fluctuations of the carbon concentration become more homogeneous upon annealing, the remaining alloy is still random. This explains the red shift with increasing measurement temperature, which results from carriers bound to alloy fluctuations, as has been observed in $Si_{1.x}Ge_x$, too [12]. With increasing temperature the electrons become mobile and establish an equilibrium distribution that preferentially fills the regions with the smallest band gaps.

(iv) The layers are thermally stable to beyond 850 °C, with no indications for a change of the average concentration of substitutional carbon. Thus noticeable diffusion of carbon or SiC precipitation requires higher temperatures and should not be a severe limitation for device processing.

5. Conclusions and Outlook

We have established MBE growth conditions for high-quality $Si/Si_{1-y}C_y$ and $Si/Si_{1-y}C_y/Si_{1-x}Ge_x$ samples with substitutional carbon concentrations of up to 1.7 %. Well-behaved PL signals from band edge recombination in the $Si_{1-y}C_y$ layers, and at the $Si_{1-y}C_y/Si_{1-x}Ge_x$ interface, respectively, have been observed. The quality of the layers improves significantly upon annealing at moderate temperatures of about 725 °C, without affecting the substitutional carbon concentration. At these temperatures annealing mainly reduces the defect density in the layers and leads to a more homogeneous distribution of substitutional carbon. The layers are thermally stable to beyond 850 °C, where we observe first indications for a reduction of the substitutional carbon content.

Successful growth of carbon-containing, Si-based heterostructures is an important prerequisite for a future implementation of n-type MODFETs with tensilely strained $Si_{1-y}C_y$ quantum wells. In a next step growth conditions have to be adjusted to allow somewhat higher carbon concentrations of about 2 – 2.5 %, which are necessary for the required conduction band offset of 130 to 160 meV. Such layers will allow the fabrication of MODFETs for an assessment of the electronic properties.

Acknowledgments

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Structural Investigations of Phosphorous Doped Silicon Layers

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The structure and surface topography of low-pressure chemical vapor deposited silicon films have been studied using atomic force microscopy. The films were grown on the thermal oxide of a (100) silicon substrate at temperatures between 550 °C and 630 °C. For comparison two different ex-situ doping processes were used: doping from a $POCl_3$ source, and implantation. The measurements have been performed on undoped as-grown as well as on doped and annealed samples. Due to the much lower roughness of the layers amorphously deposited below 570 °C the roughness values of the doped samples are different by more than a factor of ten. Additionally, depending on the initial state of the as-grown layers the grain sizes and their shapes are very different for the doped layers although the annealing parameters are comparable.

1. Introduction

Thin films of conducting polycrystalline silicon prepared by low-pressure chemical vapor deposition (LPCVD) and subsequent doping are very important in the production of integrated circuits. Due to the wide range of their conductivity they are used in a large number of different applications. For instance, heavily doped films are used in the production of gate electrodes and interconnections, and films with high resistivity are used for resistors and floating gates.

Due to the progress in the production of integrated circuits the lateral dimensions of the components continuously decrease. As a consequence the requirement for a better understanding of the detailed properties of polycrystalline silicon layers and their dependence on the production conditions increases. During the last decades a lot of different characterization methods have been developed. All methods have disadvantages in common like a limited lateral resolution, an extensive preparation and a restriction to special surfaces. In contrary, scanning probe microscopy is a powerful tool for real-space surface imaging with high 3D resolution, and needs a minimum of preparation techniques for materials used in the semiconductor device production.

In this work we report on structure and surface roughness investigations of silicon films produced by LPCVD at different temperatures (550 °C – 630 °C) and subsequent doping. The measurements were performed with an atomic force microscope (AFM) operated in contact mode under high vacuum (HV) conditions. The samples have been taken from production-line testwafers, produced by high-volume equipment.

2. Experimental

The measurements have been performed using a UHV AFM with a 5 µm range tube-scanner driving the sample. Samples and tips can be exchanged in HV. Commercially available silicon nitride cantilevers characterized by a 36° interior angle and 20 nm radius of curvature have been used for the contact-mode-AFM measurements. Force calibration for individual cantilevers has been obtained by measuring the bending of the cantilevers as a function of the distance between dip and sample and taking into account the force constant of the cantilevers.

The investigated films have been deposited onto silicon dioxide thermally grown on (100) n-type silicon wafers. The deposition temperature for different samples was changed from 550 °C up to 630 °C in steps of 10 °C. The thickness of the as-deposited layers was between 250 and 270 nm. The ex-situ phosphorous doping was produced in two different ways: a) by a gaseous predeposition using a $POCl_3$ source at 900 °C, followed by a drive-in step at the same temperature and the deglazing in a buffered oxide etch (BOE), and b) by implantation of phosphorous and subsequent annealing of the films at 900 °C. Doping by implantation was applied to films grown at deposition temperatures below 600 °C only.

Prior to the scanning probe measurements an additional selective silicon dioxide etching has been applied to all samples by dipping them in 2% hydrofluoric acid (HF). This procedure is well known to produce surface passivation by H-termination of silicon dangling bonds. Immediately after etching, the samples have been mounted in the AFM chamber and were measured at high vacuum conditions at a residual gas pressure $< 2\times10^{-7}$ mbar. A comparison of HF-treated and untreated samples have shown that the HF passivation of the surface changes neither the topographic nor the grain structure of the samples [1].

The measurements have been performed with constant normal forces as low as 0.05 nN (normal forces below 1 nN only in vacuum) and ranging up to 10 nN. The roughness values discussed below have been evaluated from contact-mode AFM measurements. In order to exclude effects due to different tip qualities, all samples have been investigated using the same type of cantilevers and a low normal force of 0.1 nN. Additionally, for the comparison of the tip quality the first measurements of each tip have been done on a sample with narrow trenches. Previous measurements had shown that in high vacuum and for normal forces below 1 nN no degradation effects of the tips and the silicon surfaces are observable for more than 200 scans.

Areas have been chosen randomly on each sample. Samples taken from different areas of the wafer show no significant difference in structure and topography of the surface. At least 10 images of 1x1 μm^2 have been acquired on each sample. Roughness values have been calculated from each image using standard software, which fits a plane to the entire image, determines the deviation of each image point from this plane, and calculates the root-mean-square value R_{rms}. The roughness values for each layer have been obtained by averaging measurements of at least five areas.

3. Results

Previous measurements on as grown films [2] have shown that films grown at deposition temperatures below 570 °C are amorphous. Films grown above 600 °C are polycrystalline, and the hillocks were identified as the grains of the layer [3]. For deposition

temperatures from 570 °C to 600 °C an amorphous matrix with an increasing number of embedded crystallites occurs. The roughness values of the amorphous films are below 1 nm and more than one order of magnitude smaller than those of the polycrystalline films (10 - 15 nm).

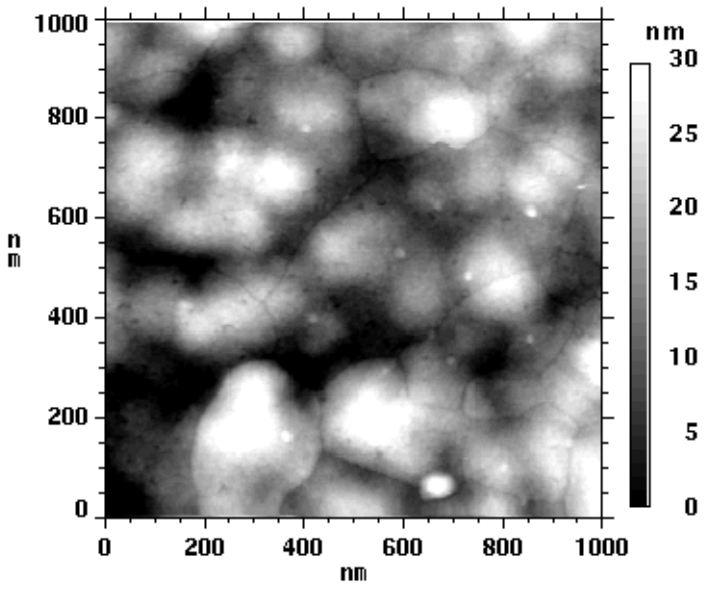

Fig. 1: Contact-mode-AFM topographic image of a doped polycrystalline silicon film grown at 620 °C.

A conventional topographic image of a doped silicon film grown at 620 °C is shown in Fig. 1. The image is dominated by a hillock structure with lateral features between 70 and 200 nm and is characteristic for all films grown at temperatures higher than 600 °C. A comparison of the topographies of doped and as-grown films show only slightly enlarged and flattened hillocks for the doped films with roughness values between 7 and 12 nm. In contrary to the as-grown films the hillocks of the doped samples can no longer be identified with the grains shown in Fig. 2. In this image the topographic data have been differentiated and convoluted to enhance short-scale corrugation. This way a well defined grain structure clearly becomes observable and resembles earlier TEM micrographs of similarly processed samples reported by Wada et al. [4]. Typical lateral dimensions of the grains are 350 nm, but ranging up to 500 nm.

Fig. 3 shows the topography of a doped silicon film grown at 560 °C. Due to the very low roughness values of the films grown below 570 °C the boundaries of the grains can be observed directly in the topography without differentiation. Fig. 3 is characteristic for all samples grown below 570 °C and both kinds of doping processes. The grains partially exhibit unusual elongated shapes with angles at the corners deviating strongly from 120°. Their lateral dimension ranges up to above 1000 nm. The roughness values for these films are between 1 and 2 nm.

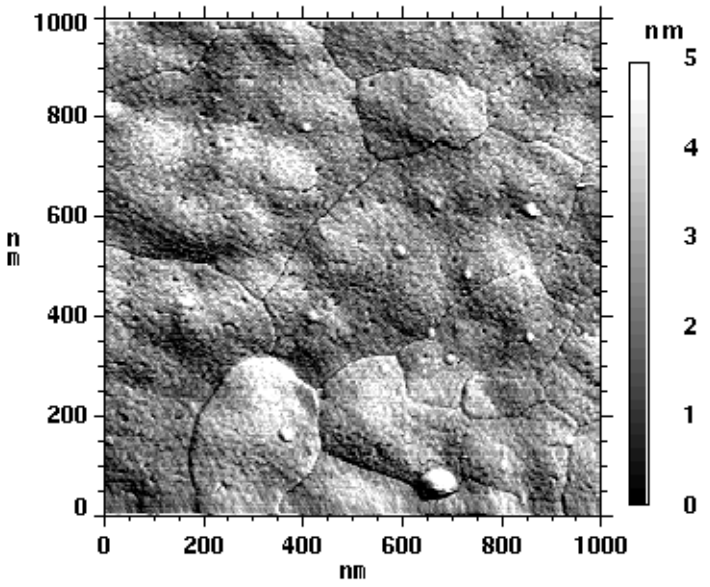

Fig. 2: Differentiated and convoluted image of Fig. 1, showing grain boundaries.

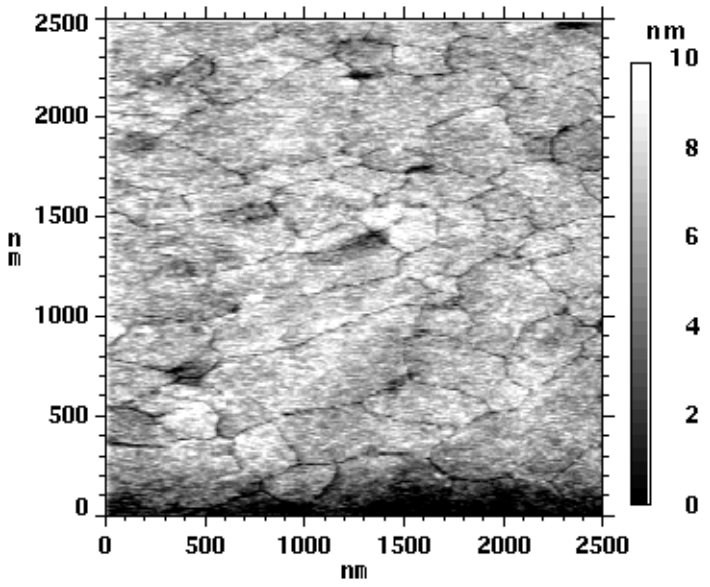

Fig. 3: Contact-mode-AFM topographic image of a doped polycrystalline silicon film grown at 560 °C.

4. Conclusion

The AFM techniques applied in this work have proven to be a powerful tool for the characterization of silicon layers taken out of the production line of the integrated circuit production. Particularly, for the first time it has been possible to distinguish between topographic hillocks and the grain structure of polycrystalline silicon films using only one characterization technique.

We have investigated undoped and doped films grown in a temperature range between 550 °C and 630 °C. The roughness values for the amorphous films grown below 570 °C are by more than a factor of ten smaller than those of the polycrystalline grown films above 600 °C. The doping and subsequent annealing at temperatures around 900 °C causes a complete recrystallization of the layers. Therefore the amorphous films become polycrystalline and the size of the grains of initially polycrystalline films increases. In contrary to this change in the structure of the films the topography of the films is only slightly modified. Consequently the roughness values do not change drastically due to the doping process.

In addition we have shown that the grain structures of initially amorphous and polycrystalline films are very different after the doping process although temperature and duration of the annealing processes are comparable. Doped films grown below 570 °C show partially unusual shapes of their grains with lateral dimensions in a wide range up to above 1000 nm. In contrast to this result doped films grown above 600 °C exhibit more regular shapes of their grains with lateral dimensions in a small range around 400 nm.

The reason for the different recrystallization behaviors is not completely understood. Due to the importance of homogeneous and flat polycrystalline silicon films for the production of integrated circuits with very large scale integration this behavior should be investigated in further experiments.

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Laser-Induced Deposition and Etching of Tungsten Microstructures

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Micron-sized deposition and etching of W in WF_6 + H_2 atmosphere is investigated by local laser-induced heating of thin tungsten layers on quartz substrates. The process is strongly dependent on the partial pressures of the two gases. A process with high amount of hydrogen permits deposition of W, whereas etching of W occurs if the working gas does not contain hydrogen.

1. Introduction

Tungsten is an attractive material for use in microelectronics, because of its refractory nature, relatively low resistivity, high melting point, low thermal expansion coefficient, and high chemical inertness. Both blanket and selective deposition of W is applied in the VLSI technology [1], [2]. Micron sized structures of tungsten can be generated with focused ion beams [3]. But also lithographic patterning of W using RIE is widely implemented for submicron manufacturing [4], [5].

Laser chemical processing is a method for fast single-step modification and patterning of solid surfaces with dimensions down into the submicrometer range. Laser-induced chemical vapor deposition (LCVD) allows localized growth and direct writing of structures with specified materials [6]. The process can be employed for fast 3D processing of non-planar substrates and for fabrication of free standing 3D micron sized devices [7].

For tungsten deposition, WF_6 is a standard precursor. The frequently used Si reduction process allows selective deposition, whereas hydrogen reduction of WF_6 provides high deposition rates [1]. This latter thermal process shows a number of interesting phenomena which can be visualized on SiO_2 substrates covered with a thin W layer of well defined thickness.

2. Experimental

2.1. Production of Tungsten Films

Tungsten films have been fabricated by using the Perkin Elmer 4400 sputtering system at the *Institut für Allgemeine Elektrotechnik und Elektronik*, Technical University of Vienna. The most important technical details are as follows: 8” magnetron cathode; purity of the target material (tungsten) 99,97%; rf-sputtering with 13.57 Megahertz;

sputter power 800W; substrate palette rotation mode; substrate bias 20V; deposition without using a substrate heater; quartz substrates freely lying on a glass support; substrates ultrasonically cleaned with propanol and further cleaned in the sputtering chamber by sputter etching (300 W, 15 min) immediately prior to the deposition of a tungsten film; purity of the sputter gas (argon) 99.9999%; argon pressure $5x10^{-3}$ Torr ($6.7x10^{-3}$ mbar), film thickness 850 Ångström, sputter time 16 minutes; waiting time prior to taking out the substrates of the vacuum chamber 30 minutes.

Film thickness measurements have been carried out with a Tencor Alpha Step 200 instrument. The film steps necessary for these measurements have been fabricated on test substrates by applying the well known photoresist float-off technique. These test samples are placed quite close to the quartz substrates during film deposition.

Mechanical stress in the film has been controlled by detecting the curvature of very thin glass plates (24 x 24 x 0.15 mm) which are also coated simultaneously with the quartz substrates. The sputter parameters have been carefully chosen in such a way that the internal mechanical stress is minimized (very small compressive stress, definitely no tensile stress).

2.2. Deposition/Etching Experiments

The experimental setup employed is similar to that described in [8], [9]. The high reactivity of WF_6 requires the reaction chamber and feed pipes to be fabricated out of stainless steel. Only a few Viton seals have been used. The system was flooded with argon and heated out to temperatures between 150°C and 400°C. The W-covered SiO_2 substrates were rinsed in aqueous KOH, acetone and methanol, and baked out before mounting.

The WF_6 gas employed (Fluka-Chemie) had a purity of 99.56% with tungsten oxyfluorides (< 0.4%), CF_4 (< 0.025%), HF (< 0.01%) and SF_6 (< 0.01%) as main contaminants. The flow rate (15 sccm) of gases was controlled by needle valves and flowmeters.

The Ar^+-laser beam was focused onto the substrate at perpendicular incidence ($\lambda \approx 515$ nm, $2w_0$ (1/e) ≈ 2.1µm). Laser pulses with variable duration were generated by means of a Pockels cell.

Patterning was performed by moving the substrate with respect to the laser beam. The whole process was observed via a TV camera in combination with a lens system. The geometry and morphology of patterns were investigated by a scanning electron microscope (SEM).

3. Results and discussion

3.1. Single Dots

With both the substrate and the laser beam fixed, the deposition/etch pattern has circular symmetry. Figure 1 shows SEM pictures and corresponding sketches of patterns observed with various partial pressures of gases.

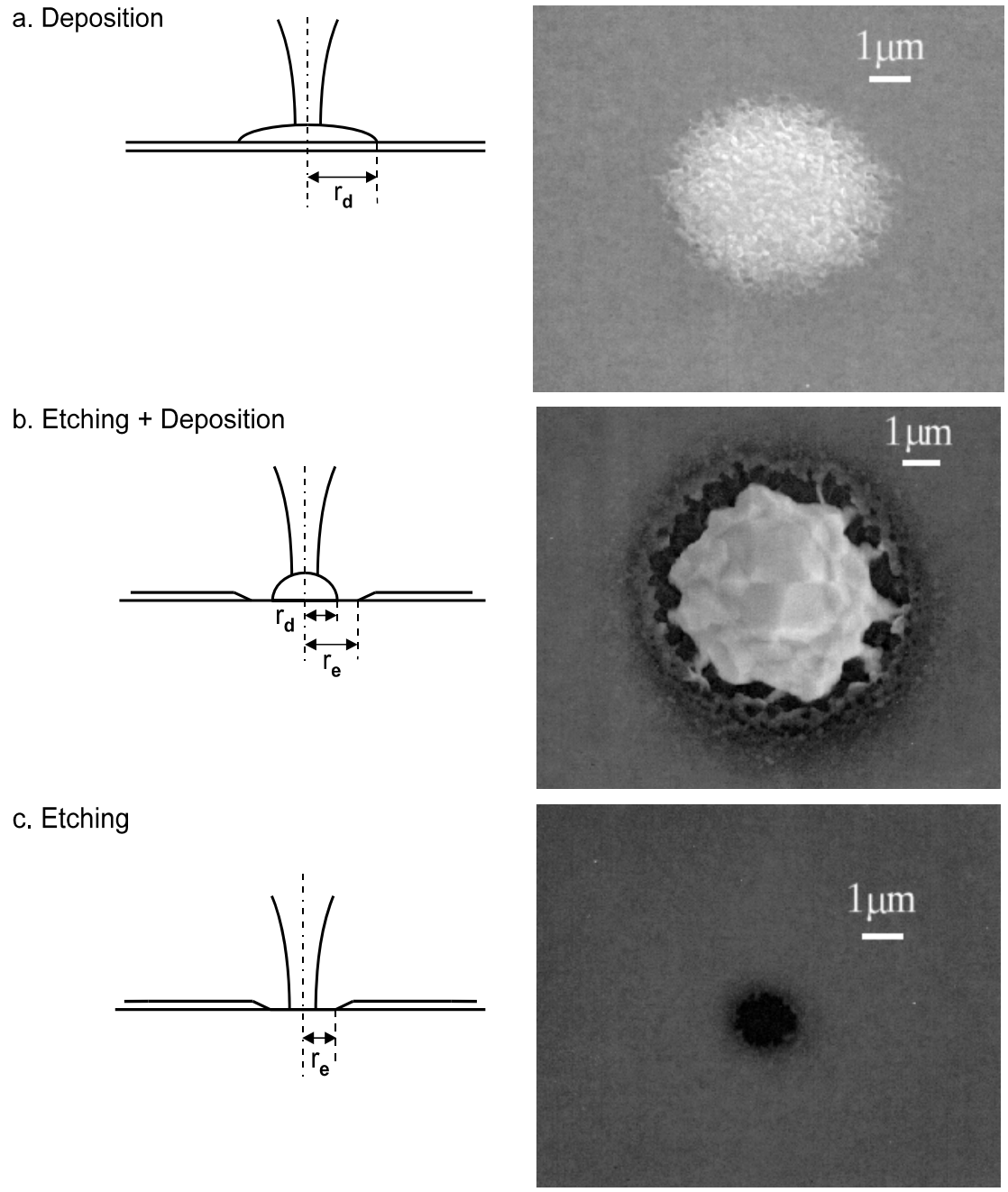

Fig. 1: Schematic illustrations and SEM pictures of the different types of processes occurring with different values of Γ_P. a) p_{WF_6} = 1 mbar, Γ_P = 5, incident laser power P_{inc} = 160 mW, b) p_{WF_6} = 2 mbar Γ_P = 0.25, P_{inc} = 160 mW, c) p_{WF_6} = 2 mbar, Γ_P = 0, P_{inc} = 96 mW.

With pressure ratios $\Gamma_P \equiv p_{H_2}/p_{WF_6} \geq 1$ we observe deposition without any indication for etching (in standard CVD [1] pressure ratios $\Gamma_P >> 1$ are employed). Figure 1a shows W dots deposited with p_{H_2} = 5 mbar and p_{WF_6} = 1 mbar. Here the overall deposition reaction is

$$WF_6 + 3\,H_2 \rightarrow W(s) + 6\,HF. \qquad (1)$$

The morphology of deposits is similar to that described in [6].

The situation changes significantly with decreasing Γ_P. Figure 1b shows the pattern observed with p_{H_2} = 0.5 mbar and p_{WF_6} = 2 mbar. The deposit within the center is now surrounded by a circular ring of (outer) radius r_e . Within this ring, i.e. within the area $r_d \leq r \leq r_e$, the W film is etched. The process can be described by [8], [9], [10]

$$W(s) + 5\ WF_6 \rightleftarrows 6\ WF_5\ . \qquad (2)$$

With decreasing Γ_P, the diameter of both the deposit and etched ring decreases. In the absence of hydrogen ($\Gamma_P = 0$), only etching is observed (Fig. 1c).

At the laser wavelength used both the deposition and the etching process are thermally activated, i.e. they obey to Arrhenius laws with certain activation energies ΔE_d and ΔE_e, respectively. Due to the nonlinearity of both the deposition and the etching process structures with lateral dimensions less than the focal width of the laser beam are possible. The nonlinear characteristics of the process provide also the possibility to etch through the W layer totally, i.e. with no metal remaining within the etch hole. This is possible because if $r_e < w_0$, enough laser radiation will be absorbed at the borders of the etch hole even when the hole is etched through, and thereby the temperature is kept high enough to maintain the etching process. It should be noted here that the etching process proceeds efficiently even at very moderate temperatures, i.e. at p_{WF_6} = 2 mbar and T ≈ 500 K the etch rate is ≈ 100 Å/s. At high process temperatures additional removal of the SiO_2 substrate is observed. Because high temperatures are localized to a narrow area around the laser-beam center, this possible "etching" effect is of small lateral size [10].

The overall process has been analyzed in detail by thermodynamic calculations and by modeling of etching/growth based on the accurate calculation of laser-induced temperature distributions [11].

3.2. Direct writing

Deposition of tungsten lines by direct writing has been widely investigated [6]. Nevertheless, the possibility of writing W lines on optically transparent SiO_2 substrates should be mentioned. Starting the deposition on an absorbing medium, when passing onto SiO_2, the thermally activated deposition process is maintained due to the fact that the laser radiation is partly absorbed by the already deposited stripe. Similar as in the case of etching, this absorbed power keeps the temperature high enough for further deposition to occur. But continuous and homogeneous patterns are only possible in narrow parameter regimes. Figure 2 shows SEM pictures of a stripe written on SiO_2.

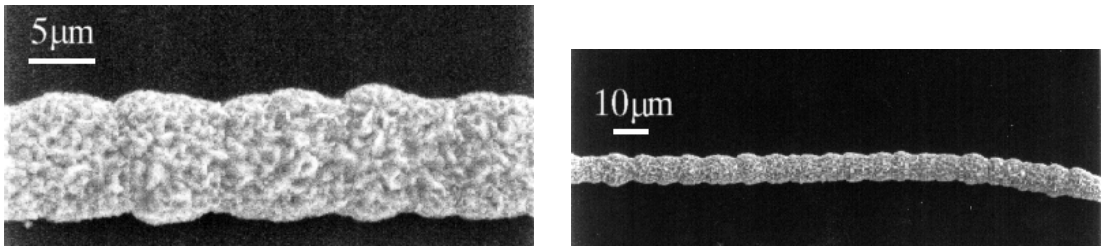

Fig. 2: SEM pictures with different magnifications showing a W-line "written" on SiO_2 (thermal induction by self-absorption of laser radiation), p_{WF_6} = 1 mbar, Γ_P = 2, P_{inc} =140 mW. Scanning velocity v_S = 10 μm/s.

With $\Gamma_P = 0$ the direct writing of etch patterns in the thin W-layer is possible. Figure 3 shows SEM pictures of lines etched at two different scanning velocities v_s.

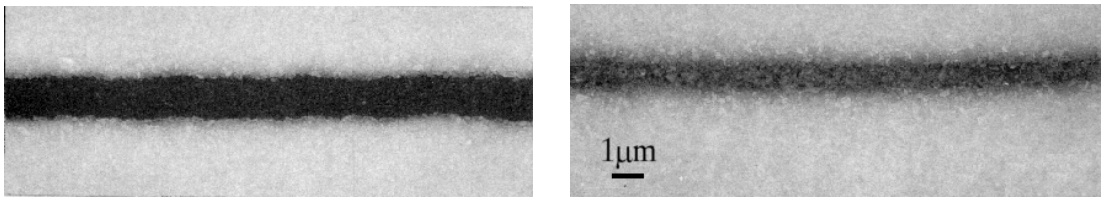

Fig. 3: SEM pictures showing etch lines directly "written" within the W-layer at different scanning velocities. p_{WF_6} = 2 mbar, P_{inc} = 96 mW.
Left: v_S = 4.2 µm/s, right: v_S = 42 µm/s.

With increasing scan speed the complete etching is possible due to an increase in processing temperature. The necessary increase in absorbed laser power occurs due to the flattening of the front groove angle of the etch line [12]. Total etching of the layer is possible below a parameter dependent value of v_S.

4. Conclusion

Laser-induced deposition/etching of W in $WF_6 + H_2$ atmosphere has been investigated. With pressure ratios $\Gamma_P = p_{H_2}/p_{WF_6} > 1$ we observe only deposition, while with $\Gamma_P \leq 1$ deposition *and* etching takes place simultaneously. With $\Gamma_P = 0$ the net reaction results in pure etching.

Concerning the conditions $\Gamma_P > 1$ and $\Gamma_P = 0$ an application as a single step writing/erasing tool of W structures by adding/removing of H_2 in a defined passivated system is possible.

Acknowledgments

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UNICHIP Vienna, a Technology Transfer Center for ASIC Design

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After a short description of the SME oriented work of UNICHIP a design of an analogue ASIC is presented. This project has been undertaken in close cooperation with and Austrian SME (Frequentis-Nachrichtentechnik) It serves perfectly well as an successful example of technology transfer of ASIC design and know-how.

1. Introduction

From its very beginning the work of the UNICHIP Wien design team was targeted towards technology transfer of ASIC design knowledge mainly to Austrian SMEs. Various measures were taken to achieve this goal. Firstly the undergraduate education of VLSI design methodologies has been intensified. Recently interesting diploma-theses have been completed such as a "Re-targetable VHDL-module for an SCSI-Controller" or "CULT – A new class of scaleable benchmark circuits for FPGAs".

For training and education focused directly towards SMEs we use various different approaches. Apart from front-end design courses which are held together with the University Extension Center, in-house training and consulting activities lasting between one and three days each have proved to be very successful. In the last two years more than 15 firms accepted this offer. Finally, projects performed in close cooperation with a partner from industry are by far the most effective way of technology transfer. In the remaining part of this report we shall describe such a transfer project.

2. Analog Headset Transceiver: A Technology Transfer Project

Together with Frequentis, an Austrian SME dealing with speech communication systems for air traffic control, an analogue headset transceiver ASIC was developed. Instead of focusing on design based training of Frequentis engineers, the authors tried to transfer knowledge on how to manage analogue IC design projects and to specify circuits to be developed and fabricated by sub-contractors. The cooperation started with a short product analysis study lasting no more than four weeks. As a result of this preliminary work, four areas suitable for replacing standard solutions with ASICs were spotted, one analogue and three digital designs of varying complexity. It was agreed to realize the analogue ASIC, this one being the most urgent.

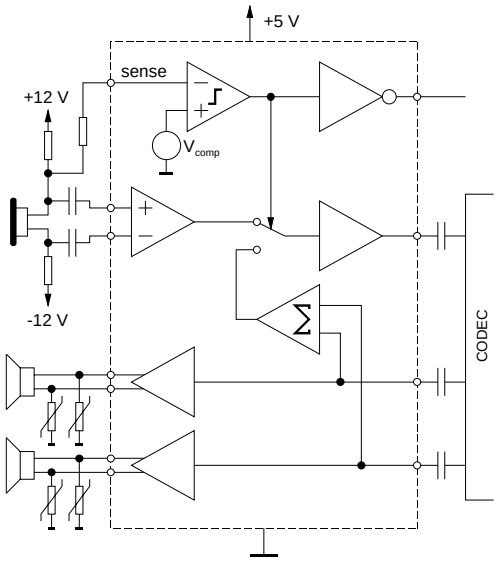
[1] Member IEEE

The headset transceiver (HST) is basically the interface between the communication system and the air traffic controllers. Since each working place in a typical system has three sockets to which headsets can be connected, the first benefit expected from an integrated solution is a significant reduction of space on the printed circuit boards needed for the interfaces. Another advantage is the increased reliability. The third and somehow unusual benefit is a standardization aspect. Speech communication systems are unique solutions, and so far, despite a modular design of the digital parts of the system, the interface boards have been developed anew for each customer. An ASIC, however, is a fixed starting point for future designs and may thus help reduce also development costs.

2.1. Function of the HST

The basic function of the ASIC is the amplification and conditioning of the voice-band signals that come in from the headset's microphone or are applied to the earphones, respectively. In addition, the presence of a headset must be detected. If no headset, or more precisely, no microphone, is attached to the module, then a loop-back function is to be activated such that the speaker hears his own voice, signaling him that his partner does no longer exist. This function is also useful for testing purposes because the complete signal path through the system — including the CODECs and most of the analogue amplifiers — may be monitored.

Figure 1 shows a block diagram of one channel of the HST together with the specifications. The ASIC actually comprises two of them. Since there is only a single supply voltage available, the drivers for the loudspeakers need differential outputs to meet the specifications. To be independent of the dc levels of the signals generated by the CODEC, capacitive coupling is used. Thus the internal reference potential could be set to its optimum value, which is derived from the supply with a simple resistive divider. An optional external capacitor connected to the divider improves the PSRR, and this analogue ground is carefully buffered to minimize crosstalk between the signals.



Power supply voltage	+5 V
Loudspeaker driver	
Output power	10 mW_{eff}
Load Impedance	150-600 Ω, 0,5-3 nF
Voltage gain	20 dB
Microphone amplifier	
Load impedance	20 kΩ, 15 pF
Voltage gain	0 dB
Summing amplifier	
Voltage gain	-20 dB
Harmonic distortion	< 1 %

Fig. 1: Block diagram of HST together with electrical specifications.

Like all circuits in air traffic control applications, the whole system must comply with IEC 801-2-91, which requires the circuitry to withstand ESD pulses of 8 kV applied to its ports. Therefore all connections to the headset are protected by additional transient voltage absorbers. Unfortunately, these devices impose a significant capacitive load on the output drivers of the HST. Another important requirement is that for reliability reasons the drivers must survive shorts between the output terminals as well as between the outputs and ground (a typical cause of such a short is a mechanical damage of the headset cable).

2.2. The Course of the Project

As a first step a three months' study was launched with the objective to evaluate the feasibility of this design from technical and economical points of view. As a result the following items could be delivered: an area estimation, design effort, possible ASIC manufacturers. It could be foreseen that the headset transceiver ASIC would be the only analogue integrated design effort for Frequentis for the next few years. Thus acquiring knowledge of the necessary design skills (CMOS amplifier design, analogue simulation, and analogue IC layout) would be of no use for the design engineers.

On the contrary, it turned out that correct (e.g. error free and complete) specification of integrated circuits to be designed by sub-contractors was the main knowledge for Frequentis to be gained from this collaboration. So far they had underestimated the constraints imposed by an ASIC design on internal project schedules. The design project was refined and launched. The very first task was the preparation of a detailed specification. This was done in close cooperation with design engineers of Frequentis who were used to working with discrete operational amplifiers. After the ASIC had been specified to a certain extent, the design work started.

The Mietec 2.0 µm CMOS process offered via EUROCHIP was selected for two good reasons. Firstly, there was an MPW run scheduled for mid-May, which perfectly fitted into the project timetable. Secondly, the process offered a wide range of supply voltages, which in turn was convenient for the designers at Frequentis in that they needed not specify critical design parameters like the required output power once and for all. If for example in later applications a higher output voltage swing was needed, the supply voltage could readily be increased to meet the changed requirements. Yet the primary goal was to use the 5 V supply already available in the system.

A few days before the submission to EUROCHIP, someone noticed that the external protection devices at the loudspeaker outputs had a huge parasitic capacitance, whereas all the time before a purely ohmic load had been assumed. This mistake stemmed from a simple misunderstanding. Our partners had thoroughly analyzed all headsets they used in their systems, but nobody had ever taken the true environment of the HST into account. As the designers were not familiar with analogue IC design, they did not know that 3 nF already mean a large capacitive load for a CMOS op-amp, and thus the protection devices had been neglected.

The fabrication phase of the prototypes unfortunately coincided with the summer holidays, and the ICs spent several weeks in different European countries waiting to be processed, packaged, or delivered to the customer. This was bad fortune indeed and no one had taken such a delay into consideration before, but when Frequentis eventually received the silicon, we were five weeks behind schedule.

In the meantime, the complete schedule had changed in that now a deadline for the availability of functioning prototypes in January had been set up. Although the problems with the first design had been spotted and the specification had reached a stable state, a second prototyping run via EUROCHIP with its eleven weeks turnaround time seemed impossible. The tight schedule and the fact that due to the unforeseen fabrication delay, Frequentis had partly lost their confidence in the EUROCHIP MPW services, led us to seek a purely commercial solution. For the new version, we selected AMS as manufacturer mostly because they are reachable from Vienna within two hours by car. The entire re-design on a 1.2 µm N-well process providing high ohmic poly (which had not been available in the processes offered via EUROCHIP) was then completed within two weeks. By the end of January 1997, Frequentis received the fully functioning engineering samples.

2.3. Implementation Details

While in the first version the chip size was about 8 mm², the final circuit after the redesign required only 4.7 mm². In the left and right columns of the core, one can see the amplifiers for the loudspeakers. Figure 2 shows the layout of the HST ASIC. The feedback resistors have been placed in the pad ring. The low-noise microphone amplifiers occupy the top and bottom of the middle column in close proximity of the respective IO-pads. In the center of the core the summing amplifiers and the analogue ground buffer are located.

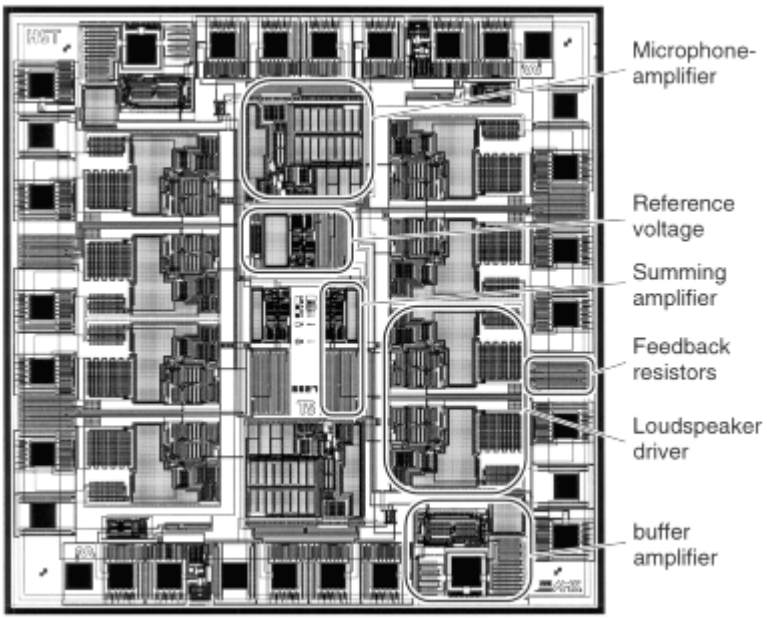


Fig. 2: Layout of the HST ASIC.

2.4. Conclusion

The development of an analogue ASIC helped the company to reduce the system costs, increase the reliability by implementing additional monitoring functions, and to a certain extent standardize their products. Prototyping services like those provided by EUROPRACTICE proved to be very valuable, their cost-effectiveness being an essen-

tial argument in easing the decision of an SME towards the use of new technologies. On the other hand, comparatively long turnaround times acceptable for universities may irritate industrial partners, and the consequences on project schedules have to be pointed out from the very beginning. In this sense both partners gained experience in managing projects including MPW prototyping.

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ASICs in Electronic Instrumentation

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Application Specific Integrated Circuits (ASICs) are used for various reasons in electronic instrumentation. The most significant advantages in industrial environment are obviously less power consumption and less space combined with a good possibility of signal conditioning for proper information transfer to a central processing unit. In laboratory equipment reliability and flexibility as well as the reduction of cost and space are the counting arguments for the use of ASICs. This paper will give a review on projects already worked out at the Department of Electronics and will then — as the annual report of UNICHIP Graz — focus on an ASIC devoted to highly accurate thermometric instrumentation.

1. Introduction

The Department of Electronics at the Technical University Graz started to design integrated circuits (IC) in 1988. Since then several systems have been developed in the department comprising ASICs devoted to electronic instrumentation. The methodology involved spans from gate-array to standard-cells if digital; in case of analog or mixed-mode the analog section is full-custom.

The systems under consideration are predominantly sensoric sensing physical properties of liquids (density, velocity of sound, and temperature) either in the harsh environment of industrial process control or in the clean laboratory with the highest level of accuracy.

2. Instrumentation in Industrial Environment

There are various reasons for the use of ASICs in electronic instruments for industrial environment. Our systems being in almost all cases instrumentation designed to support sensors the small size of the ASIC is very much appreciated as such systems fit directly into the probes. The small outline helps with respect to electromagnetic interference and to mechanical robustness. If power consumption is low the system can be supplied with a current loop (typically 4 – 20 mA), which is also used to carry information to the central processing unit. Both requirements (small, low power consumption) can be met with ASICs. Three ASICs of this kind have been developed at the department in the last years. They are briefly described in the following chapters.

2.1. GOETHE

This was the very first gate-array design [1] in the field of industrial instrumentation at our department. It was thought to replace a PCB system which was used to encode the temperature of a liquid into a bit-stream locked in frequency to the periodic signal coming from a mechanical oscillator carrying information on the density of said liquid.

In other words, the temperature was measured using a platinum thermometer and a reference resistor in an integrating ratiometric Analog-to-Digital Converter (ADC). As the clock for the ADC was the mechanical oscillator, the resolution in temperature with respect to time was by far to low.

The ASIC (GOETHE) had an on-chip crystal oscillator to provide a fast clock signal for the ADCs. The control- and the quantization units for two of them were integrated in the gate-array. The resolution is 20 bit each. The analog sections of these ADCs are added off-chip. The results of the conversions are counted BCD numbers. They modulated the pulse width of the mechanical oscillator signal. The information was transferred by means of a binary current signal on a two-wire line also providing the power for the whole sensor system.

This ASIC brought the expected increase in performance and a significant decrease in space needed for the interface system.

2.2. ASTERIX

This ASIC was the first standard cell design at our department. It is used in a warm water boiler to periodically “wake up” a microcontroller which then takes measurements of temperatures and performs calculations on whether there is enough energy stored or not. The results are sent back to the ASIC which offers a multiplexed LCD driver circuit. The display shows status information.

The main advantage of this ASIC was an enormous reduction in the power needed to operate the control system as only a very small part was active all the time and the power consuming parts were activated for just a short period. With the multiplexed LCD driver in the ASIC a reduction of the package to a 28 pin type could be achieved. This saves extra cost for the PCB and the ASIC.

The development of ASTERIX was a cooperation of an Austrian enterprise, Joanneum Research and our department. ASTERIX is part of a product of this Austrian enterprise.

2.3. SUPERGOETHE

This ASIC is a more powerful version of GOETHE. Therefore a standard-cell approach was chosen in a 1.0 µm CMOS technology [2], [3]. The system was extended to be able to operate the analog sections of three 20-bit ADCs and to quantize up to three periodic signals (both density and velocity of sound are transferred to periodic electrical signals; the information is the length of the period) with selectable resolution. The problem with this quantization is the absolute accuracy, the long time- and the temperature stability of the crystal oscillator in the interface. To avoid this problem a method of counting multiple periods with no error and determining the length of these periods by counting a high frequency oscillator clock is used. If the rate for the information transfer and the oscillator clock have a fixed ratio the clock period can be measured in the central processing unit, where power consumption is no severe problem and therefore accurate and stable oscillators (e.g. heated crystal) can be used as reference. The time for the measurement is one second. The information gathered in this time is transferred in the following second. The supply current is periodically switched between two values. The information is encoded in the duty-cycle of this signal.

This ASIC is very flexible. It can be configured to many operational modes. It is used in two products so far. One is a two channel traceable thermometer with an accuracy of

0.01 °C. The second product is a modular sensor interface system for measuring density, temperature, pressure, and velocity of sound in industrial environment. This system is certified to be intrinsically safe.

2.4. Preworks on an ASIC for the Measurement of the Velocity of Sound

One method for measuring the velocity of sound in liquids is to determine the transit time for a known distance between the sender and the receiver of an ultrasonic pulse. This is done in electronic circuits on PCB level very well [4]. Some research activity was spent to find a way of integrating such a system on a single chip. Various input amplifiers have been designed but are not yet fully evaluated.

3. Instrumentation in Laboratory Equipment

To save space on the PCB and to increase reliability and functionality ASICs are put in electronic instruments for laboratories. Power consumption is normally no problem in this case except when the instrument is battery powered. Then of course this is a driving argument for the use of an ASIC. Two ASICs are presented here which were designed the years ago. Chapter 4 then covers a recently developed circuit in more detail.

3.1. ADONIS

Laboratory equipment often uses electromechanical components (pumps, transformers) which are dependent on the mains frequency. To eliminate the need of a switch to adapt the instrument to the right frequency these AC signals are often synthesized. A crystal oscillator is used together with H-bridge power switches to do this synthesis from a DC voltage. An ASIC (ADONIS) was developed using gate-array technology to get a 50 Hz and a 100 Hz signal to drive a transformer and a pump in a density meter [5]. All control signals for the power switches are generated in the ASIC. Overload switch-off and power-on-reset are available. The driving output signals can be turned on and off separately.

3.2. ENDOR

To minimize size and power consumption of a handheld battery powered density meter an ASIC (ENDOR) was designed [6]. It has a 8051-compatible microcontroller interface and consists of some glue logic, a unit to quantize and encode a Charge-Balance ADC and to measure the period of a signal. This signal comes from a mechanical oscillator, which is electrically brought to its resonance frequency. The period of this signal is used to calculate the density of the liquid. The ASIC works according to the specifications.

4. ENDEAVOR - An ASIC for a Highly Accurate Thermometer

As a result of the activities in research and development at the department a highly accurate thermometer was built [7], [8]. The accuracy is 0.001 K in the range from -200 °C to +800 °C. The thermometer offers two channels for measurement.

It uses a platinum resistor for sensing as this is the only type of temperature sensor with respect to this wide temperature range and this high accuracy [9]. The thermometer

consists of two current sources, a voltage-to-current converter and of an ADC working in current mode. There is also a microcomputer to select the channel, to set the right direction of the current, to control the ADC and to calculate the temperature.

Figure 1 shows the circuit diagram of the voltage-to-current converter. The currents I_P and I_N convert the unknown resistance of R_X and the resistance of R_0 (which is used as reference) to a voltage. The input current (I_E) of the ADC is the sum of an offset current (I_O) and the current, which comes from the voltage across R_X or R_0 (depending on the pairs of switches 3 and 4) and R_S. I_O makes I_E positive for all values of R_X and both currents I_N and I_P.

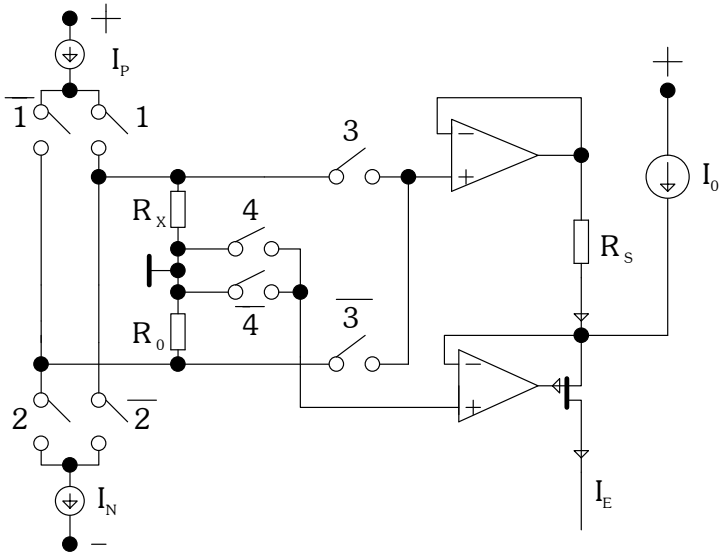

Fig. 1: Voltage-to-current converter

The control signals for the switches 1 to 4 are provided by the microcomputer. For one value of R_X we get four different currents I_E and therefore also four results of an analog-to-digital conversion. From these results we can get the ratio R_X/R_0 by subtraction and division without errors of the order zero (thermo- and offset voltages) and the order one (value of I_P, I_N and R_0).

Figure 2 shows the structure of the ADC [7], [10], [11]. The comparator S determines the discharge of capacitor C_i after the conversion. Comparator C is used to show that the voltage across C_i is lower than the voltage U_{Ref}. Switch 9 is used to start the conversion with the capacitor C_i discharged. The complementary pair of switches 6 can guide the current I_E either to the input or the output of the integrator. The same is done with the reference currents I_R and $I_R/256$ and the switches 7 and 8.

The current I_E is integrated for 0.1 s. The reference current I_R compensates I_E in this phase using a Charge-Balance method. The charge in C_i after this integration is determined with the help of $I_R/256$. The numeric result of this conversion is 256 times the number of clocks during the disintegration using I_R in addition to the number of clocks used for discharging with $I_R/256$.

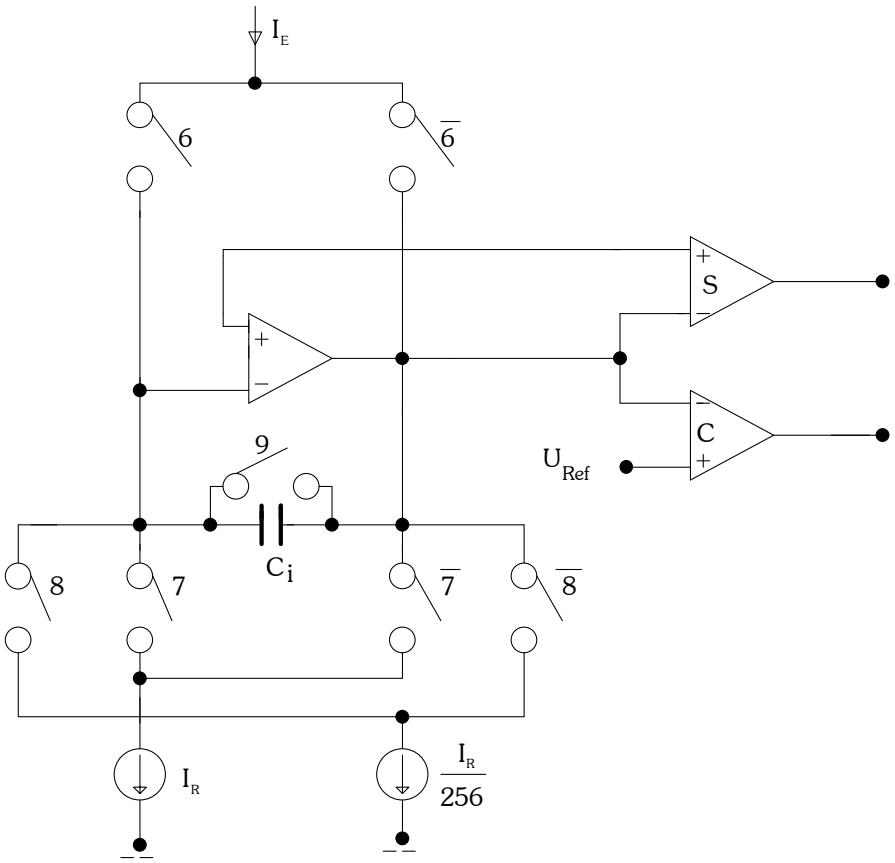

Fig. 2: Structure of the ADC

To control all the switches and to provide the time frame for the conversion a digital control unit is used. The number of clocks is counted by the microcomputer which also calculates the temperature either using IEC751 or ITS-90.

To be able to add more channels, to add more flexibility to the system of the thermometer and to overcome the electromagnetic compatibility (EMC) problems with digital signals on lines (between the comparators and the microcomputer) near a 23-bit ADC an ASIC (ENDEAVOR) was designed [12].

The number of channels was increased to eight. The counters for the clock pulses, which are the result of the analog-to-digital conversion, are added on-chip. There are no digital signals outside the ASIC when a conversion is made. On-chip counters have a low load capacitance on the clock line. Spikes in the power supply are therefore avoided. The information is serially transferred to the microcomputer at a time, when no conversion is going on. The digital signals then can cause no interference to the result of the conversion.

Figure 3 shows the block diagram of ENDEAVOR. A crystal oscillator provides the system clock of 1 MHz. Counters and decoders generate the control signals. A baudrate generator is implemented to provide a serial output signal of 9600 baud. The information has ASCII format, so a simple terminal program can be used to visualize the results of the conversions. The implementation of the original control unit guarantees compatibility to the existing system. The channels are periodically activated for measurement. The sequence can be set up with control signals.

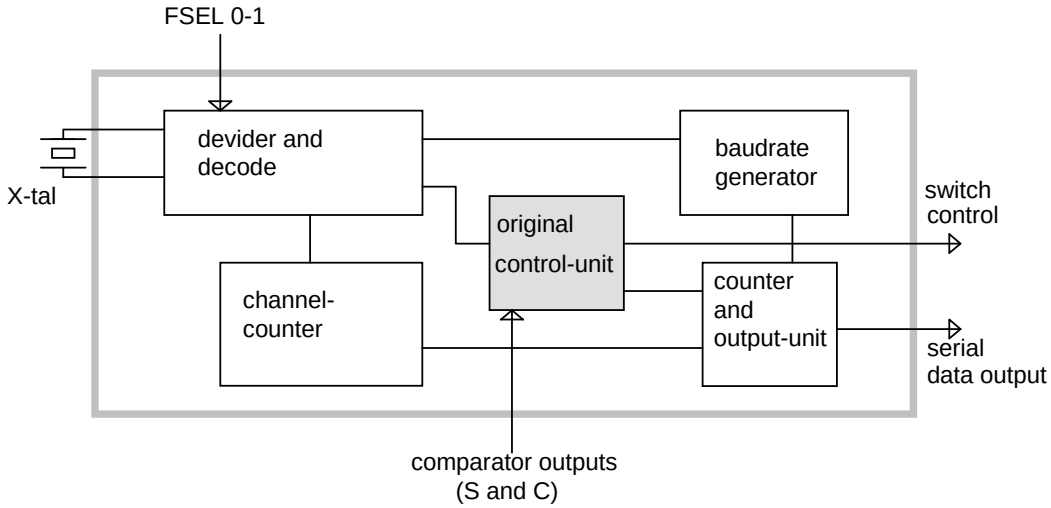

Fig. 3: block diagram of the ASIC

The ASIC is in fabrication (0.8 µm AMS CMOS-process) at the moment. The transistor count is approximately 5500. The size is 1.9x1.9 mm^2. A 28 pin PLCC package is used. The first engineering samples are expected for the middle of March 1997. Then it will be seen if the selected targets could be reached:

- No digital signals outside the ASIC during conversion should bring a reduction of the system internal noise interference. The expected increase in the ADCs resolution is at least from 23 to 24 bits.
- 4 times more channels (8 instead of 2).
- More flexibility: a simple terminal program can be used to visualize the results of the conversation; the sequence of the active channel can be changed via control signals.
- Less power consumption and less space requirements for a smaller and cheaper thermometer.

5. Conclusion

The use of ASICs in electronic instrumentation offers a wide spectrum of advantages. Topics which lead to the decision to start the design of an ASIC are not only reduction of space and power consumption but are also sometimes problems of EMC. In most cases the functionality and reliability of the system can be raised as shown with the examples of the industrial instrumentation (multi-channel measurements and better overall performance). BiCMOS technology is supposed to bring new advantages in some critical analog integrated circuits.

Acknowledgment

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Silicon Technology: Risks, Opportunities and Challenges

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1. Introduction

The enormous progress of microelectronics over the last two decades has resulted in an orders-of-magnitude increase in computational power and storage capacity. There is a general consensus in industry and academia that this exponential growth will continue for another 10 to 15 years.

Progress will come at a price, however. The increase in both technology process and product design complexity will require enormous interdisciplinary efforts to cope with the challenges ahead. Finally the often quoted "limits of microelectronics" may be less determined by the physical limits of device miniaturization but by economic considerations, both on the manufacturing and design levels.

Future technologies (nanotechnology, quantum electronics, molecular electronics) will have to measure up to this criterion as well. It will be difficult for them to prove their viability in view of the overwhelming momentum, both technical and economic, that silicon technology has gained over the last three decades.

2. Roadmap

In the 1970s, Gordon Moore predicted a doubling of complexity for Silicon ICs every 18 months [1]. Ever since, analysts have warned that deviations from this exponential behavior were imminent, quoting "barriers" at minimum feature sizes of, e.g., one micron, 0.5 µm, 0.25 µm, for various physical and technical reasons. Today it seems likely again that we may experience a deviation from "Moore's law" – to even faster growth.

For the last several years, the US-based Semiconductor Industry Association (SIA) has convened a panel of microelectronics experts who develop and maintain a National Technology Roadmap for Semiconductors (NTRS) [2]. Figure 1 shows a strongly condensed version. The NTRS predicts a continuing exponential increase in IC complexity, according to Moore's law, extending to minimum feature sizes of 0.07 µm at 64 Gbit memory densities in 2010.

	1995	1998	2001	2004	2007	2010
Feature size (µm)	0.35	0.25	0.18	0.13	0.10	0.07
Memory	64 M	256 M	1 G	4 G	16 G	64 G
Logic (µP) Trans./cm^2	4 M	7 M	13 M	25 M	50 M	90 M
Chip frequency (MHz)	300	450	600	800	1000	1100
Substrate dia. (mm)	200	200	300	300	400	400
Supply Voltage Standard	3.3	2.5	1.8	1.5	1.2	0.9
Portable	2.5	1.8-2.5	0.9-1.8	0.9	0.9	0.9

Semiconductor International 1995

Fig. 1: National Technology Roadmap for Semiconductors (SIA NTRS)

Since its first presentation the NTRS has become a “self-fulfilling prophecy”. Everyone expects that their competitors’ speed of innovation is obeying the same (or even faster) pace. The burden is on microelectronics research and development to make the NTRS a reality. The following paragraphs will outline a few of the technical challenges that face us.

3. Processing Challenges: Lithography

The most obvious “barrier” for further reduction of feature size is the possible lack of a suitable mask printing process. According to earlier predictions, X-ray lithography should have replaced optical lithography at the 0.5 µm level already, due to the limit imposed by the wavelength of visible light.

Today, however, printing of 0.25 µm structures is the industry standard, using a wavelength of 248 nm (deep UV, KrF excimer laser light).

The first ArF (193 nm)-light-based lithography is currently being installed and may yield an industrially viable process at least down to 0.13 µm (Fig. 2). Adding the possibilities of special enhancement techniques (Phase Shift Masks (PSM), Off Axis Illumination (OAI), Optical Proximity Correction (OPC)) plus F_2 (157 nm)-light at the horizon, optical lithography may take us all the way to 0.1 µm structures.

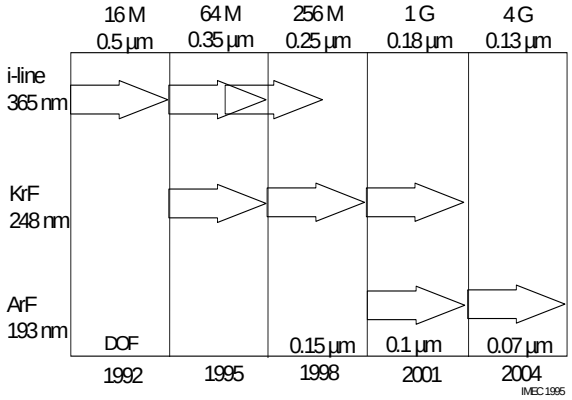

Fig. 2: Roadmap for optical lithography into the 0.1µm generation

Incidentally, 0.1 µm is also the resolution limit for X-Ray lithography with conventional shadow masks [3].

However, the advent of these leading edge optical techniques will require enormous qualitative leaps in, e.g., optics, photoresist, antireflective coatings, planarization processes and metrology (overlay accuracy is most critical). Last but not least, the enhancement techniques mentioned above will result in a complex relationship between circuit design / layout and technology, requiring a huge interdisciplinary involvement of the CAD tool community.

4. Materials Challenges

As device dimensions shrink into the deep sub-micron regime, some of the electrical parameters escape the usual trend towards better performance. As an example, the requirements for data retention in a dynamic memory device (DRAM) force us to keep the storage capacity at approximately 30 fF. Given the decreasing lateral feature size this means an increased size in the third dimension. For one of the most successful ideas in DRAM, the trench capacitor, this “escape” is coming to an end, however, starting at the 1 Gbit level. Etching depths for the trench capacitor are becoming prohibitive (> 10 µm), even if more for economic than technical reasons (Fig. 3).

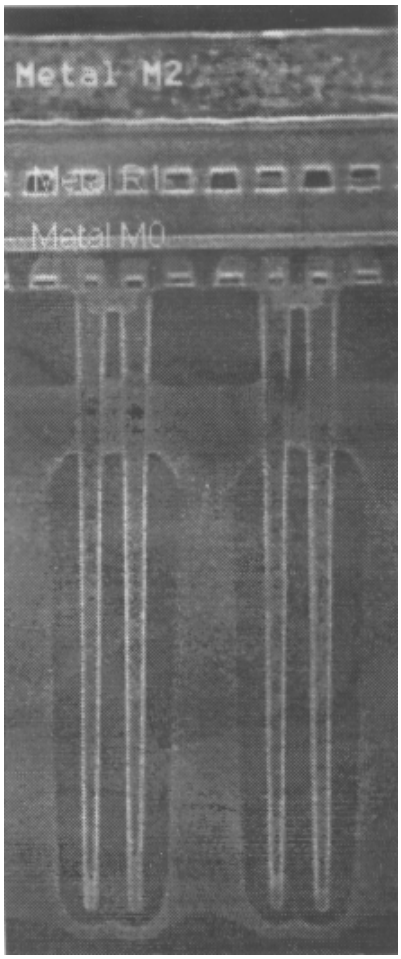

Fig. 3: 256M DRAM trench cell (IBM/Siemens/Toshiba)

Similar arguments hold for a capacitor stacked on top of the silicon surface. Since the thickness of the storage dielectric cannot be shrunk beyond the tunneling limit, the options to maintain the storage capacitance are reduced to an increase in the dielectric constant. This increase must go much beyond what is available from SiO_2 ($\varepsilon_r \approx 4$) or ONO ($\varepsilon_r \approx 7$).

One of the presently favored high ε materials is $(Ba,Sr)TiO_3$ (Barium-Strontium-Titanate or BST) which exhibits paraelectric behavior at room temperature with $\varepsilon_r >> 100$. The use of BST as a storage dielectric will also pave the way for introducing "real" ferroelectric materials (like Strontium-Bismuth-Tantalate, SBT) into memories. Ferroelectric RAMs (FRAMs) may be the ultimate storage solution, combining non-volatility as in EEPROMS with the speed of DRAMs.

Introducing these materials into silicon processes has numerous challenges, however. Capacitor dimensions in the tenth-micrometer range require thin (30 nm) layers of high ε material, conformally deposited over high-aspect ratio, deep-sub-micron structures, without sacrificing crystallinity and stoichiometry. This requires a well-controlled multi-component CVD process, followed by a high temperature anneal in oxygen. This in turn requires new electrode materials (candidates are Pt, Ru, RuO_2, Ir) and appropriate barrier materials since silicon components will oxidize strongly at these conditions. Accompanying the materials and process challenges is the risk of contaminating the IC fabrication line with these "exotic" substances.

Generally, the realization of the NTRS will require a "paradigm shift" away from silicon components and related "simple" materials to more risky substances (Fig. 4). Solving these problems will again require an interdisciplinary approach from material scientists and chemists, analytics experts, process and equipment designers and integration specialists.

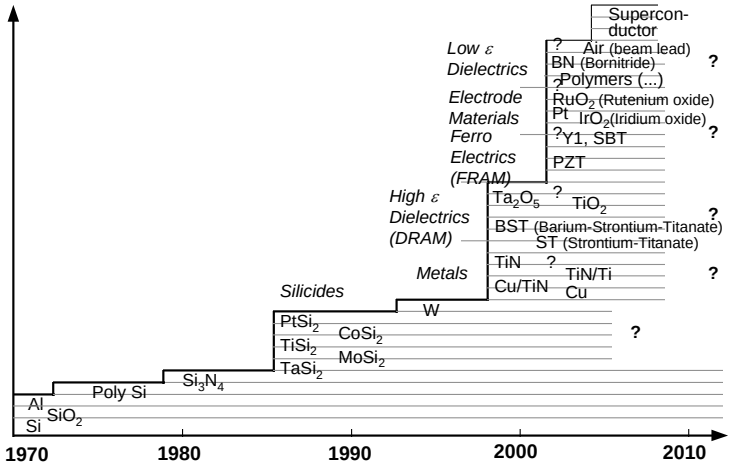

Fig. 4: Progress in microelectronics increasingly requires the introduction of new materials

5. Manufacturing challenges

The cost of IC manufacturing has seen an exponential behavior comparable to Moore's law . In view of the decreasing minimum feature sizes, the decreasing critical defect density, the increasing wafer size and increasing number of process steps (e.g. needed for the integration of new materials) it seems unlikely today that the cost curve will bend down in the future.

To meet this economic challenge will require applying "smartness" to all levels of manufacturing. On the equipment side the major issue will be to increase utilization, i.e. the time in which actual production wafers are processed. A way to achieve this goal is short-loop controlled, in-situ monitored single wafer equipment. That in turn demands detailed knowledge of physics and chemistry of the processes which must be gained through intense use of simulation and analysis tools. On the process integration side, "Smart Fabrication" calls for modular cost-effective processes with harmonized process flows across a large mix of different products.

On the product development side, design for manufacturability will be the major challenge. The main issues here will be to get the most performance at the lowest power from a given technology on one hand, and the highest yield on the other hand. This will require in part to break with one of the most successful paradigms in microelectronics, which was the separation of technology process details from the circuit and system design levels. A new level of computer aided technologies will have to be generated to deal with this new complexity [4], [5].

6. Outlook

In view of the predictions of the SIA NTRS, it seems that there is no need for an alternative to Silicon ICs in the foreseeable future. Adding the production lifetime of a technology of at least 10 years to the 2010 timespan of the NTRS, we may have a quarter of a century before silicon will be "outdated". Nevertheless, one of the most threatening physical effects that may force us much earlier to seek for alternatives is power consumption. Simple calculations show that, without revolutions in system architecture and technology, systems-on-chip in the 64 Gbit age will be prohibitively power-hungry.

The ultimate low power device (in theory at least) may be a Single Electron Transistor. It allows switching of states with just one electron based on the Coulomb blockade effect.

However, it seems unlikely that these devices will simply replace today's MOSFETs in logic circuits. Rather, they will probably lead to new systems architectures. They may even use a different signal representation than binary logic, e.g., multilevel logic or error-tolerant designs. The same considerations may be even more true for "biological" technologies (like molecular electronics).

In any case, it seems safe to say that these alternative technologies will require an industrial commitment of at least the size of silicon microelectronics today to become "mature". Nevertheless, these technologies — in the long run — may change the world as profoundly as silicon technology has done in the last two to three decades.

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„Mixed Signal“ und „Smart Power“ — Kernkompetenzen für den globalen Mikroelektronikmarkt

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Im weltweiten Wettbewerb in der Mikroelektronik werden Kernkompetenzen immer wichtiger, weil sie einen wesentlichen Standortvorteil darstellen können. Die Globalisierung umfaßt heute nicht nur Aspekte der Niedriglohnfertigung einfacher Arbeiten, sondern in immer stärkerem Ausmaß auch hochwertige Fertigungs- und Entwicklungstätigkeiten. Am Beispiel gemischt analog-digitaler Schaltkreise („mixed signal“) und integrierter Systeme der Leistungselektronik („smart power“) wird gezeigt, wie Know-how-intensive Bereiche mit starkem Systemanteil dennoch in Europa für den Weltmarkt konkurrenzfähig entwickelt werden können.

1. Einleitung

Im Bereich der Mikroelektronik kann seit einigen Jahren, ähnlich wie bei anderen Industrien, ein starker Trend zur Globalisierung beobachtet werden. Dies betrifft nicht nur die Fertigungseinrichtungen (Wafer Fabs, Montagen), sondern zunehmend auch die Entwicklungsressourcen. Beispiele hierfür können in allen großen Firmen der Mikroelektronik gefunden werden, seien es Halbleiterhersteller oder Baugruppen- und Systemlieferanten. Eine besondere Attraktivität bieten für diese Firmen die aufstrebenden Länder im südostasiatischen Raum. Dort ging man in den letzten Jahren dazu über, nicht nur als Billiglohnland Fertigungen bereitzustellen, sondern zunehmend auch Entwicklung vor Ort zu betreiben.

Dafür gibt es mehrere Gründe: Die Förderpolitik vieler Staaten dieser Region orientiert sich am Grad an Innovation, die beim Transfer von Einrichtungen in diese Länder mit eingebracht wird. Häufig werden wesentliche Steuererleichterungen („Pioneer Status“) oder die Zollpolitik damit verknüpft. Der Wunsch nach einer Präsenz im lokalen Markt und als Folge daraus die Entwicklung spezieller, auf diesen lokalen Markt zugeschnittener Produkt (z.B. Videotextbausteine oder Betriebssystemvarianten für chinesische Schriftzeichen) stellen weitere Motivationsfaktoren dar. Nicht zuletzt muß darauf hingewiesen werden, daß durch das große Wachstum im Bereich der Mikroelektronik und Telekommunikation weltweit eine Verknappung höherer Qualifikationen am Arbeitsmarkt droht und in diesen Ländern hervorragendes Know-how vorhanden ist.

In diesem weltweiten Wettbewerb ist es nun für die Entwicklung und die Fertigung sowie das erfolgreiche Zusammenwirken beider wesentlich, eine sinnvolle Zuordnung von Kernkompetenzen zu finden. Je nach Firma und Produktspektrum, sowie nach dem in externen Stellen (Universitäten und Forschungseinrichtungen) vorhandenem Spezial-Know-how können sich unterschiedliche Strukturen ergeben.

2. Integrierte Schaltungen — Grundtypen

In einer groben Kategorisierung der Entwurfsverfahren für Integrierte Schaltkreise kann man zwei Varianten sehen:

Die eine Variante basiert auf vordefinierten Elementen, das sind vorwiegend digitale Grundzellen und Teilblöcke, und nähert sich der Implementierung in Silizium von der informationstechnischen Seite, ähnlich wie beim Softwareentwurf. Die Schwerpunkte dieses Bereiches liegen beim Entwurf und der Optimierung von übergeordneten, digitalen Systemen, Architekturen von Datenpfaden sowie ganzer Rechnerkerne, bei der Implementierung von Algorithmen und Funktionen. Die Abbildung dieser Eigenschaften auf Silizium erfolgt stark automatisiert über Entwurfssprachen wie z.B. VHDL. Die Simulation beschränkt sich auf die funktionale und logische Ebene. Nach diesen Methoden werden komplexe, vorwiegend digitale Komponenten, wie sie z.B. in Rechnersystemen, Personal Computern und Baugruppen der Telekommunikation Einsatz finden, entworfen (Abb. 1), aber auch Teilfunktionen von Bausteinen, wie sie im folgenden betrachtet werden.

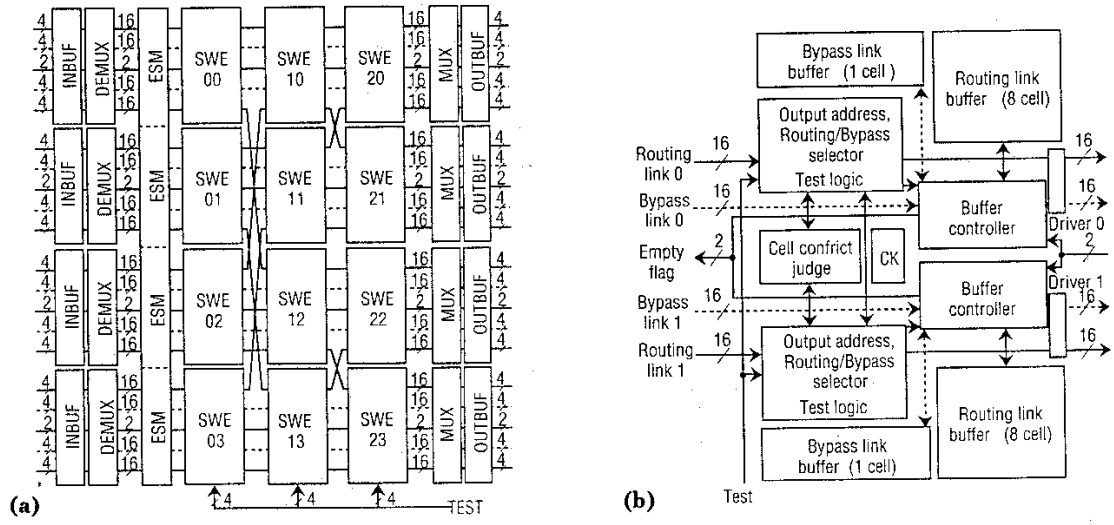


Abb. 1: Blockdiagramm (a) und Teilstruktur (SWE) (b) eines Hochgeschwindigkeits-Datenübertragungsbausteins [1]

Die andere Variante des Entwurfs beginnt beim einzelnen Schaltelement und sieht dieses und seine Eigenschaften von der elektrotechnischen Seite, die Simulation beginnt in der Entwurfshierarchie ganz unten und berücksichtigt in hohem Maße die elektrischen Eigenschaften der Bauelemente und der Verbindungsstrukturen. Man setzt sich intensiv mit Wechselwirkungen der Bauelementeigenschaften mit der Chiptemperatur, den Umgebungseinflüssen und den technologischen Grundlagen auseinander. In diesen Bereich fällt die gemischt analog-digitale Systemintegration, die heute bereits Leistungsbauelemente und Sensoren am gleichen Substrat mitbetrachtet. Es hat sich gezeigt, daß in diesem Bereich der Aufbau von Know-how der Mitarbeiter und das Formen einer Gruppe mit Kernkompetenz und Erfahrung mehrere Jahre dauert. Auch die intensive Zusammenarbeit mit den Technologen der Fertigungseinrichtungen spielt hier eine große Rolle für den Markterfolg. Da in einem solchen Zeitraum eine Vielzahl von sehr engen Kundenbeziehungen aufgebaut wird und daher nicht nur das Wissen über die einzelnen Schaltungen, sondern auch über die bearbeiteten Gesamtsysteme wächst, konnte eine im

weltweiten Vergleich sehr gute Wettbewerbsposition der Entwicklung in Villach entstehen. Dies zeigt sich einerseits am Erfolg der hier entwickelten und teilweise auch gefertigten Produkte, die in hohen Stückzahlen am Weltmarkt eingesetzt werden, andererseits an einem deutlichen Anstieg der Nachfrage nach den Entwicklungsleistungen, der eine Verdoppelung der Entwicklungsressourcen während der letzten 4 Jahre zur Folge hatte.

In den folgenden Abschnitten werden die Gebiete „Smart Power“ und „Mixed Signal“ näher dargestellt. Dies umfaßt Aspekte des Entwurfs und der Fertigung sowie einige Beispiele.

3. Mixed Signal - Gemischt analog-digitale Systeme

Die folgenden Abb. 2 und 3 zeigen als Beispiel für gemischt analog-digitale Systeme Anwendungen aus dem Telekommunikationsbereich. Typische Komponenten sind analoge Frontend-Blöcke zur Ankopplung an Übertragungsstrecken, seien dies nun elektrische oder optische Kanäle bei Modems oder die akustische Kopplung zum menschlichen Ohr beim Telephon, sowie verschiedene digitale Signalverarbeitungselemente. Die Systeme aus Abb. 3 folgen diesem allgemeinen Schema.

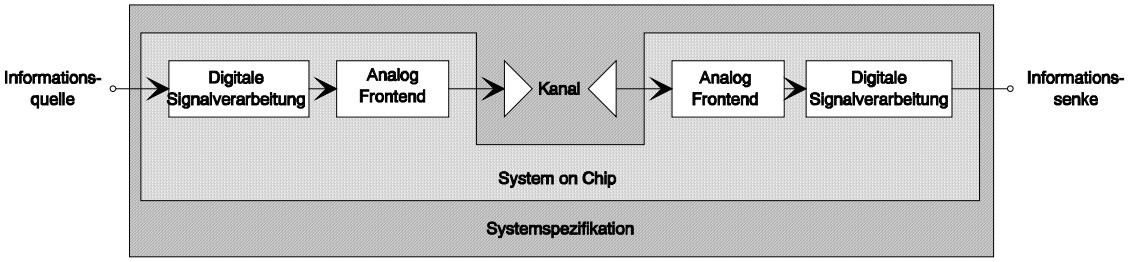


Abb. 2: Beispiel für ein „System on the Chip“ für die Kommunikationstechnik

	GSM	DECT	IEC	SLICOFI
DSProcessing	Sprachkodierung	Sprachkodierung	Echo Kompensation	Voice Codec
	Kanalkodierung	Modulation/Demodulation	Entzerrer	TTX-Erzeugung,Filter
	Modulation/Demodulation			On Chip Ringing
	Entzerrer			
Analog Frontend	Mischer auf RF	Mischer auf RF	PAM Modulation	A/D, D/A Umsetzung
	A/D, D/A Umsetzung	A/D, D/A Umsetzung	A/D, D/A Umsetzung	
Kanal	Luftstrecke 900, 1800 MHz	Luftstrecke 1900 MHz	Kupferkabel	Kupferkabel/SLIC

Abb. 3: Typische Systembeispiele aus der Kommunikationstechnik

Aufgrund der stetig ansteigenden Integrationsdichte sind nunmehr ganze Systeme in integrierter Form auf einem Schaltkreis möglich. Damit hat sich auch die Schnittstelle zwischen dem Systemhaus und dem Halbleiterhersteller verschoben. Der Entwurf erfolgt in enger Zusammenarbeit („Concurrent Engineering“) nunmehr beim Halbleiterhersteller, die Aufgaben des Systemhauses haben sich auf höhere Ebenen verschoben. Durch diese Veränderungen der letzten Jahre hat sich eine wesentliche Aufwertung der Rolle des IC-Entwurfs ergeben, der auch zu größeren Herausforderungen führte. Die Entwurfssysteme und Entwurfsverfahren haben in ihrer Komplexität deutlich zugenommen, bereits beim Aufteilen des Systems auf einzelne Schaltkreise müssen in

enger Abstimmung die richtige Fertigungstechnologie und geeignete Schaltungskonzepte gewählt werden, um wirtschaftlich erfolgreich zu sein.

Weiters ist die Gesamtfunktion innerhalb des jeweiligen Bausteins nach technischen und wirtschaftlichen Gesichtspunkten optimal aufzuteilen auf:

- analoge Komponenten (Anpassungsschaltungen, Verstärker, Filterstrukturen)
- geeignete AD-Wandler (häufig werden hier ΣΔ-Umsetzer verwendet)
- digitale, festverdrahtete Strukturen (Filter, Kompression/Expansion)
- programmierbare Signalprozessorelemente (Filter-Algorithmen)

Für erfolgreiche Projekte ist ein erfahrenes Team mit einer über Jahre gewachsenen Kernkompetenz von großer Bedeutung. Die Umsetzung in Integrierte Schaltungen wird durch geeignete CAD-Systemkomponenten zwar unterstützt, das Zusammenspiel der verschiedenen Entwurfs- und Simulationsebenen erfordert aber einen breiten Erfahrungshintergrund. Eine schematische Darstellung der einzelnen Komponenten und Entscheidungsebenen vom realisierungsunabhängigen Konzept bis zur Verifikation der physikalischen Realisierung findet sich in Abb. 4.

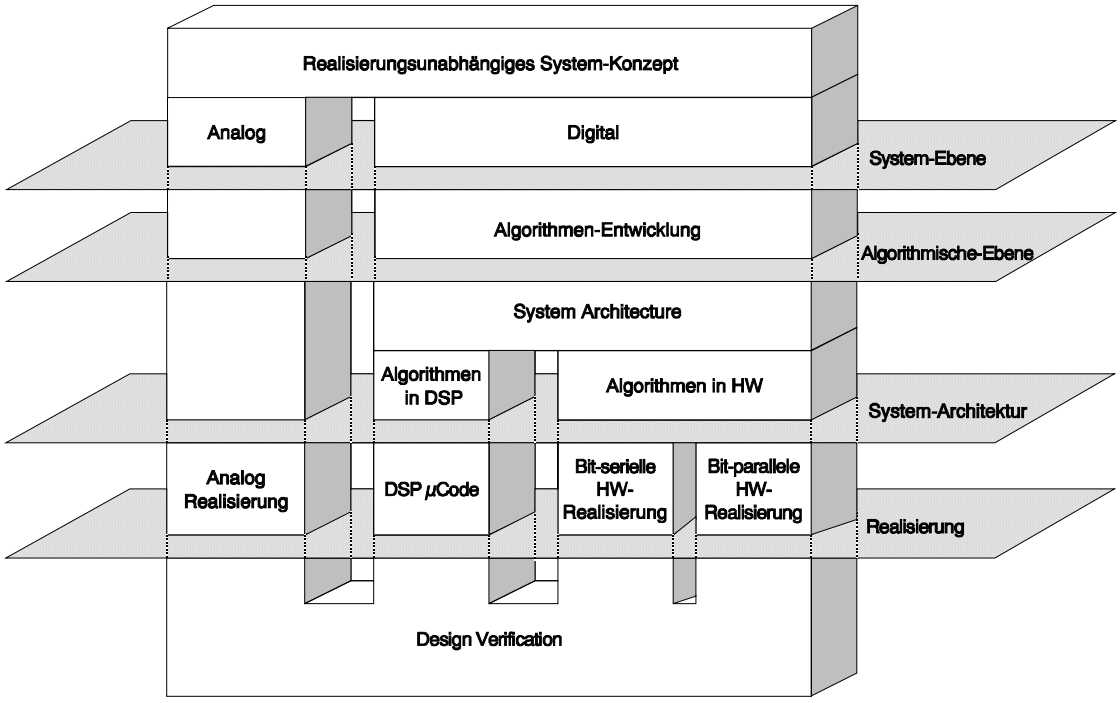


Abb. 4: Struktur des Entwurfssystems für komplexe gemischt analog-digitale Schaltungen

In der Folge findet sich ein realisiertes Beispiel, das am Markt bereits in hohen Stückzahlen sehr erfolgreich ist [2], [3]. Es handelt sich hier um eine 2-Chiplösung für die Ankopplung konventioneller, analoger Telephonleitungen an digitale Vermittlungsämter. Dieses Gebiet stellt auch heute noch ein großer Markt existiert.

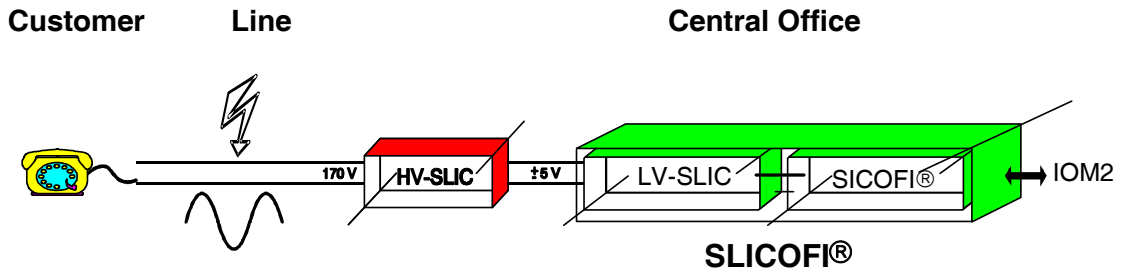
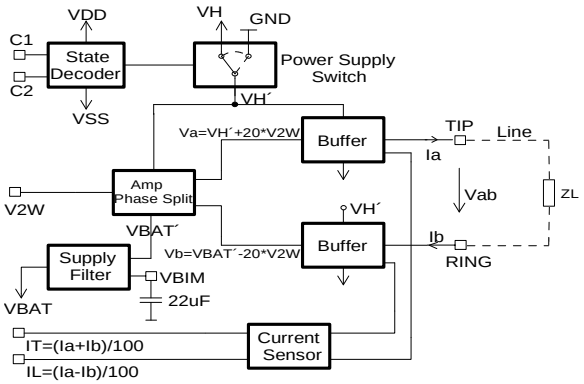


Abb. 5: Schema eines Kanals der Leitungsanschlußbaugruppe einer digitalen Vermittlung

Für die Applikation aus Abb. 5 wurden die Technologien (170 V BiCMOS/DMOS und BiCMOS 0,8 µm 5 V) nach den externen (Leitungsüberspannung) und internen Anforderungen (Integrationsdichte, Übertragungsdaten) ausgewählt und die Gesamtfunktion entsprechend aufgeteilt [2], [3]. Die besondere Herausforderung dieses Systems lag in der Kombination der hohen Spannungsfestigkeit und der hohen Ströme auf der Leitung bei gleichzeitig hoher Präzision der Übertragungseigenschaften (Verstärkungstoleranz, Frequenzgang, S/N-Verhältnis).



Technology	170V junction isolated
Devices	BICMOS and High Voltage DMOS, lateral PMOS High Precision Poly Resistors Zener & HV Diodes
	Technical Data
Supply	150 V
Output	85 Vrms / 100 mA
Power Dissip.	250 mW Active 1.300 mW Ringing
PSRR	>40 dB
Gain flatness	0,01 dB (300 - 3.400 Hz)
Long. Reject.	70....90 dB @ a / b

Abb. 6: Blockschaltung und technische Daten des HV-SLIC Bausteins

4. Smart Power - Intelligente Systeme der Leistungselektronik

Der Markt der Integrierten Schaltungen zeigt nicht nur in den traditionellen Bereichen, wie z.B. Informations- und Signalverarbeitung ein deutliches Wachstumspotential, sondern auch in den Bereichen der Leistungselektronik. Dies betrifft neben den Einzelbauelementen (Leistungstransistoren, Thyristoren, Dioden) insbesondere das Gebiet der „Smart Power Systems“. Moderne Technologien ermöglichen innovative Systemlösungen, welche konventionelle Bauelemente wie Sicherungen, Relais und Schalter durch Transistoren mit integrierten Überwachungsschaltungen ersetzen. Beispielsweise können Ströme und die Chiptemperatur überwacht, der Zustand an eine Zentralelektronik

gemeldet und der Leistungsteil bei kritischen Zuständen abgeschaltet werden. Dies ist beispielsweise im Automobilbereich von großer Bedeutung, aber auch in der Industrieelektronik und bei EDV-Geräten (Festplatten, Drucker).

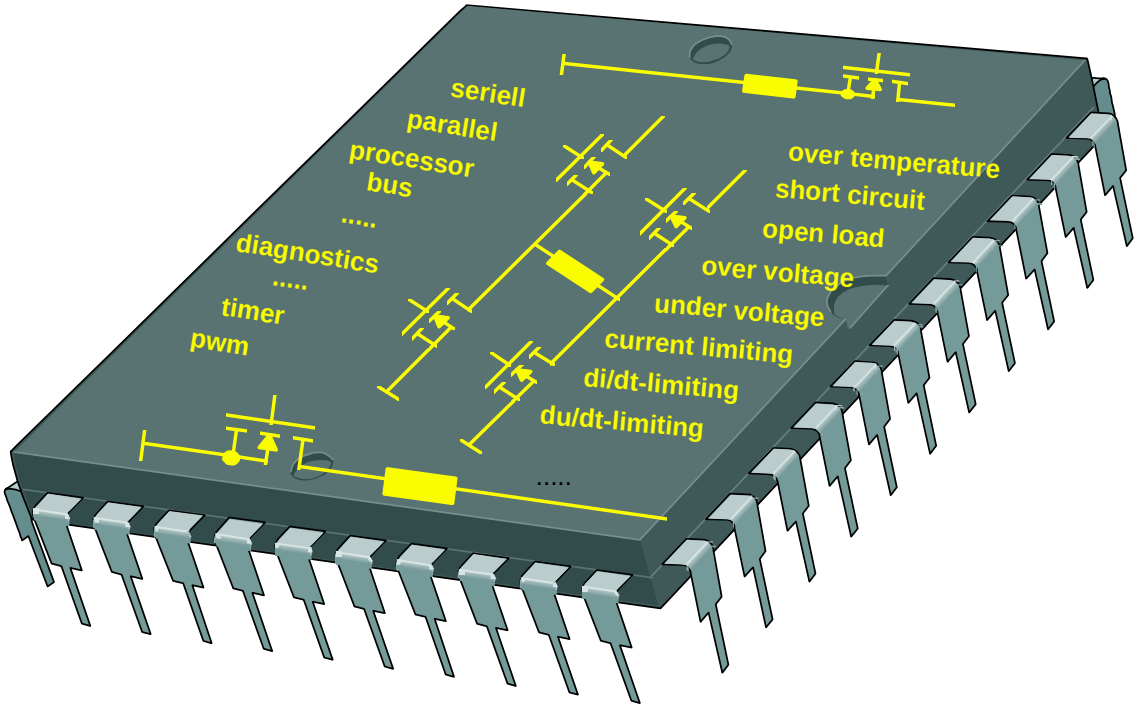


Abb. 7: Funktionsblöcke von Smart Power Schaltern

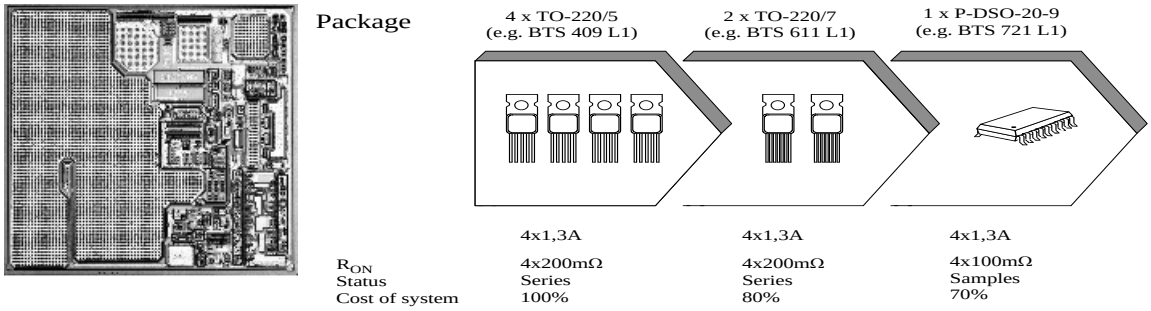


Abb. 8: Smart Power Schalter bringen erhebliche Vorteile in der Automobilelektronik (Chipphoto links und Gehäuseformen rechts im Bild).

Mit den heute bei verschiedenen Firmen verfügbaren Technologien ist es möglich, ganze Systeme auf einem oder einigen wenigen Chips zu integrieren [4]. Dies führt zu einer systematischen Miniaturisierung (z.B. Antiblockiersysteme [5], Airbagsysteme, Systeme für die Steuerung von EDV-Einheiten, etc.) bei gleichzeitiger Erhöhung der Zuverlässigkeit und Reduktion der Kosten. Systemintegration bedeutet dabei, daß verschiedenste Funktionen, analoge Verarbeitung, Stromversorgung, digitale Steuer- und Kommunikationsfunktionen bis hin zu einem kompletten Mikrocontroller auf einem Stück Silizium zusammengefaßt werden können. Damit wird die Zusammenfassung elektronischer, mechanischer und hydraulischer Komponenten zu sehr kompakten, zu-

verlässigen mechatronischen Modulen möglich. Abb. 9 veranschaulicht diese Entwicklung. Ähnlich wie bei den im Abschnitt 3 beschriebenen Entwicklungen ist auch in diesem Gebiet die vertrauensvolle, enge Zusammenarbeit mit den Kunden von wesentlicher Bedeutung. Die rasche, kostengünstige und zuverlässige Entwicklung und Realisierung hängt auch hier in hohem Maße von dem Aufbau und der Pflege einer Entwicklungsmannschaft mit Kernkompetenz ab. Durch die hohen Ströme und kritischen Umweltbedingungen ist die räumliche Nähe einer Fertigungsstätte hier von besonderer Bedeutung für die Umsetzung erfolgreicher Entwicklungen in Markterfolge.

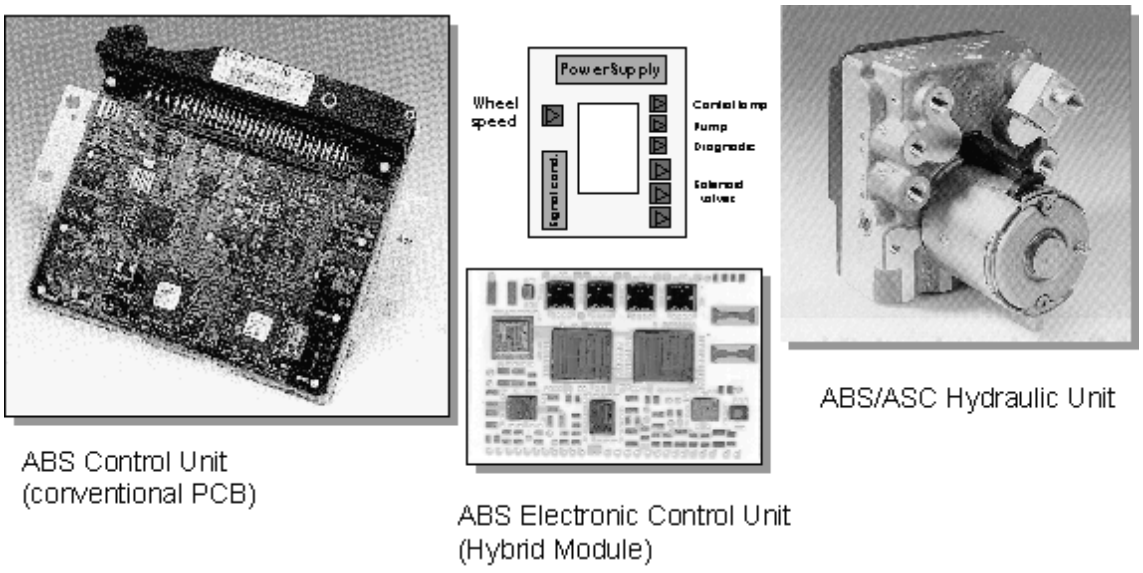


Abb. 9: Miniaturisierung der elektronischen und hydraulischen Komponenten, gezeigt am ABS-System: links konventionelle Leiterplatte, Mitte: hybrid aufgebautes System mit hohem Integrationsgrad, rechts: mechatronisches Element mit höchstintegriertem Smart Power Chip.

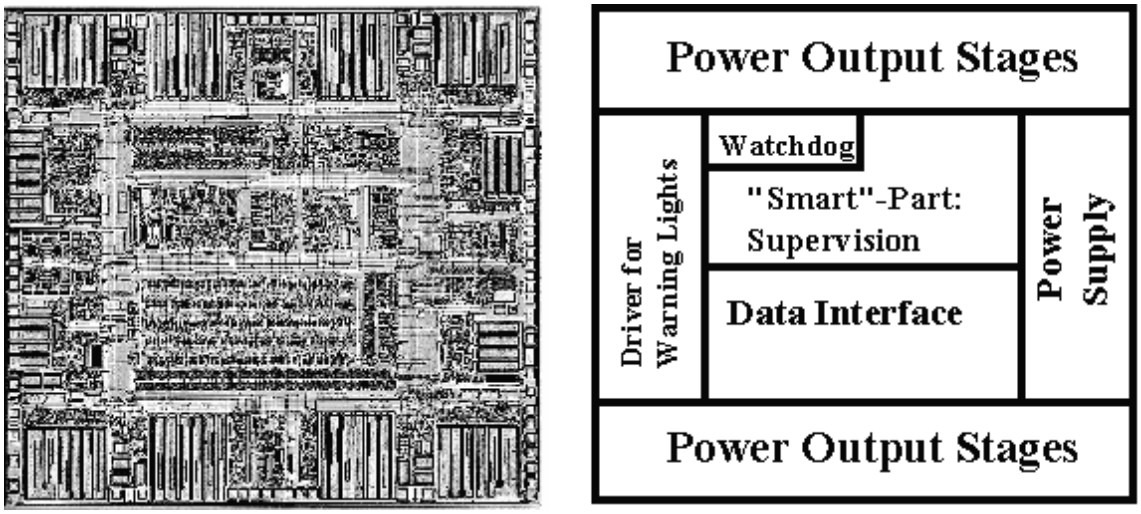


Abb. 10: Chipphoto eines Smart Power Systemschaltkreises mit Bezeichnung der Teilblöcke

5. Schlußbemerkungen

Die Bereiche gemischt analog-digitale Schaltungen und Smart Power stellen Kernkompetenzgebiete für Entwicklung und Fertigung dar. Dieses Know-how kann nur über einen längeren Zeitraum kontinuierlich aufgebaut werden, lebt sehr stark von intensiver Zusammenarbeit mit den Kunden und umfaßt als wesentliches Element anwendungsspezifisches Systemwissen. Diese fachspezifischen Aspekte stellen gemeinsam mit dem zu erwartenden Marktwachstum eine gute Basis für eine längerfristige Konkurrenzfähigkeit auf Weltniveau und somit eine gute Zukunftsperspektive dar. In technischer Hinsicht kann eine weitere Erhöhung der Integrationsdichte in beiden Bereichen erwartet werden. Daraus werden neue Herausforderungen an die Kreativität im Bereich der Technologie und Schaltungstechnik, aber auch neue Systemkonzepte und wesentliche Innovationen bei den CAD/CAE-Methoden erwachsen.

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Single-Mode and Single-Beam Emission from Surface Emitting Laser Diodes Based on Surface Mode Emission

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Single-mode and single-beam emission has been achieved from surface emitting laser diodes based on the surface-mode-emission technique. By employing an optimized device design and a first-order grating coupler, the laser diodes show under pulsed operation condition a single-mode emission with a linewidth of 0.11 nm. A power up to 3.6 mW is emitted into a single, surface-emitted beam, which has a beam divergence of 0.20^{o}.

1. Introduction

The most important impact of laser diodes is the area of transmission systems for optical telecommunication, where single-longitudinal-mode (SLM) laser diodes are required to achieve a high transmission capacity and distance. Among the various types of single-mode laser diodes the distributed-Bragg-reflector (DBR) and the distributed-feedback (DFB) laser diodes are most commonly used and have been successfully employed in commercial transmission systems [1], [2]

By far most of the present SLM-laser diodes are conventional edge emitters, while many novel optoelectronic applications, like optical interconnects, optical computing and high power laser arrays, require surface emitting laser diodes. Various types of surface emitting laser diodes, like horizontal cavity lasers with 45°-mirrors, DBR and DFB-laser diodes with second order grating couplers, Master-Oscillator-Power-Amplifiers and Vertical Cavity Surface Emitting laser diodes have been developed so far [3] – [5].

We have presented a new concept based on the surface-mode-emission (SME) technique, which has been applied to realize a new type of surface emitting laser diode [6], [7]. In addition we have recently proposed this technique as flexible concept for a new type of SLM-laser diode [8]. A real single-mode emission from this type of laser diode, however, has not been achieved yet [9].

2. Experimental

We report on a single-mode and single-beam emission achieved from SME-laser diodes. Under pulsed operation condition a single-mode emission with a linewidth of 0.11 nm is achieved, while a power up to 3.6 mW is emitted into a single, surface-

emitted beam with a beam divergence of 0.20^{o}. This has been achieved by an optimized device geometry and by fabricating high-quality first-order gratings with an Ion-milling etching technique.

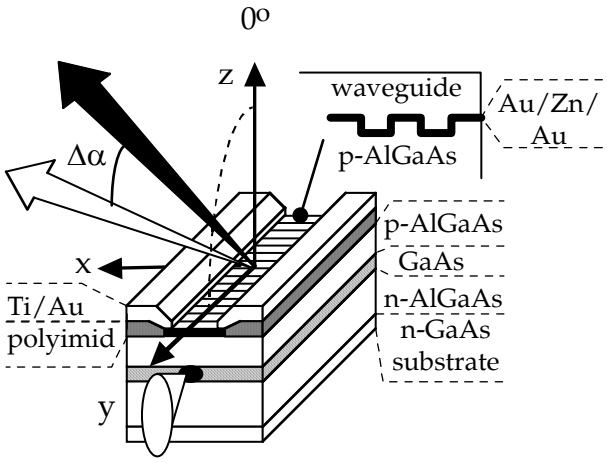

Fig. 1: Geometry of the SME-laser diodes. The surface grating is oriented in y-direction, while the laser stripe is oriented in x-direction. The window for the SME-coupling process has a width of 8 µm and extends over the whole length of the cavity.

The SME-technique is based on an interactive coupling between the laser light propagating in the active region of the laser diode and a transverse electrically polarized TE_0-surface mode propagating in a waveguide structure on top of the laser diode. This requires a special device geometry, which is shown in Fig. 1. The laser diode is a conventional GaAs/AlGaAs-double-hetero-structure grown by MOCVD. An n-AlGaAs cladding layer (thickness 1300 nm, 35% Al) is grown on a n-GaAs substrate followed by an undoped GaAs active region (thickness 90 nm). Next is a p-AlGaAs cladding layer (thickness 550 nm, 30% Al) with a highly doped p-GaAs cap layer (thickness 5 nm) on top. While in recent structures p-AlGaAs cladding layers with thickness of 700 nm and 900 nm were used, the thickness has been reduced to 550 nm in order to achieve an enhanced coupling between the laser light and the TE_0-surface mode. A first-order grating, which is holographically exposed in photoresist, is etched into the p-AlGaAs-top-cladding layer by ion-milling (grating period $\Lambda = 415$ nm, grating amplitude 100 nm). This etching technique has strongly improved the quality of the grating as compared to recent samples, where a wet-chemical etching process has been used. The evaporation of a semitransparent Au/Zn/Au metal stripe (50 Å/50 Å/200 Å) with a width of 12 µm oriented normal (x-direction) to the grating grooves (y-direction) defines the laser stripe. The single laser stripes are separated at a distance of 250 µm, the surface of the sample in between is isolated with polyimid. Ti-Au contact pads (500 Å/3000 Å), which overlap the laser stripe from both sides by 2 µm leaving a 8 µm wide window in the center of the laser stripe, are evaporated on the polyimid isolation. Next the laser stripe is spin-coated with photoresist (Hoechst AZ 6615, thickness 250 nm) forming a slab wave guide on top of the laser diode, which supports the TE_0-surface mode. Finally the laser bars are cleaved to a length between 400 µm and 600 µm.

Locally in the window the laser light is coupled to the TE_0-surface mode. In this experiment the window extends over the whole cavity length, while in recent experiments the window (length 200 – 300 µm) was only a part of the cavity length. This increases the coupling efficiency from the laser light to the surface mode. Part of the laser light is scattered from the active region via the surface grating into the waveguide. The light is propagating in the waveguide as a zig-zag-wave, where part of the zig-zag-wave is scattered into air into the emission angle α resulting in efficient surface emission. In addition, part of the zig-zag-wave is scattered back into the active region providing a positive, wavelength selective feedback process, which can result in a single-mode emission. These coupling mechanisms have been discussed in detail in Ref. [8].

The corresponding far-field pattern in DC-operation is shown in Fig. 2. The farfield pattern is measured by scanning the laser diode along the laser stripe (x-direction) from one cleaved facet to the other. The sample emits the light into a single beam in an emission angle of -55.35°. The beam divergence in x-direction is less than 0.15°, while the beam divergence in the direction normal (y-direction) to the laser stripe is 8°. The intensity emitted per solid angle into the single beam is more than 15 times higher than the edge emitted intensity per solid angle, which demonstrates the high efficiency of the SME-technique. Presently a power up to 3.6 mW is emitted into the single beam, which is 15 % of the totally emitted power of 24 mW.

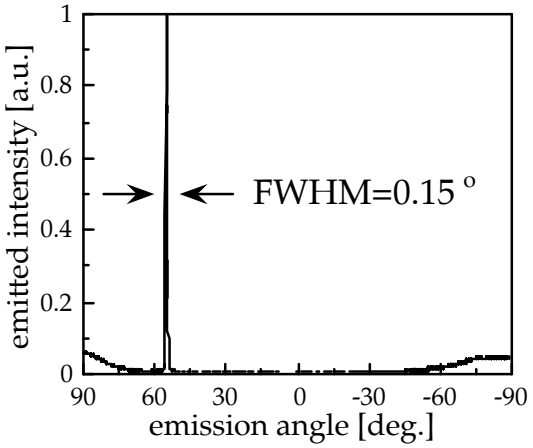

Fig. 2: The far-field pattern measured by scanning the laser diode along the laser stripe (x-direction) from one cleaved facet to the other. The SME-laser diode emits the light into a single beam in an emission angle of -55.35°. The beam divergence is less than 0.2°, a power up to 3.6 mW is emitted into this single, surface-emitted beam.

The SME-laser diodes show threshold current densities between 1.8 and 2 kA/cm^2. The wavelength emission spectrum of a SME-laser diode (threshold current I_{th} = 140 mA) in pulsed biased condition (pulse width 0.6 µsec, f = 40 kHz) at a current of 1.3 x I_{th} is shown in Fig. 3 (left). The sample shows a single-mode emission at λ = 874.08 nm with a full-width-half-maximum (FWHM) of 0.11 nm. The single-mode emission is maintained with increasing current, but the FWHM increases up to 0.17 nm at 1.6 x I_{th} and up to 0.27 nm at 1.8 x I_{th}. The right part of Fig. 3 shows the DC emission spectrum at a current of 205 mA. The laser diodes operates in a single-mode, the minimum linewidth achieved is 0.06 nm, the best side-mode-suppression-ratio is 24 dB.

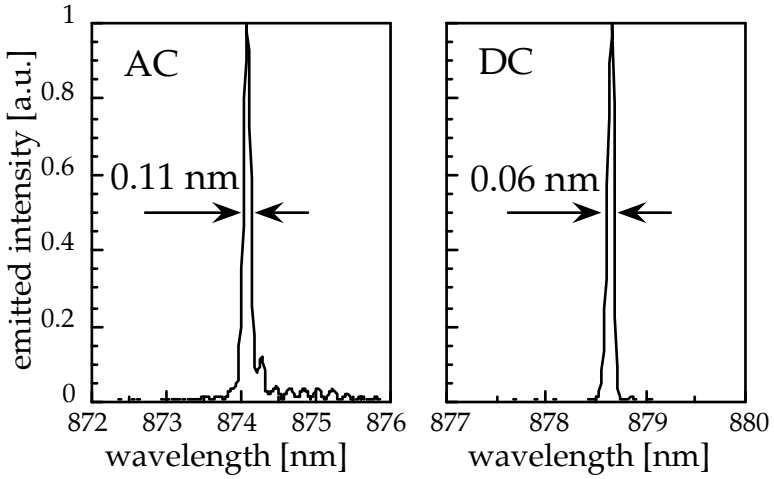

Fig. 3: Single-mode emission spectrum of a SME-laser diode in AC-condition (left) (pulse width 0.6 µsek, f = 40 kHz) at a current of 180 mA (= 1.3 x I_{th}) and in DC-operation at a current of 205 mA (right).

3. Discussion and Conclusion

The main advantage of the SME-type of laser diode as compared to surface emitting DBR- or DFB-laser diodes is a simple and flexible fabrication process. It utilizes the well-established technique of the conventional striped laser and requires no regrowth. The present performance of the SME-type of laser diode (relatively high threshold current densities (1.8 – 2 kA/cm^2), low output power) can be optimized by mirror-coatings: High-reflection mirrors on the cleaved facets will both decrease the threshold current density as well as increase the surface emitted power. The use of a quantum-well structure as active region instead of the double-hetero-structure should further decrease the threshold current density.

As has already been demonstrated [9], the emission wavelength (and so the emission angle) can be adjusted by the waveguide thickness and depends on the refractive index of the waveguide. This makes the SME-type of laser diode very suitable to be employed in practical applications: On one hand wavelength-division-multiplexing (WDM) techniques require on the transmitter side arrays of single-mode laser diodes, which emit at different, well-defined wavelengths. On the other hand WDM requires wavelength-tunable laser diodes on the receiver side for the heterodyne-detection-scheme [10]. The fabrication of laser bars containing laser diodes emitting at well-defined, different wavelengths (wavelength spacing $\Delta\lambda \sim 0.5 – 3$ nm) can be realized by processing adjacent SME-laser diodes with slightly different waveguide thickness ($\Delta d \sim 2 – 5$ nm). The use of an electro-optically active polymer, for example, as waveguide material will allow a continuous change of the waveguide's refractive index by applying an electric field across the waveguide. This would result in a continuous wavelength-tuning around a central wavelength primarily defined by the waveguide thickness. Thus SME-laser diodes have the potential to achieve both WDM-requirements. Therefore it is essential to apply the SME-technique to laser diodes operating in the 1.3 µm- and 1.5 µm-wavelength regime.

In addition due to their high beam quality, surface emitting SME-laser diodes can be employed as direct optical interconnects. For this specific application the steering of the surface emitted beam by tuning the emission wavelength is of high importance.

Acknowledgments

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Recent Developments in Femtosecond Technology

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The availability of ultrabroad-band sub-10 fs optical pulses from Ti:sapphire laser oscillators allows 0.1 TW-scale pulse generation from compact kHz-rate amplifiers. The amplified sub-20 fs pulses can be compressed below 5 fs using novel techniques for self-phase modulation and dispersive compression. The resultant high-power light pulses comprising less than two oscillation cycles within their intensity-FWHM open up new possibilities in strong-field physics including the study of reversible nonlinear optical processes in solids beyond the 10^{14} W/cm^2 intensity level.

Despite the unmatched results in extreme ultrashort pulse generation with Ti:sapphire since a few years alternative laser materials are under investigation in order to achieve an all-solid-state laser design. The generation of 14 fs pulses from a KLM-modelocked Cr:LiSAF (60 mW average output power) and a similar Cr:LiSGaF laser (100 mW) is reported representing the shortest femtosecond pulses with the highest average power ever produced out of Cr-doped colquiriite laser crystal oscillators.

1. Introduction

The development of novel broadband solid-state laser materials along with concomitant advances in ultrafast all-optical amplitude modulation techniques has resulted in the emergence of a new generation of femtosecond sources over the last few years. Titanium-doped sapphire has been the most successful gain medium among a number of vibronic solid-state laser materials because of its broad bandwidth (approximately 200 nm FWHM centered at 800 nm) and excellent mechanical and thermal characteristics [1]. The discovery of Kerr-lens mode locking (KLM) [2] and novel means of intracavity dispersion control [3] have opened the way to an efficient exploitation of the enormous optical bandwidth of Ti:sapphire for ultrashort pulse generation.

Soon after the first dispersion-controlled KLM Ti:sapphire lasers had been put into operation it was recognized that system performance critically depends on the bandwidth $\Delta\nu_{GDD}$ over which the overall (negative) cavity group delay dispersion (GDD) is approximately constant [4], [5]. This finding led to the development of Ti:sappire oscillators using fused silica prisms [6] introducing the lowest cubic phase dispersion and allowing sechant-hyperbolic-shaped pulses down to 15 fs in duration. Further pulse shortening could be made possible by employing aperiodic (chirped) multilayer dielectric mirrors for intracavity dispersion control [3]. Specifically designed chirped mirrors have been capable of introducing a nearly constant negative GDD over a wavelength range significantly exceeding the largest $\Delta\nu_{GDD}$ achievable with prisms. As a result, mirror-dispersion-controlled (MDC) Ti:sapphire lasers can produce high-quality nearly-

transform-limited pulses down to 7.5 fs in duration [7] (Fig. 1). The spectrum of these pulses can be centered at 790 nm with a time-bandwidth product of ≈0,4. The use of dispersion engineered mirrors instead of prisms for GDD control also improves compactness and the reproducibility of system performance. This is because in MDC systems the net intracavity GDD (and hence pulse duration) is insensitive to resonator alignment, in strong contrast to prism-controlled systems.

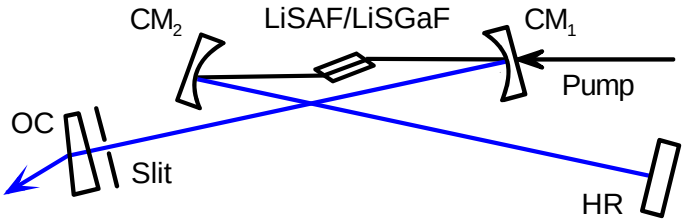

Fig. 1: Typical setup of a MDC femtosecond oscillator

When pursuing the ultimate goal of a really compact all-solid-state femtosecond laser system direct diode pumping of the laser material is a challenge. Thus, during the last years several Cr-doped colquiriite crystals like LiCAF, LiSAF, LiSGaF and others being known already since longer time [8], [9] have invoked new interest because of the availability of new red (670 nm) high power (~500 mW) laser diodes. The insights of optimum laser resonator design for the Ti:sapphire laser have been transferred successfully to the Cr-doped lasers by a number of authors [10] – [13] yielding so far only pulses in the 40-fs region as long as usable average output power is considered to be an essential feature (>50 mW).

Chirped mirrors as they have been developed for the Ti:sapphire laser proved to be too lossy for resonators containing the lower gain Cr-doped media. Hence, dielectric Gires-Tournois mirrors (GTM) have been developed causing lower losses due to a smaller penetration depth of the radiation within the structure. Their GDD is relatively high and adjustable but highly nonlinear hardly allowing to break the 40-fs pulse limit. Only recently, new dielectric materials and further optimized layer sequences allowed to create chirped mirrors which could be employed as straightforward as in the Ti:sapphire lasers [14] yielding pulse durations in the sub-20 fs regime at reasonable average powers as it will be reported later in more detail.

The present sub-10 fs MDC-KLM Ti:sapphire oscillators are ideally suited for seeding high-power femtosecond amplifier systems. The extremely broad bandwidth (≈120 nm) of the emitted sub-10 fs pulses centered at the gain peak of Ti:sapphire allows the implementation of chirped-pulse amplification (CPA) in a fairly simple and compact system. This is because, due to their ultrabroad bandwidth, the seed pulses can be substantially broadened by introducing a relatively small amount of GDD. In fact, the pulse duration increases to several picoseconds upon passage through the usual system components used for isolation and pulse selection. Additional broadening up to tens of picoseconds can be readily induced by introducing a piece of highly dispersive SF57 glass (Schott) without adding notable complexity. In the following, it will be depicted how 5 fs pulses could be generated by further amplification and an optimized pulse compression technique.

2. Sub-TW Pulse Generation

The pulse energy can be boosted beyond the millijoule level in a single-stage 8-pass "bow-tie" amplifier without excessive nonlinearities emerging in the amplifier crystal. Owing to the moderate amount of positive GDD to be compensated for, pulse recompression following amplification by a simple and high-throughput (≈80 %) double-prism sequence. The residual high-order phase dispersion of the system (up to fourth order) is eliminated by specially designed chirped mirrors. The absence of an extra pulse stretcher and lossy diffraction gratings significantly reduces system complexity and (indirectly) gain narrowing, respectively, as compared to conventional CPA systems. The described system currently produces 20 fs pulses beyond the millijoule level at a repetition rate of 1 kHz [15]. This performance comes in combination with excellent stability, pulse energy fluctuations are less than $\pm$3 %.

The high-power 20 fs pulses can be uniformly self-phase modulated across the beam profile in a microcapillary filled with some noble gas, as recently proposed and demonstrated (with 140 fs seed pulses) by M. Nisoli, S. DeSilvestri, and O. Svelto [16]. Suitable choice of the nonlinear medium (Kr, Ar, Ne, etc.), the channel diameter of the fused silica capillary, the length of the hollow waveguide, and the pressure of the noble gas allows controlling spectral broadening and the output beam profile. The pulses exiting the waveguide are propagated through an ultrabroad-band high-throughput dispersive system providing nearly optimum chirp compensation over the wavelength range of 650 – 950 nm [17]. Key components of the dispersive delay line include AR-coated thin fused silica wedged plates and chirped mirrors designed and manufactured by R. Szipöcs and K. Ferencz at the Research Institute for Solid State Physics in Budapest (Hungary). This compressor currently delivers 0.25 mJ, 5 fs pulses, which are focusable to intensities beyond 10^{17} W/cm^2 representing the world's shortest optical pulses.

The entire setup consisting of the MDC oscillator, multipass amplifier, recompression stage, and pump sources occupies an area of approximately 2 m^2 on the optical table. This compactness combined with the ruggedness and reliability of solid-state components make this system a versatile tool for a broad range of experiments in nonlinear optics and related fields. Furthermore, the unique performance described above holds out the promise of pushing the limits of nonlinear optics.

3. Prismless Cr:LiSAF and Cr:LiSGaF Lasers

It was a great challenge to improve the technology of dielectric chirped mirrors so as to make them suitable for LiSAF and LiSGaF lasers. New types of low loss chirped mirrors have been developed at the above mentioned Solid-State Physics Institute, Budapest, involving new dielectric layer materials with different steps of the index of refraction. New algorithms allowed further optimization of the dispersion properties, both aspects currently being filed for patent.

In this paper, we report the shortest, to our knowledge, pulses obtained in MDC-modelocked Cr:LiSAF and Cr:LiSGaF lasers of a duration of 14 fs at the substantial output power for Cr-lasers of 100 mW at 1.6 W incident 647 nm power.

Having optimized the net intracavity GDD by taking the measured dispersion data for LiSAF and LiSGaF crystals into account, a most simple and compact resonator design has been realized. The cavity is a standard X-cavity, consisting of only two curved (R = 100 mm) dispersive mirrors, the active medium, a high reflector end mirror and an out-

put coupler varying from 0.4 to 2.3 %. The Cr:LiSAF crystal used had a length of 2.8 mm and 0.8 % Cr content, the Cr:LiSGaF crystal was 4 mm long with 0.75 % of Cr. The implemented dispersive mirrors exhibited a maximum GDD of ≈80 fs^2 (Fig. 2).

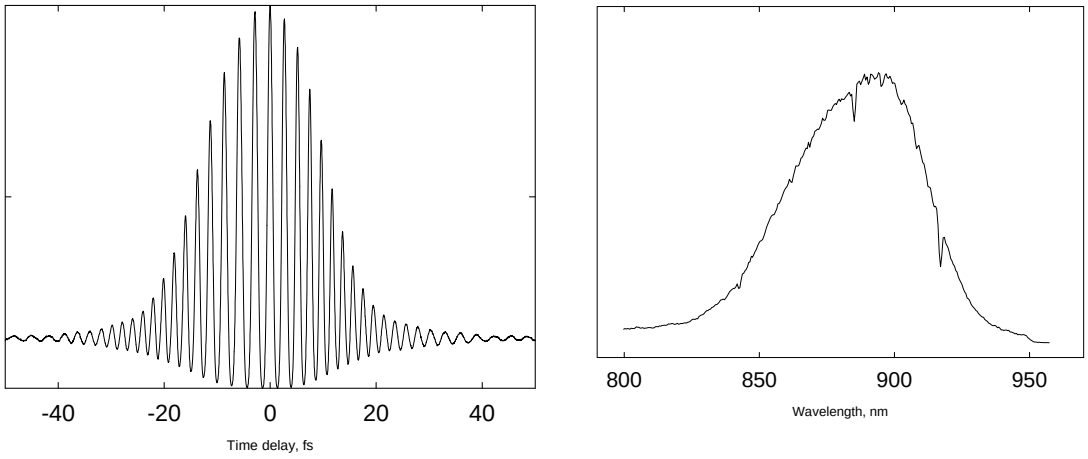

Fig. 2: Interferometric autocorrelation trace and spectrum of the shortest pulses out of a Cr-doped laser

The autocorrelation trace and the measured spectrum of the mode-locked laser pulses centered around λ = 880 nm and having a bandwidth FWHM of 70 nm allow to calculate a duration of 14 fs and a time-bandwidth product $\Delta\tau\Delta\nu$ = 0.32 using a $sech^2$ pulse shape fit indicating nearly transform limited pulse quality.

As a next step efficient diode pumping of this oscillator will be realized involving at least 4 of the presently available moderate power AlGaInAs array diodes emitting ~500 mW. After this is realized the Cr-doped colquiriite laser could be an interesting more compact alternative for some applications to the well established Ti:sappire femtosecond laser oscillator.

4. Conclusion

In conclusion, we demonstrated the first successful realization of 5 fs (< 2 optical cycles) laser pulses of 0.25 mJ energy via compression of amplified pulses originating from a MDC Ti:sappire oscillator and being self-phase modulated in a microcapillary. These pulses are focusable to intensities beyond 10^{17} W/m^2 and may be capable of pushing the current limit of coherent X-ray generation by laboratory scale experiments to shorter wavelengths than 6 nm reaching the important water window.

Furthermore, we showed what is to our knowledge the first generation of nearly transform-limited 14 fs pulses from prismless KLM Cr:LiSAF and Cr:LiSGaF lasers having average powers of up to 100 mW. The laser setup is characterized by extreme compactness, comprising only two dispersive mirrors, replacing conventional cavity mirrors, giving rise to high stability of the mode-locked operation.

Acknowledgment

This work was a joint project of two groups (F. Krausz and E. Wintner) at the above mentioned institute supported by the Austrian National Science Foundation Projects P 10409 and P 10733, the Austrian National Bank Projects No 6026 and 5847, and by the Gesellschaft für Mikroelektronik.

The 5 fs compression experiment has been performed in collaboration with M. Nisoli, S. DeSilvestri and O. Svelto from the Politechnico Milano (Italy). The cooperation with R. Szipöcs and K. Ferencz from the Research Institute for Solid-State Physics in Budapest (Hungary) for the development of the different versions of chirped mirrors is gratefully acknowledged. We also would like to thank the suppliers of the LiSAF and LiSGaF crystals, A. Cassanho of VLOC, Tarpon Springs, and H.P. Jenssen, University of Central Florida, Orlando, Florida for their support.

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Rastersondenmikroskopie und -Spektroskopie an Halbleiteroberflächen und Bauelementen: Von der Grundlagenforschung zu industriellen Anwendungen

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Die Entwicklung verschiedener Verfahren der Rastersondenmikroskopie und -spektroskopie [1] hat sowohl einen neuen Zugang zur Physik auf der Nanometerskala eröffnet als auch neue Wege bei der Charakterisierung von Halbleiterbauelementen erschlossen [2]. Während die Rastertunnelmikroskopie/-spektroskopie Informationen über die elektronischen Eigenschaften von Halbleiteroberflächen bis hin zur atomaren Skala liefert, ist besonders in jüngster Zeit die Rasterkapazitätsmikroskopie/-spektroskopie zur Untersuchung elektronischer Eigenschaften von Halbleiterbauelementen im Submikrometerbereich ins Zentrum des Interesses gerückt [3], [4]. Eine weitere wichtige Methode zur Untersuchung der lokalen optischen Eigenschaften ist die nahfeldoptische Mikroskopie und Spektroskopie, welche heutzutage verstärkt mit einer Reihe kraftmikroskopischer Betriebsarten kombiniert wird. Die Rasterkraftmikroskopie und -spektroskopie leistet ferner wichtige Beiträge zur Optimierung mikromechanischer Bauelemente bezüglich Reibung, Abrieb und Verschleiß.

Ziel dieses Vortrags ist es, die breiten Anwendungsgebiete der Rastersondenmethoden — von der atomaufgelösten Spektroskopie bis hin zur Bauelement-Qualitätskontrolle — darzustellen. Dabei werden auch die sehr unterschiedlichen instrumentellen Voraussetzungen für die Grundlagenforschung einerseits und die industriellen Anwendungen andererseits angesprochen.

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Ballistic Electron Spectroscopy of Semiconductor Heterostructures

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We present a study of ballistic electron transport in GaAs/GaAlAs with different well widths under given bias conditions. A three terminal device is used to inject an energy tunable electron beam via a tunneling barrier into an undoped superlattice and to collect the transmitted current as a function of the injection energy. Significant increase of the collector current is observed due to miniband conduction in the superlattice. Due to the localization of the electron wave function in biased superlattices, the quasi-continuous miniband breaks up into a ladder of discrete Wannier Stark states. The results are compared to calculations based on an envelope function approximation using a transfer matrix method. In order to resolve the discrete Wannier Stark states, a Four Terminal Device (FTD) is designed.

1. Introduction

Decreasing the barrier thickness of multiple quantum well structures leads to a stronger coupling between the degenerate eigenstates in the wells and thus to the formation of superlattice (SL) minibands. For these strongly coupled quantum wells the electronic states are extended. Applying an electric field in the direction perpendicular to the layer planes leads to a reduction of the interwell coupling and localizes the electronic states into a finite number of periods. This splitting of the quasi-continuous miniband into a ladder of discrete Wannier Stark states has direct consequences on the ballistic electron transport properties.

A hot electron transistor [1] is used to probe the superlattice transmittance. In such three terminal devices, an energy tunable electron beam is generated by a tunneling barrier, passes the superlattice after traversing a thin highly doped GaAs (base) and an undoped drift region. Having the possibility to drive the injected current and the electric field applied to the superlattice independently, the transmittance can be measured directly at given superlattice biases. The probability for an injected hot electron to cross the superlattice reflects the transmittance of the miniband and can be considered to be proportional to the measured transfer ratio $\alpha = I_C/I_E$.

2. Device Fabrication

Our samples, grown by molecular beam epitaxy (MBE), have the following common features: A highly doped n^+-GaAs collector contact layer ($n = 1x10^{18}$ cm^{-3}) is grown on a semiinsulating GaAs substrate. Followed by a superlattice and the drift regions which are slightly n-doped (~$5x10^{14}$ cm^{-3}), in order to avoid undesired band bending. To reduce quantum mechanical confining effects originating from the quantum well formed by the emitter barrier and the superlattice the drift region is chosen to be at least 200 nm in width. This is followed by a highly doped ($2x10^{18}$ cm^{-3}) n^+-GaAs layer (base) of

13 nm width. As found in previous experiments [2], about 75% of the injected electrons traverse the base ballistically. On top of the base layer a 13 nm undoped $Ga_{0.7}Al_{0.3}As$ barrier is grown followed by a spacer and an n^+-GaAs layer, nominally doped to $n = 3x10^{17}$ cm^{-3}, in order to achieve an estimated normal energy distribution of injected electrons of about 15 meV [3]. It should be noted that the half width of the injected electron beam limits the energy resolution of the experiment. Finally, an n^+-GaAs contact layer ($n = 1x10^{18}$ cm^{-3}) is grown on top of the heterostructure to form the emitter. Four different superlattices have been studied with $Ga_{0.7}Al_{0.3}As$ barriers (2.5 nm) and GaAs wells, with varying widths (6.5 nm, 8.5 nm, and 15 nm) and periods (see table 1).

sample #	well (nm)	periods	Δ_{01}(meV)	Δ_{MB1}(meV)	Δ_{12}(meV)	Δ_{MB2}(meV)
1	6.5	5	46	22	114	94
2	8.5	5	33	13	85	53
3	15	5	14.5	3.5	40	14
4	6.5	10	46	22	114	94

Table 1: Summary of the superlattice tunneling structures investigated. Δ_{MB1} and Δ_{MB2} denote the widths of the first and of the second miniband, Δ_{01} the energy position of the first miniband with respect to the conduction band edge and Δ_{12} denotes the width of the minigap between the first and the second miniband.

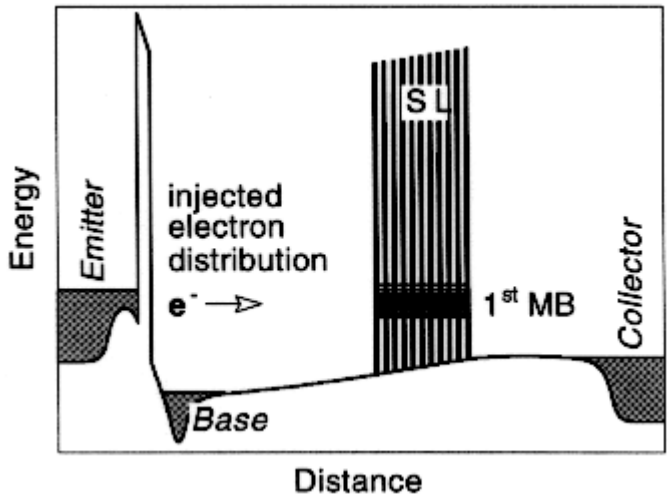

Fig. 1: Conduction band diagram under typical bias conditions.

The fabrication of the three terminal device includes the following steps: $SiCl_4/SF_6$ reactive ion etching (RIE), unselective etching to the collector layer, metallization of the AuGeNi ohmic contacts, Si_3N_4 isolation of the emitter mesa (PECVD), and finally the metallization of the CrAu bonding pads. More details can be found elsewhere [4].

The spatial profile of the bottom of the conduction band along the growth direction under typical bias conditions, as calculated by a Poisson solver, is shown in Fig. 1. All measurements are done in common base configuration at 4.2 K.

3. Results and Discussion

3.1. Unbiased Superlattices

Under flat band conditions the eigenstates of the periodic structure are expected to be extended over the entire length of the superlattice. Using the concept of a hot electron transistor the transmittance of an undoped field free superlattice, grown in the drift region between base and collector, is measured directly. To investigate the superlattice properties and to confirm the results of the measured transfer ratio $\alpha = I_C/I_E$, three superlattice structures with different well widths are measured.

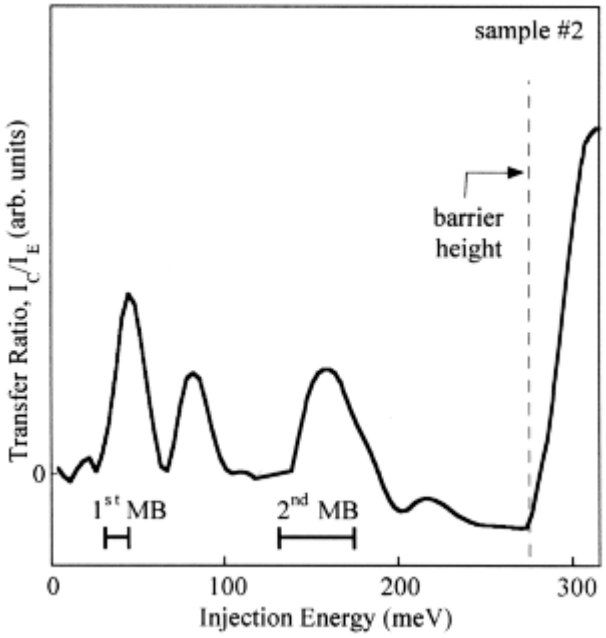

Fig. 2: The transfer ratio $\alpha = I_C/I_E$ versus injection energy ($\approx e.U_{EB}$) of sample #2. The calculated miniband positions are indicated by bars (⊢——⊣).

The static transfer ratio of sample 2, $\alpha = I_C/I_E$, plotted in Fig. 2 as a function of the injection energy, shows several maxima and a sharp rise at 280 meV. No current is observed below the energy of the first peak. The position of the first peak coincides very well with the first miniband. Thus, we claim that the first peak is due to miniband transport through the lowest miniband. For energies higher than the first miniband the transfer ratio drops quite significantly since there is no transport possible through the forbidden minigap of the SL. The second observed peak is shifted 36 meV to higher injection energies and is ascribed to the first LO-phonon emission replica ($\hbar\omega_{LO}$ = 36 meV) of the injected electron distribution. The relative position in energy and width are equal to that of the first peak. The energy range of electrons injected at voltages corresponding to this second peak is in the forbidden band and no contribution is expected from electrons which have not lost energy due to optical phonon emission. The peak at 150 meV represents transport through the second SL miniband. For an analysis of the observed features we compare the experimental data with the theoretically calculated miniband positions. The calculated positions and widths of the first and second miniband are indicated by bars. The sharp rise of the transfer ratio at 280 meV is due to the

transition to continuum. This energy, which corresponds to the conduction band offset of the superlattice barriers, gives us a confirmation of the AlAs mole fraction of the AlGaAs compound.

In Fig. 3 we show the transfer ratio α as a function of the injection energy for three samples with different well widths at lower injection energies. There is a clear shift of the peaks to higher energies with decreasing superlattice well width. The calculated miniband positions are again indicated by bars as in Fig. 2. It can be seen that the tunneling data agree very well with the self constant solution of the Schroedinger equation. Note that it is possible to resolve even very narrow minibands at low energies as seen for sample 3.

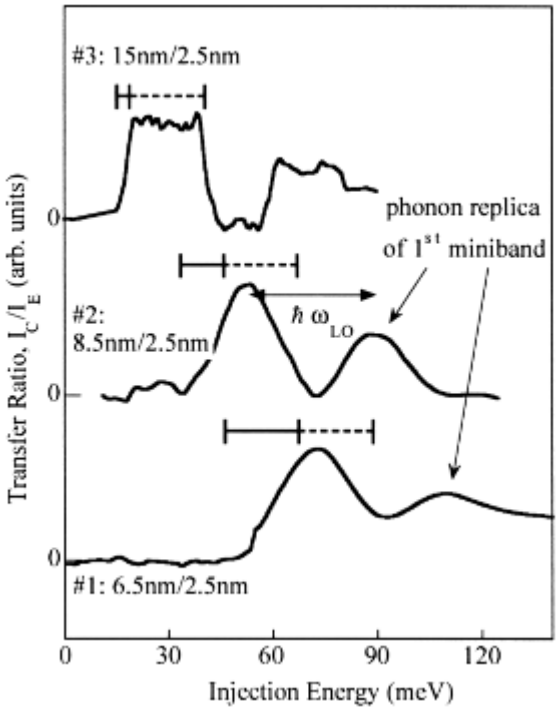

Fig. 3: Transfer ratio α versus injection energy for all three samples (├──┤ indicates the calculated miniband position, ├ − ┤ indicates the broadening due to the energy distribution of the injected electron beam). A double arrow represents the energy of a longitudinal optical phonon ($\hbar\omega_{LO}$ = 36 meV).

Due to the broadened energy distribution of the injected electrons, the peaks corresponding to ballistic transfer through the first miniband are broadened as well. The shape of the energy distribution is investigated using a three terminal device with a resonant tunneling diode grown in the drift region which acts as an energy filter of the injected electrons [5], [6]. Thus we are able to measure directly the injected normal energy distribution. It can be seen that this energy distribution is not symmetric and the broadening takes place mainly at the low energy side. This low energy tail of the injected electron beam is indicated by dashed bars in Fig. 3.

3.2. Biased Superlattices — Breakdown of the Extended Electron Wave Function

The splitting of minibands in biased superlattices has direct consequences on the ballistic electron transport properties. Due to the localization of the electron wave function, the quasi-continuous miniband breaks up into a ladder of discrete Wannier-Stark states [7].

The transfer ratio of a biased 10 period superlattice (sample 4) was studied and compared with a theoretical transfer matrix calculation. The structure under investigation is except the number of periods similar to the structure described above.

The measured transfer ratio α as a function of the normal electron injection energy at different collector-base biases is shown in Fig. 4. It can be seen that the onset of the transfer ratio shifts with the applied collector-base bias since the lower edge of the first miniband shifts with the superlattice bias. The observed transfer ratio decreases quit dramatically with the applied electric field. Longitudinal optical phonon replicas, which are shifted 36 meV to higher injection energies, can be observed at all biases.

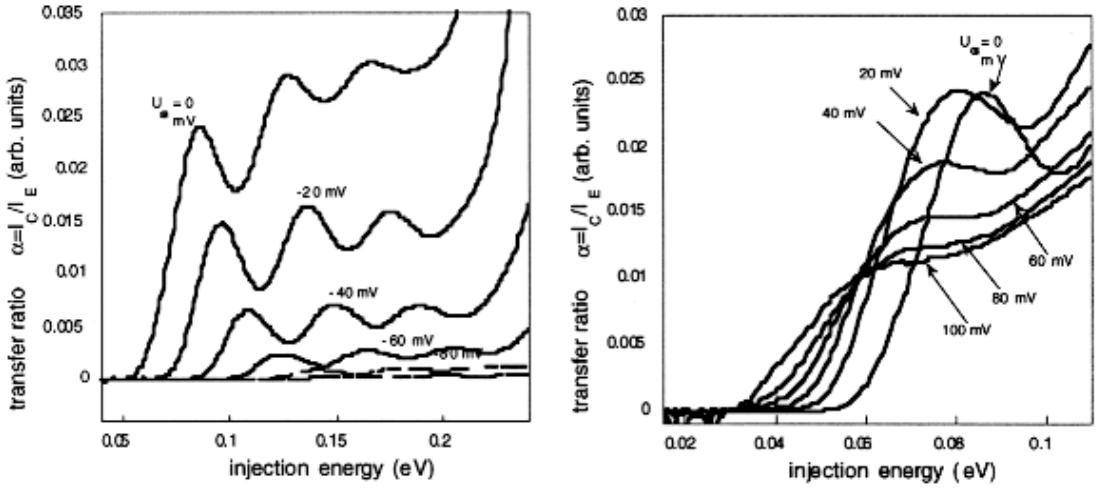

Fig. 4: Measured transfer ratios at different collector-base bias vs. injection energies

Figure 5 shows the transfer ratio at peak position of the investigated superlattice versus applied electric field. The maximum transmission can be observed at zero bias voltage, since all superlattice states are extended over the total superlattice dimension. Applying an electric field leads to a decrease of the transmission due to the localization of the lowest and uppermost superlattice states i.e. these states do not contribute to the ballistic transport any more. The transfer ratio of the superlattice vanishes for an applied electric field of about 5 kV/cm. This is in good agreement with the simple estimate of the localization length $\lambda \approx \Delta/eF$ (Δ is the miniband width, and F the applied electric field) which decreases to about half of the total superlattice length at this bias.

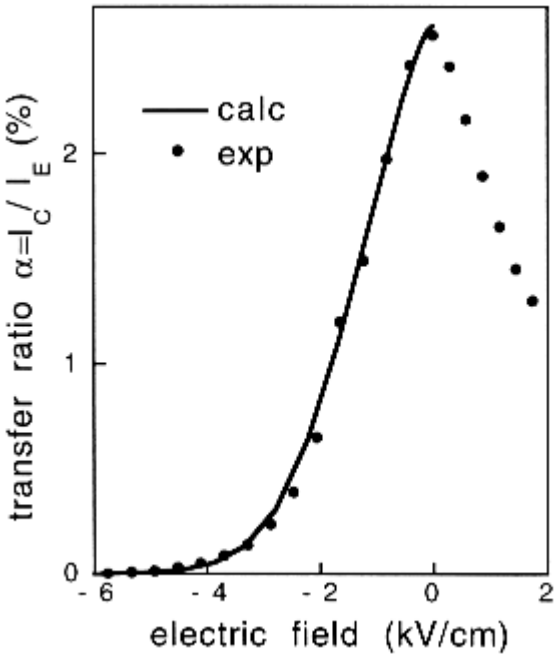

Fig. 5: Measured (dots) and calculated (line) transfer ratio vs. electric field.

In addition, we perform theoretical calculations based on a transfer matrix method using an envelope function approximation [8]. The solid line in Fig. 5 shows the result of such calculation for the measured structure. We find an excellent agreement between our experimental results and the quantitative theoretical prediction.

For the first time, the miniband positions, widths, and the collapse of the superlattice states under the influence of an applied electrical field using the technique of hot electron spectroscopy is observed directly.

3.3. Four Terminal Device (FTD)-Detection of Plasmon Emission

A new four terminal device is developed including a resonant tunneling diode as an injector in order to decrease the width of the injected electron distribution. As the resonant condition of the injector resonant tunneling diode is set, we are able to tune the injected sharp electron beam. This device is used to observe directly the relaxation of hot carriers via plasmon emission in a low doped ($n = 3x10^{17}$ cm^{-3}) GaAs drift region which is contacted to the ground in order to avoid undesired charging in this drift region.

In between this low doped drift region and the collector an analyzer resonant tunneling diode is grown. A SEM picture of the device is shown in Fig. 6. A schematic sketch of the band diagram is shown in the inset of the figure. The four terminal device is also being considered as a structure which allows the possibility to set up conditions for the beam plasma instability leading to local oscillations of charge densities and consequently to an emission of radiation in the THz range.

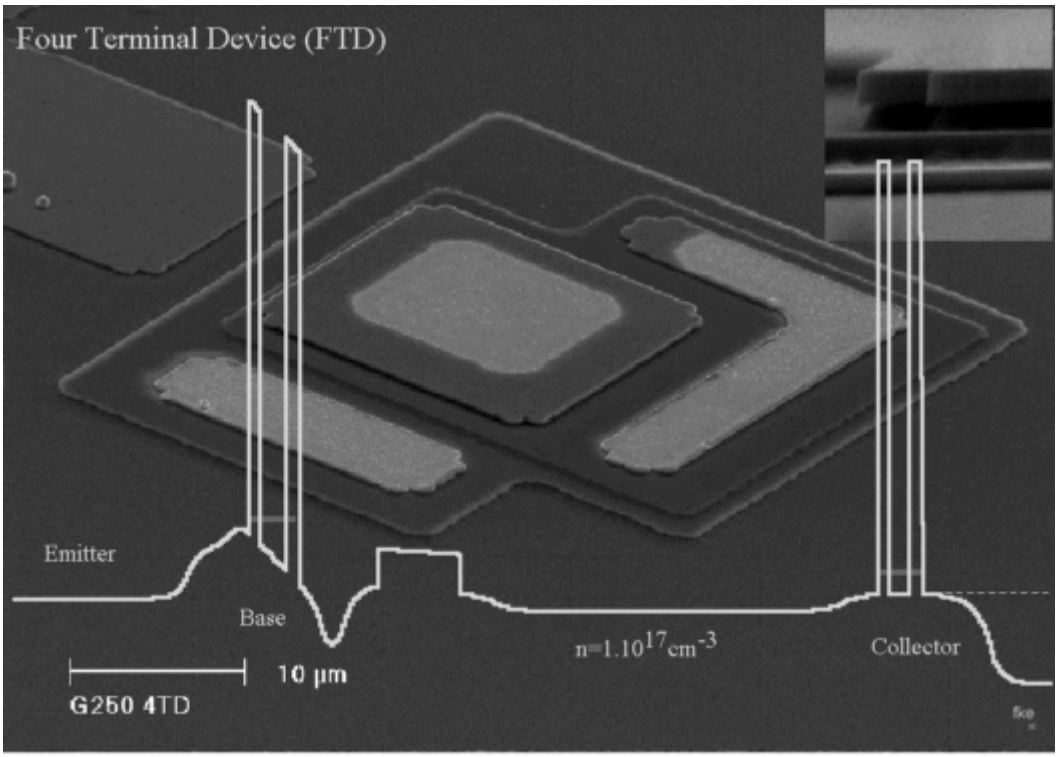

Fig. 6: SEM picture of the Four Terminal Device (FTD). The inset shows the conduction band structure.

In addition the four terminal device design is used to resolve the single Stark states of a short period superlattice, since the injected electron distribution is much narrower than the spacing between the single states.

4. Conclusion

In summary, direct experimental current spectroscopy of minibands in undoped superlattices is demonstrated using the technique of hot electron spectroscopy. Miniband widths and gaps of different unbiased superlattices are investigated and compared to the results of a self-consistent Schroedinger calculation. Applying an electric field to the superlattice the quasi-continuous miniband splits up into a discrete ladder of Stark states, and consequently the transmission of ballistic electrons decreases. The measured transfer ratio at different bias conditions is in excellent agreement to the theoretical calculation based on a transfer matrix method using an envelope function approximation. For the first time, the collapse of the superlattice electron states under the influence of an electrical field is observed directly in transport.

In order to increase the resolution of the experiment and in order to measure the relaxation of hot carriers via plasmon emission, a four terminal device (FTD) is designed and fabricated.

Acknowledgment

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Backside-Laserprober Technique for Characterization of Semiconductor Power Devices

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An infrared laserprobe technique for the characterization of the self-heating in the µs range in power VDMOSFETs and IGBTs is presented. Based on the thermo-optical effect in silicon, this technique detects interferometrically the temperature induced changes of the silicon refractive index. The time evolution of the lattice temperature in the device active region is studied for the power devices biased under shorted load conditions. Optical experiments are combined with electro-thermal device modeling and electrical characterization. From the calculated phase modulation signals fitted to the experiments a value for temperature coefficient of the refractive index of $1.6 \cdot 10^{-4}$ K^{-1} is found which is in good agreement with the literature.

1. Introduction

The steady increase of the switching frequency of power semiconductor devices under high voltage and current conditions causes transient thermal effects to become a more severe and critical issue. Although much attention has been given to thermal effects in power devices, there are so far no experimental techniques available for a time-resolved analysis of destructive thermal effects in dynamic device operation. In this paper we present the application of the backside laserprobe technique [1] to analyze the transient heating in power Vertical Double-diffused (VD)MOSFETs and in Insulated Gate Bipolar Transistors (IGBTs) biased under shorted load conditions.

2. Optical Technique

The principle of the laserprober set-up is demonstrated in Fig. 1. An increase in the refractive index of silicon due to the lattice heating (thermo-optical effect) in dynamic device operation modulates the phase of the laser probing beam. The probing beam reflected from the gate and a reference beam reflected from the drain metallization interfere in a photodetector. The electrical signal at the detector corresponding to the thermally induced phase change is recorded and averaged by a digital oscilloscope. Since the photon energy of the laser beam (λ = 1.3µm) is below the energy gap of silicon, the optical measurements have no impact on the device electrical characteristics.

The laserprobe measurements were performed on commercially available VDMOSFETs of 150 V and 200 V breakdown voltage, and on IGBTs with 1200 V breakdown voltage. In VDMOSFETs, optical access through the drain contact is obtained after mechanical removal of the original contact metallization, polishing the substrate and evaporation of a thin Ti-Au film leaving a small square window opened. This preparation does not

change the device performance, but induces a small drain contact resistance. For measurements on IGBTs, the device preparation is different as mechanical contact removal would also destroy the p^+-anode layer of the IGBT. We have therefore developed a process technique which allows selective etching of the small window (100 µm x 100 µm) into the contact metallization. The etching stops just at the silicon surface (Fig. 1) which ensures the proper functionality of the device.

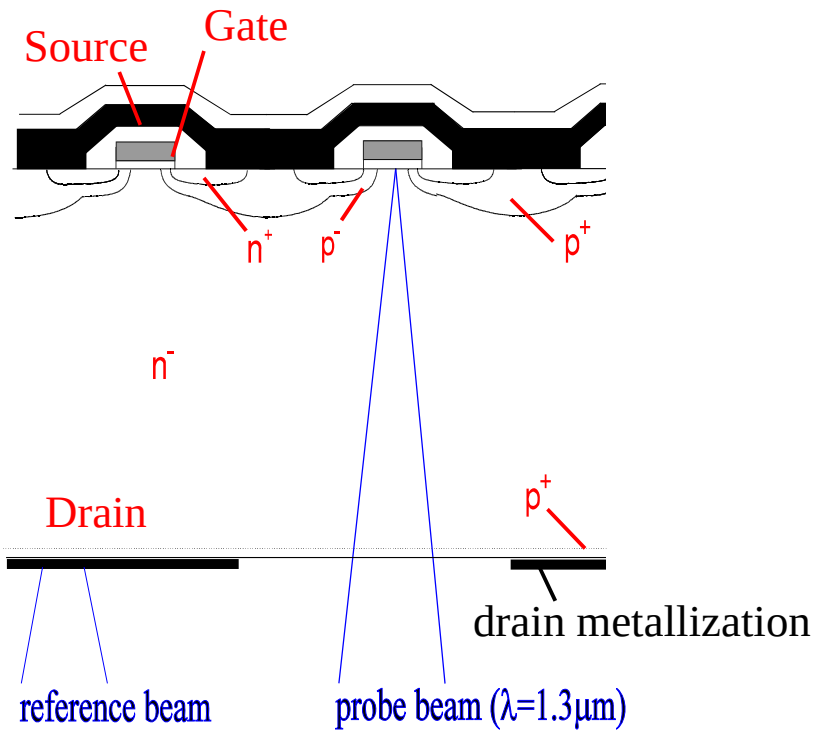

Fig. 1: Laserprobe method for the detection of the transient lattice heating in power devices. The probing laser beam (beam diameter of 8 µm) is focused through a small window in the drain contact on a single IGBT (or VDMOSFET) cell and is reflected from the polysilicon gate. The interferometer reference beam is placed at the metallization.

3. Experiments

In the experiments on VDMOSFETs, the amount of the transient lattice heating is controlled by applying pulses with different pulse levels from V_{GS} = 0 V to 8 V and 12 V and different pulse widths τ_H (5 µs to 60 µs) to the gate. The drain-to-source bias is held constant at V_{DS} = 15V. The transient drain current is monitored by a voltage drop across a resistor connected in series with the drain. The power dissipation in IGBTs is controlled by the drain-to-source voltage ranging from 50 V to 400 V. The device is switched by gate pulses of 15 V height and length of 10 µs. Here the transient current is measured inductively by means of a current probe. In both cases the pulse repetition frequency is chosen to 10 Hz, in order to enable total device cooling between subsequent pulses. Figure 2 shows typical results for the transient phase signal obtained from laserprobe experiments on VDMOSFET and IGBT. During the heating the phase signal increase is linear in time. After heating turn-off, the phase signal remains almost con-

stant in the first 100 µs. In that case, the peak temperature decreases and simultaneously, the heat propagates into the silicon well. Therefore, the length where the temperature changes (the beam modulation length) increases. As the phase change is proportional to the integral of the temperature increase along the beam modulation length, the resulting phase signal is nearly constant.

Besides the thermo-optical effect, the phase of the laser beam is also modulated due to the free-carrier effect [2]. We have found that this effect can be neglected both in VDMOSFETs and IGBTs. Performing optical measurements on VDMOSFETs with V_{DS} = 0 V and applying pulses to the gate (no device heating), the resulting phase signal is close to the detection limit of the measurement set-up. A similar experiment has been carried out on IGBT with a drain-to-source voltage of V_{DS} = 2 V. Even under this low power condition the thermally induced phase signal dominates and superimposes the free-carrier signal.

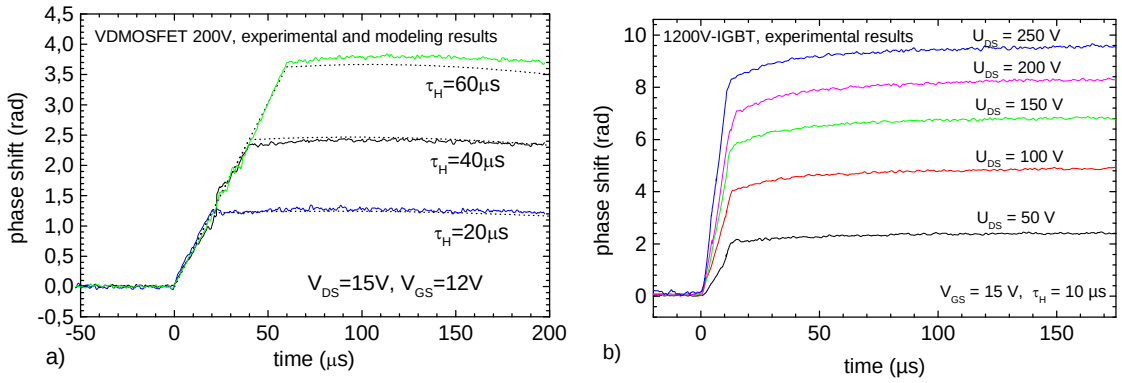

Fig. 2: Laser-probe measurement results for the time-resolved phase shift on a) 200V-VDMOSFET and b) 1200V-IGBT. Pulse widths τ_H are indicated. The phase shift calculated for a value of the temperature coefficient of the refractive index of $dn/dT = 1.6 \cdot 10^{-4}\ K^{-1}$ of silicon is shown for VDMOSFET device (dotted-line).

4. Numerical Modeling

The study of time dependence of the temperature in power devices requires modeling of the total chip consisting of several hundred cells including the chip package. To reduce the complexity of the model, we first analyzed the temperature distribution in a single VDMOSFET cell. The electrical characteristics of a single cell are calculated by a modified version of MINIMOS 6 [3]. The transient temperature profile is then obtained by numerically solving the 2-D heat conduction equation. The temperature distribution along the wafer depth (Fig. 3) at the center of the chip area is taken as input for modeling of the laser beam modulation.

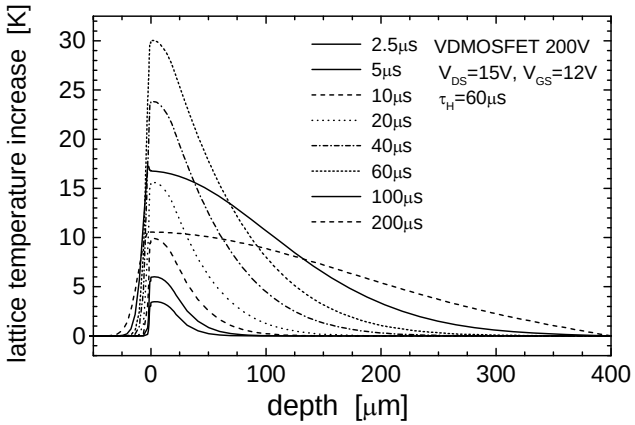

Fig. 3: Numerical modeling result of the transient temperature profile across the chip center (200V VDMOSFET).

The transient phase modulation signals are calculated by the application of the transmission-line model presented in [4], which has been extended including the lattice heating. The phase change obtained from the rigorous transmission line model is very close to that calculated from the temperature profile using a simple geometric optic approach. This implies that the geometric optic approach can be accurately used, which significantly reduces the complexity in the optical data interpretation. A direct comparison of the numerical modeling results and the phase shift from measurements is possible only if the exact value of the temperature coefficient of the refractive index of silicon (dn/dT) is known. On the other hand, assuming that accurate modeling results are provided, the dn/dT can be determined by the calibration of the experiments. For the purpose of the verification of numerical analysis, the channel temperature at various heating pulse widths τ_H is extracted from pulsed I-V measurements (Fig. 4).

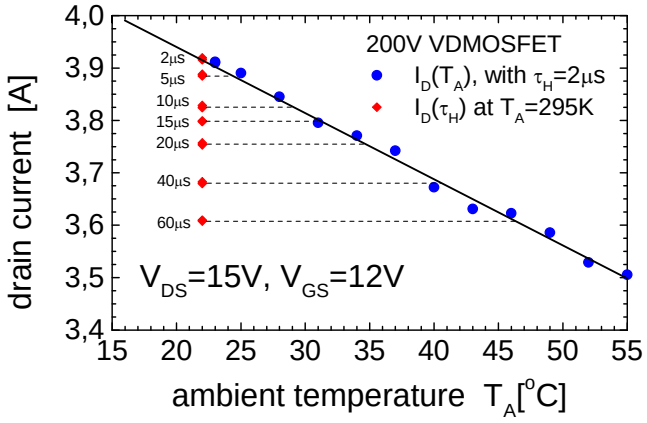

Fig. 4: Pulsed I-V measurements for the determination of the channel temperature for different heating pulse widths (200 V VDMOSFET). The channel heating at short pulses τ_H = 2 µs (circles) at increased ambient temperature is used as a reference. From the decreased drain current due to self-heating with longer gate pulses (diamonds) the corresponding channel temperature is extracted.

The modeling results for the temperature close to the Si/SiO_2-interface correspond to the values obtained from the pulsed I-V measurements. As depicted in Fig. 4 for a heating pulse width of τ_H = 60 µs, the temperature increase in the channel after 20 µs is extracted to ΔT = 12.5 K, in agreement with the calculated value of ΔT = 12 K. Quantitative matching of various modeling to measurement results of the transient phase shift at the end of the heating period results in a mean value across all samples of $dn/dT = 1.6 \cdot 10^{-4}\ K^{-1}$, where this result is very consistent with data from the literature [5]. Figure 2a shows a typical result for the calculated phase signal which is in good agreement with the experiment.

5. Conclusion

The backside laserprobe technique has been successfully applied to study the transient heating in power VDMOSFETs and IGBTs with a high temporal resolution. From the numerical analysis a 1-D thermal model combined with a geometric optic approach are found to be sufficient for the modeling of the phase modulation signals. From this study a value of dn/dT is obtained, which is the basis for quantitative studies of the critical thermal effects in such devices.

Acknowledgments

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High Precision Depth Profiles with SIMS

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This paper demonstrates applications of surface analysis techniques for the investigation and characterization of materials and production processes. SIMS depth profile measurements of implanted erbium in silicon demonstrate that high precision measurements of low concentrations are necessary to assist implantation and simulation groups. Measurements of potassium profiles in fullerene films were performed to investigate diffusion processes in order to optimize material properties. Measurements of the three dimensional distribution of trace elements in high purity molybdenum points out the importance of distribution analysis of raw materials for microelectronics.

1. Introduction

Surface analysis techniques play an important role for supporting material development and process optimisation. One of the most common techniques is Secondary Ion Mass Spectrometry (SIMS). This is due to the high detection power of the method, the fact that all elements are detectable and the possibility of registering two- and three dimensional distributions of trace elements.

To support various investigations in the field of microelectronics, the performance of analytical methods has to be increased. The actual questions of technology demand a permanent development of the precision of measurements, especially at very low concentrations. The supervision of the implantation process stability by measurements of depth profiles for erbium demonstrates the support of optimizing production processes. Investigation of the implanted potassium distribution in C_{60} fullerenes supplies information for the development of new materials. It will be shown that the determination of trace element concentration is necessary for the development of high purity materials like molybdenum.

2. Results

2.1. Erbium in Silicon

The 4f shell of rare earth elements is well shielded by the outer shell electrons. Therefore these elements exhibit sharp and almost atom-like spectra when incorporated as dopants in semiconductors and isolators. The emitted wavelengths practically coincide with those observed for isolated atoms and depend only little on the host material. Erbium implanted into Si produces rich spectra of sharp lines in photo- and also in electroluminescence in a narrow spectral region close to 1,54 µm. This wavelength stimulates interest in Si:Er as a candidate for light emitting devices for fibreoptic communication systems and also for on-chip and inter-chip optical data transfer.

Investigations by high resolution photoluminescence and deep level transient spectroscopy of Er-implanted silicon were made by Dr. Palmetshofer [1].

The ion implantation of 320 keV (implanted by Dr. Palmetshofer, University Linz) and 2 MV (implanted in Guildford, UK) erbium in CZ and FZ silicon was performed at room temperature with doses of 3,13 x10^{13} and 8,13x10^{13} cm^{-2}. To determine the diffusion coefficient of erbium in silicon, one series of the samples were tempered at 900 °C for 30 min in nitrogen.

The SIMS depth profiles of implanted erbium in silicon show no broadening of the erbium implantation profiles during the temperature treatment. The maximum concentration of erbium was about 2x10^{18} atoms per cm^3, the profiles were Gaussian like. The detection limit was lower than 1x10^{15} atoms per cm^3. This indicates that there is no significant diffusion of erbium at a temperature of 900 °C.

The profiles show no enrichment of Er at the surface, this indicates that Er does not segregate during the annealing in samples with implantation doses below 10^{14} cm^{-2}.

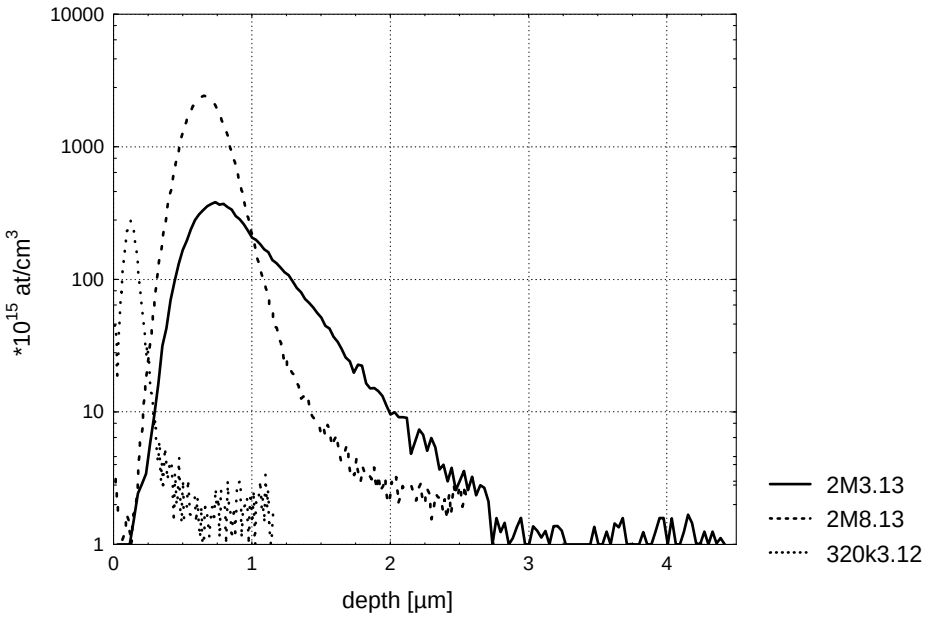

Fig. 1: SIMS erbium profiles of Si implanted with 2 MeV (2M3.13, 2M8.13) and 320 keV (320k3.12) Er^+ with doses of 3.13 x 10^{13} cm^{-2} (2M3.13), 8.13 x 10^{13} cm^{-2} (2M8.13) and 0.312 x 10^{13} cm^{-2} (320k3.12). All profiles show the expected gaussian distribution.

Contrary to all expectations the profiles of the first measured 2 MeV samples were channeling like. Further analysis shows that these profiles are not results of axial channeling in [100] direction but of planar channeling. Probably this is the result of an incorrect implantation process. Renewed implantations did not show this behavior.

2.2. K in Fullerens

Films of chromatographically purified C_{60} were prepared on silicon substrates by vacuum deposition. Ion implantation of 30 keV $^{39}K^+$ was performed at 300 °C in a vacuum better than 10^{-4} Pa. The depth profiles were measured using 5.5 keV O_2^+ primary ions.

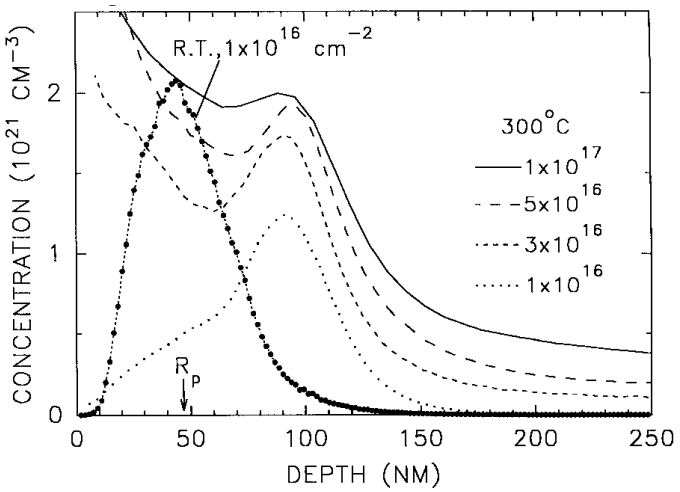

Fig. 2: SIMS potassium profiles for C_{60} films implanted with 30 keV K^+ at room temperature ($1x10^{16}$) and at 300 °C (1, 3, 5 and $10x10^{16}$ cm^{-2}).

Figure 2 shows the depth profile of $^{39}K^+$ for samples implanted with 30 keV at room temperature ($1x10^{16}$ cm^{-2}) and at 300 °C (1, 3, 5 and $10x10^{16}$ cm^{-2}). For room temperature implantation, the experimental profile is Gaussian-like with a weak diffusion induced tail at greater depths.

At 300 °C implantation temperature a peak appears in the tail region at about 100 nm, and the K-concentration within the theoretical ion range is strongly reduced. An increase of the dose leads to a subsequent increase of the peak at about 100 nm and to a slight shift of its maximum into the depth. However, with increasing dose the K-concentration in this region tends to saturate at a value of about $2x10^{21}$ cm^{-3}. A certain amount of K diffuses out to the surface, but the diffusion into the depth is more pronounced. In all samples more than 70% of the implanted atoms are found underneath a 70 nm surface layer. Raman spectra indicate that there is a passivating a-C surface layer and the accumulation of K is at the a-C/C_{60} interface. These structures may have useful applications for new Tc superconducting devices on the basis of fullerenes which can be handled on air [2].

2.3. Ultra pure Molybdenum

Due to the high heat resistivity molybdenum is used as sample holder for the MBE process. During the MBE process trace elements with concentration below the ppm (part per million) level diffuse in the sample, this results in contamination of the devices. The use of ultra pure materials prevents this process. Not only the overall (bulk) concentration is decisive for this diffusion, also the distribution and the chemical state of the trace elements. Therefore the determination of the three dimensional distribution is necessary for the development of functional materials.

The material we investigated is 6N molybdenum, that means that the concentration of all trace elements together is below 1 ppm (part per million). This material is used for the production of MBE sample holders.

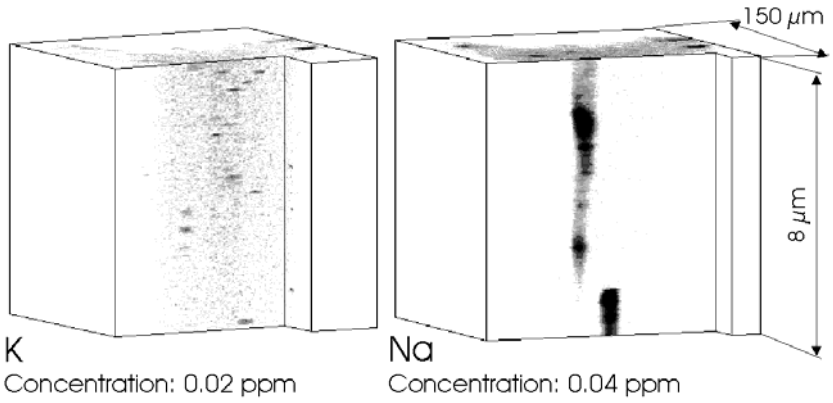

Fig. 3: 3D-distributions of K (left side) and Na (right side) in high purity molybdenum (6n purity). The K precipitates have diameters about 30 nm, the Na is concentrated in impurities with a diameter of about 1 µm.

The investigations indicates that the trace elements are concentrated in precipitates with diameters depending on the measured element. There is no correlation between the different species, this indicates that these elements are not present due to contamination during the production process.

3. Conclusion

Microelectronics is a continual challenge for modern material analysis. In many cases improvements of well established analytical methods, like SIMS, is necessary to obtain precise measurement results of the concentration of dopands and trace elements. This knowledge makes the development of new processes and materials possible.

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Characterization of Si-based Structures by Luminescence and ESR Experiments

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Bulk Si, quantum-well structures of SiGe, and porous Si structures have been investigated by luminescence and electron-spin-resonance (ESR) methods. In luminescence we find after implantation and thermal treatment residual impurities with finger-print spectra and also dislocation related structures. The latter are distinguishable from other defects by their characteristic dependence on hydrostatic pressure and temperature. In ESR experiments, cyclotron resonance is clearly visible, which offers the possibility to detect free carriers without the need for contacts.

1. Introduction

Among the current problems in the technology of Si there is (i) the development and the integration of light emitting elements [1], [2] and (ii) the development of ultra-small ultra-fast devices. In both cases, small structures are used and effective characterization methods are needed to identify residual defects, carrier concentration and their mobility, dimensionality of the structure, etc. In many cases, electrical contacts impose substantial problems in such structures and therefore contactless methods are preferred if available. Among the standard methods for the characterization of defects is photo-luminescence which in high quality crystals can detect defect concentrations as low as 10^{10} cm^{-3}, in some cases sufficient also for low-dimensional samples. The spectra reveal their origin, however, only in rather specific cases. Electron spin resonance (ESR) in principle is more powerful since it yields information also on the chemical identity of the defect and its neighbors. On the other hand, ESR relies on the absorption of microwaves which penetrate the whole sample and thus its sensitivity is rather described by an absolute number of spins which for typical defects in Si is of the order of 10^{12}, too large for small structures. The sensitivity for free carriers in ESR can be much bigger, a few thousand electrons can be easily detected in cyclotron resonance if the mobility is high enough as it was demonstrated in the course of this project.

In this paper we concentrate on two examples of luminescence results. Some of the luminescence spectra seen exhibit sharp, characteristic patterns due to phonon replica and their isotope splittings, constituting a fingerprint of the defect species. Copper, *e.g.*, is clearly seen and detectable as a frequent contamination after even simple technological steps. Other luminescence spectra produce rather wide and less characteristic features and sometimes they are not clearly distinguishable from other luminescence centers. As an example, we present data obtained on Er-implanted samples which show, after specific treatment, meant for annealing of implantation defects, a strong emission [4] close to the technically interesting wavelength of 1.54 μm. We show that this emission at low temperature really is due to Er, but at temperatures above 150 K, luminescence due to dislocations prevails.

In part 3 we present photoluminescence data on porous Si which was doped electrolytically by Er. We observe emission of the characteristic 1.54 µm emission of Er even above room temperature although in bulk Si it is quenched already below 200 K.

2. Photoluminescence Due to Dislocations on Doped Si

Although Si plays the dominant role in microelectronics, it suffers for principle reasons in optoelectronic applications: Because of its indirect gap it does not permit the fabrications of band edge emitters in contrast to III-V and II-VI compounds. In the past few years, possibilities to overcome this shortcoming were investigated making use of luminescence due to localized states. One idea in this context was to utilize the intra-4f transitions of rare earth elements, and here in particular those of Er, whose lowest transition occurs at 1.54 µm, close to the damping minimum of silica fibers [4]. In the past few years, the weak luminescence yield was optimized but a principle problem still appears unsolved: the luminescence quenches at temperatures well below room temperatures, excluding technical application [3]. More recently, however, reports appeared, claiming electroluminescence also at room temperatures due to Er in Si. In order to clarify the origin of this luminescence we have investigated samples which show luminescence close to 1.5 µm also at 300 K.

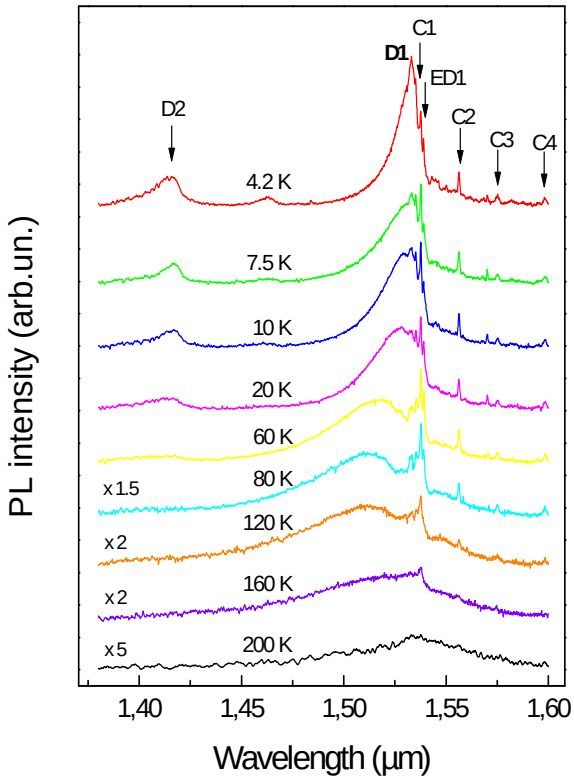

Fig. 1: Photoluminescence spectra of Er-implanted CZ-Si as a function of different temperatures.

The nature of this emission is more clearly seen in low temperature experiments. In Fig. 1, luminescence spectra are shown obtained in CZ-Si implanted with Er (2 MeV, $3 \cdot 10^{13}$ cm^{-2}) after annealing at 900 °C for 30 min. At low temperatures, the emission due

to interstitial (cubic) Er is seen (lines marked C1…C4) together with a line due to an Er complex [5]. In addition, a wide structure is seen close to 1.5 µm which, together with the line marked D2 is attributed to dislocations in the literature. The structure at 1.5 µm, known as D1 line in the literature [6], exhibits also a characteristic temperature shift — at low temperatures towards shorter, above 80 K towards longer wavelengths — whereas the Er line positions remain independent of temperature owing to the extremely localized nature of the 4f states.

Another characteristic feature of the Er lines is their independence on pressure which allows to distinguish them easily from the dislocation luminescence. This is shown in Fig. 2, where low temperature spectra are given for different hydrostatic pressure. It is clearly seen that the D-lines shift towards shorter wavelength whereas the Er lines remain independent of pressure. The pressure coefficient for the transition energy is evaluated to be -2.3 meV/kbar which may serve as an additional characteristic feature of the dislocation luminescence.

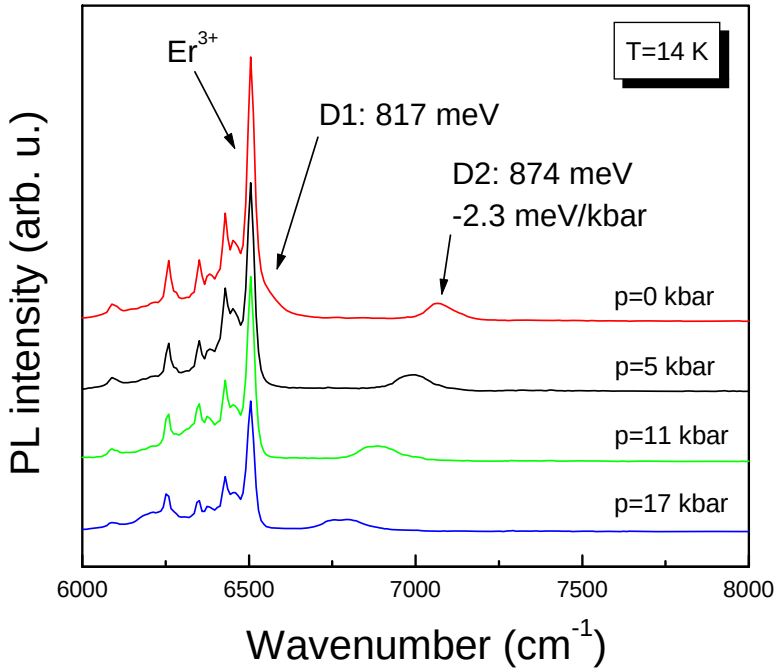

Fig. 2: Luminescence spectra of CZ Si:Er for pressures of 0, 5, 11, and 17 kbar, respectively. The highest pressure corresponds to the lowest D2 position.

The dislocation luminescence is seen also in electroluminescence devices designed for Er emission. Junctions prepared by implanting Er into p-type Si exhibit the same type of electroluminescence spectra when operated under forward bias condition as shown in Fig. 1, *i.e.*, they give strong Er luminescence at low temperature but above 150 – 180 K only the dislocation emission is seen.

3. Luminescence of Porous Si:Er

The temperature induced quenching of the Er luminescence in different host materials seems to correlate to the energy gap of the host: the bigger the energy gap, the higher the critical temperature for quenching. Therefore, in order to improve the luminescence

yield, any measure to increase the gap of Si based material should help. In order to test this hypothesis, we have produced porous Si by anodic etching. Porous Si consists of single crystal material with pores and columns of about 40 Å in diameter. Porous Si has been investigated in the last few years because of its bright visible photo- and electroluminescence which is interpreted in terms of the blue shift of the band edge emission due to electronic confinement in the small structures.

We introduced Er into po-Si electrolytically from $ErCl_3$ dissolved in ethanol. After annealing at 1000 °C for 10 s in an O_2/N_2 atmosphere the samples show sharp and intense Er-related emission which can be clearly demonstrated by excitation spectroscopy: The emission of the 1.54 µm can be excited resonantly both in the 870 and the 980 nm bands, which correspond to the transitions from the J=15/2 ground state of Er to the 9/2 and the 11/2 states, respectively. In bulk Si, these excitations are not detectable because of the strong competition of the interband transitions — these transitions are situated already above the gap of single crystal Si.

In Fig. 3 we show the temperature dependence of our po-Si:Er emission at 1.54 µm as a function of temperature in comparison to other Si-based host material. The dramatic improvement as compared to single crystal bulk Si is clearly seen which again demonstrates the empirical rule of Favennec [3].

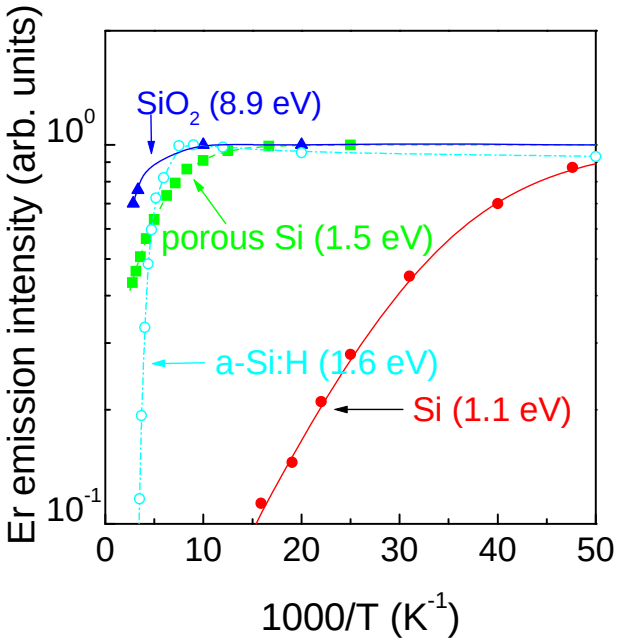

Fig. 3: Normalized luminescence yield of Er in Si-based material as a function of inverse temperature for bulk Si, amorphous Si, po-Si and SiO_2.

4. Conclusions

In this report we have shown that the technologically interesting luminescence of Er in Si can be improved dramatically at high temperatures by using Si-related material with larger energy gap: In agreement with the rule of Favennec, the thermal quenching of the Er luminescence occurs at higher temperatures for material with higher energy gap. Porous Si provides one of very few possibilities so far to increase the gap of Si (the

alloys of Si have a tendency for smaller gaps only). Reports in the literature on room temperature Er emission in electro-luminescence of forward biased p-n junctions should be reconsidered in view of our present results which show that the emission observed in our samples are due to dislocations at elevated temperature.

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Surface Analysis by Auger Electron Spectroscopy

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We investigated the ternary II-VI compound semiconductors $Zn_{1-x}Mg_xTe$ $x \in [0, 1]$ by quantitative Auger Electron Spectroscopy. Emphasize was put on the behavior of the sensitivity factor s of the various constituents of the compound as a function of the composition of the ternary compounds. The sensitivity factors were calculated by a new formalism and showed a strong dependence on the compound composition. In the case of Te we found a change of the line shape and the appearance of Coster-Kronig transitions. Binary II-VI compounds like ZnSe, ZnTe, CdSe and CdTe were investigated with respect to their surface composition after reactive ion etching in CH_4/H_2 admixtures of different composition.

1. Introduction

The binary and ternary II-VI compound semiconductors are applicable to the production of blue light emitting diodes [1] – [3]. One of the main problems in these optoelectronic devices is the degradation, which is mainly caused by defects generated from strain and stress in the layers. A possibility to overcome that drawback is to fabricate lattice-matched multilayer structures. Since the lattice match is very sensitive to the composition of the compounds, an exact control during growth of the layers is indispensable. A method to control the composition is the Auger Electron Spectroscopy (AES). A main problem in quantitative AES (QAES) is that the sensitivity factors *s* of the constituents, which are equal to the probability of the occurrence of an Auger process [4] are only known for pure elements. Within this project we performed QAES on various compositions of $Zn_{1-x}Mg_xTe$ $x \in [0,1]$.

Parallel with the development of wide band gap II-VI blue-green diode lasers, the investigation of optical properties of quantum wires and dot structures has attained considerable interest [5] – [8]. An established method for the fabrication of lateral structures (e.g. quantum wires and dots) is the reactive ion etching (RIE) technique [9]. Most of the earlier studies of RIE on II-VI compounds used chlorine-containing gas mixtures [10]. In latter works a mixture of CH_4 and H_2 was used as etchant, which allows the fabrication of very small vertical structures with a minimal width of about 25 nm [11], [12]. In the literature a mixture between 1:6 and 1:8 for CH_4:H_2 ratio is reported to be an optimum etchant with respect to optical behavior of the fabricated nanostructures [5]. There are only few publications which are dealing with the chemical analysis of etched structures [13], [14].

We performed quantitative Auger electron spectroscopy (QAES) [15] analysis of ZnSe, ZnTe, CdSe and CdTe samples which were grown by molecular beam epitaxy (MBE) [16], and etched by RIE. In our analysis emphasize was given on the changes of the chemical composition of the etched samples due to the various ratios of CH_4:H_2 in the etchant not

only at the surface but also by depth profiling. In addition, the influence of oxygen as part of the etchant was investigated.

2. Results and Discussion

2.1. Sensitivity Factors

The sensitivity factors for Zn, Mg and Te as a function of the composition of the sample obtained with different primary electron energies were evaluated. A general trend could be seen that the sensitivity factors for all elements are increasing with increasing Mg content in the sample. Only the sensitivity factor of Te has a minimum in the range of x = 0.5. This is due to so-called Coster-Kronig transitions [16], which become dominant for samples with a composition around x = 0.5. The Auger spectra for $Zn_{1-x}Mg_xTe$ layers with different concentrations of Mg show beside the normal MNN Auger transitions also the MMN Coster-Kronig transitions. As a consequence the normal Auger transitions are decreased since the number of exciting primary electrons is constant in all the experiments.

2.2. Reactive Ion Etching

In the II-VI compounds ZnSe, ZnTe, CdSe and CdTe (i) the deviations from the stoichiometry, and the incorporation of (ii) oxygen and (iii) carbon were investigated as a function of the etching gas ratio in the RIE process.

(i) Down to a depth of about 20 Å the concentration of Zn and Se is lowered due to a large incorporation of carbon and some additional oxygen. The ratio of Zn to Se is nearly constant.

The lowest deviations from stoichiometry were found at CH_4:H_2 ratios of 1:6 and 1:7. Other CH_4:H_2 ratios showed large deviations from stoichiometry. For comparison, also as-grown samples were sputtered which showed no deviations from stoichiometry and indicate no effect due to preferential sputtering. Therefore we conclude, that deviations from stoichiometry which were investigated to a depth of 100 Å have their origin in the etching process.

(ii) The incorporation of oxygen into the samples could be clearly analyzed by QAES. In the case of Zn compounds the oxygen concentration is increasing with increasing hydrogen content in the etchant, whereas for the Cd compounds the oxygen content is decreasing. For a ratio of CH_4:H_2 of about 1:7 the incorporation of oxygen is low (between 1 and 2%) for all analyzed systems.

(iii) In contrast to oxygen, the carbon concentration decreases with sputter depth. The incorporation depth is between 20 and 80 Å. For Zn compounds, the C incorporation depth is lowest around a CH_4:H_2 ratio between 1:6 and 1:7, whereas for Cd compounds the depth is monotonically increasing with higher H_2 content. At a CH_4:H_2 ratio between 1:6 and 1:8, the incorporation depth is relatively low in all compounds.

3. Conclusion

The sensitivity factors for the constituent elements in the ternary II-VI compound $Zn_{1-x}Mg_xTe$ depend very strong on the composition of the compound.

For the investigated II-VI compounds (ZnSe, ZnTe, CdSe and CdTe) a relative small deviation from stoichiometry for a CH_4:H_2 etchant ratio around 1:7 is found as a common behavior. This is in agreement with literature, where an etchant with such a CH_4:H_2 ratio is used in order to give optimum optical behavior of the etched structures [5]. In addition, the incorporation of oxygen was detected over the whole investigated depth of 100 Å, whereas the carbon incorporation was limited to a depth between 20 and 80 Å.

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