Silicon Technology: Risks, Opportunities and Challenges

Hermann Jacobs

Siemens AG, Corporate Technology, Microelectronics
D-81730 Munich, Germany

1. Introduction

The enormous progress of microelectronics over the last two decades has resulted in an orders-of-magnitude increase in computational power and storage capacity. There is a general consensus in industry and academia that this exponential growth will continue for another 10 to 15 years.

Progress will come at a price, however. The increase in both technology process and product design complexity will require enormous interdisciplinary efforts to cope with the challenges ahead. Finally the often quoted "limits of microelectronics" may be less determined by the physical limits of device miniaturization but by economic considerations, both on the manufacturing and design levels.

Future technologies (nanotechnology, quantum electronics, molecular electronics) will have to measure up to this criterion as well. It will be difficult for them to prove their viability in view of the overwhelming momentum, both technical and economic, that silicon technology has gained over the last three decades.

2. Roadmap

In the 1970s, Gordon Moore predicted a doubling of complexity for Silicon ICs every 18 months [1]. Ever since, analysts have warned that deviations from this exponential behavior were imminent, quoting "barriers" at minimum feature sizes of, e.g., one micron, 0.5 µm, 0.25 µm, for various physical and technical reasons. Today it seems likely again that we may experience a deviation from "Moore's law" – to even faster growth.

For the last several years, the US-based Semiconductor Industry Association (SIA) has convened a panel of microelectronics experts who develop and maintain a National Technology Roadmap for Semiconductors (NTRS) [2]. Figure 1 shows a strongly condensed version. The NTRS predicts a continuing exponential increase in IC complexity, according to Moore's law, extending to minimum feature sizes of 0.07 µm at 64 Gbit memory densities in 2010.

	1995	1998	2001	2004	2007	2010
Feature size (µm)	0.35	0.25	0.18	0.13	0.10	0.07
Memory	64 M	256 M	1 G	4 G	16 G	64 G
Logic (µP) Trans./cm^2	4 M	7 M	13 M	25 M	50 M	90 M
Chip frequency (MHz)	300	450	600	800	1000	1100
Substrate dia. (mm)	200	200	300	300	400	400
Supply Voltage Standard	3.3	2.5	1.8	1.5	1.2	0.9
Portable	2.5	1.8-2.5	0.9-1.8	0.9	0.9	0.9

Semiconductor International 1995

Fig. 1: National Technology Roadmap for Semiconductors (SIA NTRS)

Since its first presentation the NTRS has become a “self-fulfilling prophecy”. Everyone expects that their competitors’ speed of innovation is obeying the same (or even faster) pace. The burden is on microelectronics research and development to make the NTRS a reality. The following paragraphs will outline a few of the technical challenges that face us.

3. Processing Challenges: Lithography

The most obvious “barrier” for further reduction of feature size is the possible lack of a suitable mask printing process. According to earlier predictions, X-ray lithography should have replaced optical lithography at the 0.5 µm level already, due to the limit imposed by the wavelength of visible light.

Today, however, printing of 0.25 µm structures is the industry standard, using a wavelength of 248 nm (deep UV, KrF excimer laser light).

The first ArF (193 nm)-light-based lithography is currently being installed and may yield an industrially viable process at least down to 0.13 µm (Fig. 2). Adding the possibilities of special enhancement techniques (Phase Shift Masks (PSM), Off Axis Illumination (OAI), Optical Proximity Correction (OPC)) plus F_2 (157 nm)-light at the horizon, optical lithography may take us all the way to 0.1 µm structures.

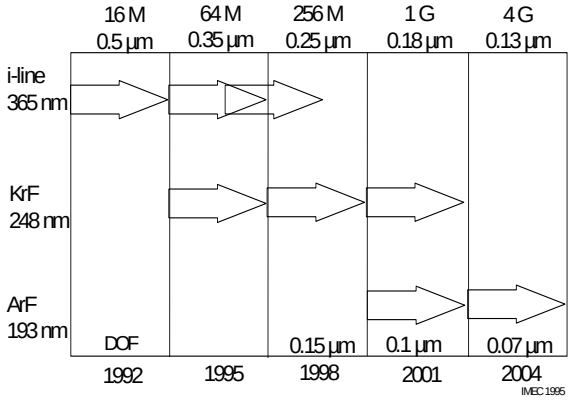

Fig. 2: Roadmap for optical lithography into the 0.1µm generation

Incidentally, 0.1 µm is also the resolution limit for X-Ray lithography with conventional shadow masks [3].

However, the advent of these leading edge optical techniques will require enormous qualitative leaps in, e.g., optics, photoresist, antireflective coatings, planarization processes and metrology (overlay accuracy is most critical). Last but not least, the enhancement techniques mentioned above will result in a complex relationship between circuit design / layout and technology, requiring a huge interdisciplinary involvement of the CAD tool community.

4. Materials Challenges

As device dimensions shrink into the deep sub-micron regime, some of the electrical parameters escape the usual trend towards better performance. As an example, the requirements for data retention in a dynamic memory device (DRAM) force us to keep the storage capacity at approximately 30 fF. Given the decreasing lateral feature size this means an increased size in the third dimension. For one of the most successful ideas in DRAM, the trench capacitor, this “escape” is coming to an end, however, starting at the 1 Gbit level. Etching depths for the trench capacitor are becoming prohibitive (> 10 µm), even if more for economic than technical reasons (Fig. 3).

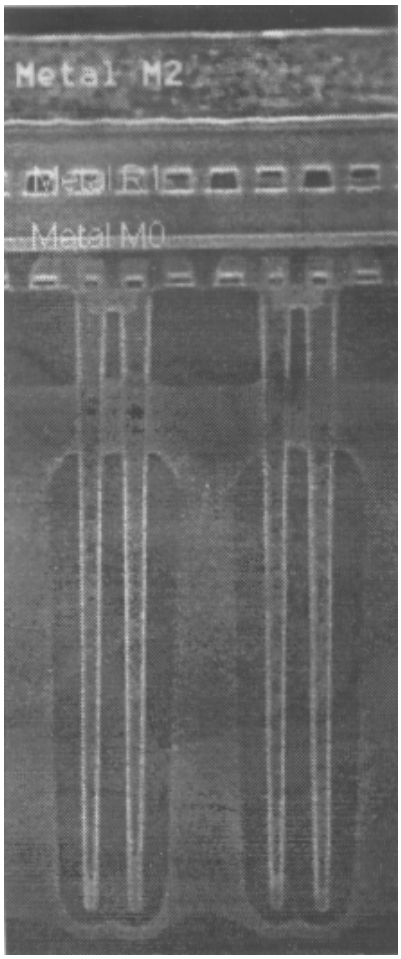

Fig. 3: 256M DRAM trench cell (IBM/Siemens/Toshiba)

Similar arguments hold for a capacitor stacked on top of the silicon surface. Since the thickness of the storage dielectric cannot be shrunk beyond the tunneling limit, the options to maintain the storage capacitance are reduced to an increase in the dielectric constant. This increase must go much beyond what is available from SiO_2 ($\varepsilon_r \approx 4$) or ONO ($\varepsilon_r \approx 7$).

One of the presently favored high ε materials is $(Ba,Sr)TiO_3$ (Barium-Strontium-Titanate or BST) which exhibits paraelectric behavior at room temperature with $\varepsilon_r >> 100$. The use of BST as a storage dielectric will also pave the way for introducing "real" ferroelectric materials (like Strontium-Bismuth-Tantalate, SBT) into memories. Ferroelectric RAMs (FRAMs) may be the ultimate storage solution, combining non-volatility as in EEPROMS with the speed of DRAMs.

Introducing these materials into silicon processes has numerous challenges, however. Capacitor dimensions in the tenth-micrometer range require thin (30 nm) layers of high ε material, conformally deposited over high-aspect ratio, deep-sub-micron structures, without sacrificing crystallinity and stoichiometry. This requires a well-controlled multi-component CVD process, followed by a high temperature anneal in oxygen. This in turn requires new electrode materials (candidates are Pt, Ru, RuO_2, Ir) and appropriate barrier materials since silicon components will oxidize strongly at these conditions. Accompanying the materials and process challenges is the risk of contaminating the IC fabrication line with these "exotic" substances.

Generally, the realization of the NTRS will require a "paradigm shift" away from silicon components and related "simple" materials to more risky substances (Fig. 4). Solving these problems will again require an interdisciplinary approach from material scientists and chemists, analytics experts, process and equipment designers and integration specialists.

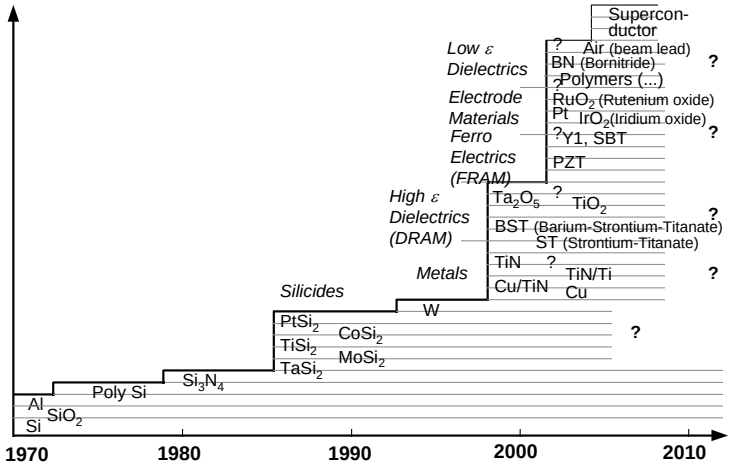

Fig. 4: Progress in microelectronics increasingly requires the introduction of new materials

5. Manufacturing challenges

The cost of IC manufacturing has seen an exponential behavior comparable to Moore's law . In view of the decreasing minimum feature sizes, the decreasing critical defect density, the increasing wafer size and increasing number of process steps (e.g. needed for the integration of new materials) it seems unlikely today that the cost curve will bend down in the future.

To meet this economic challenge will require applying "smartness" to all levels of manufacturing. On the equipment side the major issue will be to increase utilization, i.e. the time in which actual production wafers are processed. A way to achieve this goal is short-loop controlled, in-situ monitored single wafer equipment. That in turn demands detailed knowledge of physics and chemistry of the processes which must be gained through intense use of simulation and analysis tools. On the process integration side, "Smart Fabrication" calls for modular cost-effective processes with harmonized process flows across a large mix of different products.

On the product development side, design for manufacturability will be the major challenge. The main issues here will be to get the most performance at the lowest power from a given technology on one hand, and the highest yield on the other hand. This will require in part to break with one of the most successful paradigms in microelectronics, which was the separation of technology process details from the circuit and system design levels. A new level of computer aided technologies will have to be generated to deal with this new complexity [4], [5].

6. Outlook

In view of the predictions of the SIA NTRS, it seems that there is no need for an alternative to Silicon ICs in the foreseeable future. Adding the production lifetime of a technology of at least 10 years to the 2010 timespan of the NTRS, we may have a quarter of a century before silicon will be "outdated". Nevertheless, one of the most threatening physical effects that may force us much earlier to seek for alternatives is power consumption. Simple calculations show that, without revolutions in system architecture and technology, systems-on-chip in the 64 Gbit age will be prohibitively power-hungry.

The ultimate low power device (in theory at least) may be a Single Electron Transistor. It allows switching of states with just one electron based on the Coulomb blockade effect.

However, it seems unlikely that these devices will simply replace today's MOSFETs in logic circuits. Rather, they will probably lead to new systems architectures. They may even use a different signal representation than binary logic, e.g., multilevel logic or error-tolerant designs. The same considerations may be even more true for "biological" technologies (like molecular electronics).

In any case, it seems safe to say that these alternative technologies will require an industrial commitment of at least the size of silicon microelectronics today to become "mature". Nevertheless, these technologies — in the long run — may change the world as profoundly as silicon technology has done in the last two to three decades.

References

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