Realisation of threshold voltage adjustable GaAs-MISFETS for VLSI

H. W. Lettenmayr, C. G. Diskus, K. Lübke, L. Palmetshofer*, H. W. Thim
Institut für Mikroelektronik, *Institut für Halbleiterphysik, Universität Linz, 4040 Linz/Auhof

One severe problem gallium-arsenide ICs are suffering from is the difficulty of achieving threshold voltage uniformity over large chip areas required for VLSI technology. This is primarily due to the fact that there is no adequate oxide allowing the fabrication of stable normally-off MOSFET-like transistors. AlGaAs-layers embedded between gate and channel have been used successfully and have led to an increase of the breakdown voltage of MESFET-structures [1], [2]. Logic levels of +2V or higher can be achieved with such a hetero field effect transistor structure.

This type of MISFET-structure is thus well suited for fabricating integrated ultrahigh-speed DCFL circuits, and is therefore an attractive alternative to other structures with ultrathin doping layers and difficult selective etching techniques such as the well known E/D mode logic [3]. However, all these schemes suffer from problems caused by threshold voltage nonuniformities. One way to overcome the uniformity-problems is the implementation of a second gate - the backgate - underneath the channel of the switching transistor [4]. This backgate allows a continuous depletion of the channel by increasing the negative bias voltage applied to the gate. For the first realization of the backgate concept an ion implanted p^+ gate has been used. Some drawbacks of this fabrication technique are the lower quality of the epitaxial layer grown on the ion-implanted channel layer, and the high resistivity of the p^+ layer.

In this contribution a new backgate-concept suitable for VLSI-design is presented. Fig. 1 shows a schematic cross-sectional view of the logic gate. The key feature is the implementation of a second **metal** gate underneath the channel of the switching transistor. We have employed an etch-technique after glueing the active layers to carrier-substrates. After removing the semi-insulating GaAs-substrate with selective etchants metal-backgates are evaporated. In order to test the new concept single inverters, inverter-cascades and 17-stage ring oscillators (Fig. 2) with 0,75 µm backgates have been fabricated. Measured transconductance values of about 50 mS/mm to 160 mS/mm are far away from the best values, although not so far beyond calculations. The conversion of D-mode FETs to E-mode FETs by applying negative voltages to the backgate is shown in Fig. 3 and Fig. 4. Oscillations can be observed over a wide range of supply voltages (Fig. 5 and Fig. 6). Rise and fall times of 57 ps for 1.2 µm gatelength and 130 ps for 2.4 µm gatelength are in agreement with calculated RC-charging times of the gates.

In conclusion, it has been shown that ultrahigh-speed DCFL can be fabricated with the implementation of structured backgates. By applying negative voltage to the backgate the driver transistor can be depleted, larger threshold voltage tolerances in production are possible. Further development in design will improve device parameters.

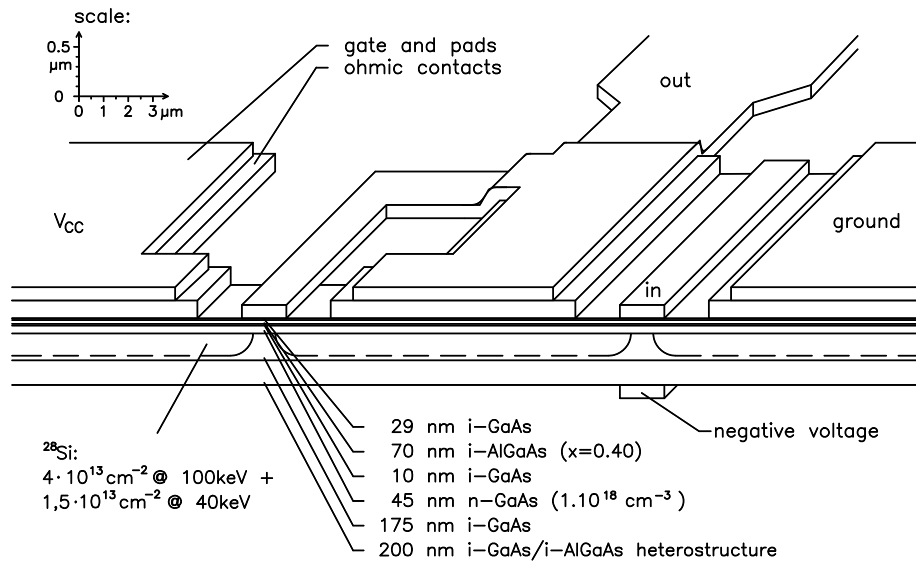

Fig. 1: Schematic cross sectional view of a logic gate.

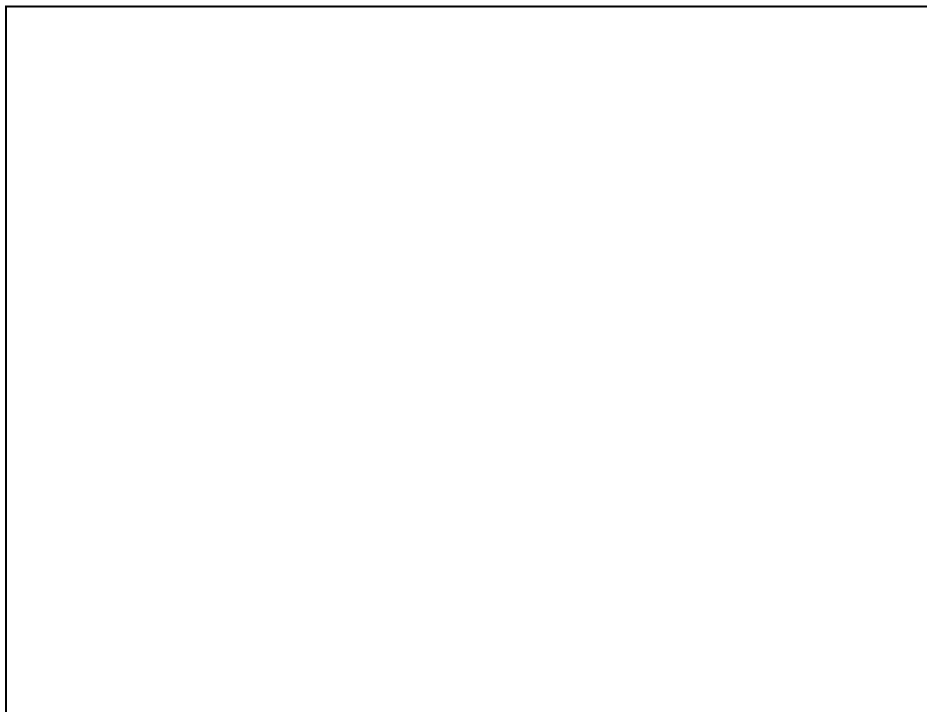

Fig. 2: SEM photograph of a 17-stage oscillator.

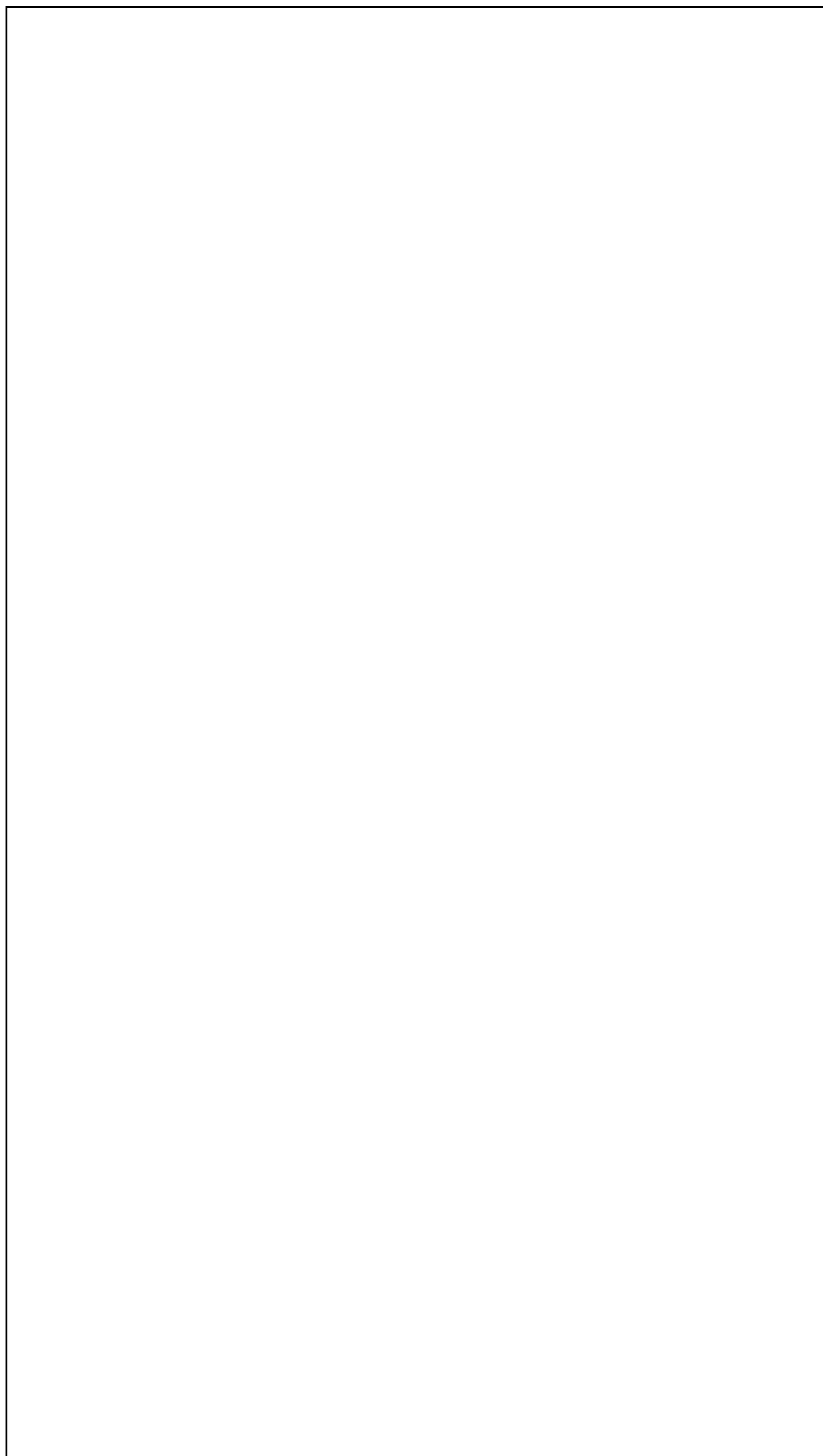

Fig. 3: FET characteristics of sample MO 752/2 2.2/2.2: $\boldsymbol{U_{BG}}$ **= 0 V**, length of gate: 2.4 mm, backgate: 0.75 mm, channel doping: $9.5 \times 10^{17} cm^{-3}$, channel thickness: 39.7 nm

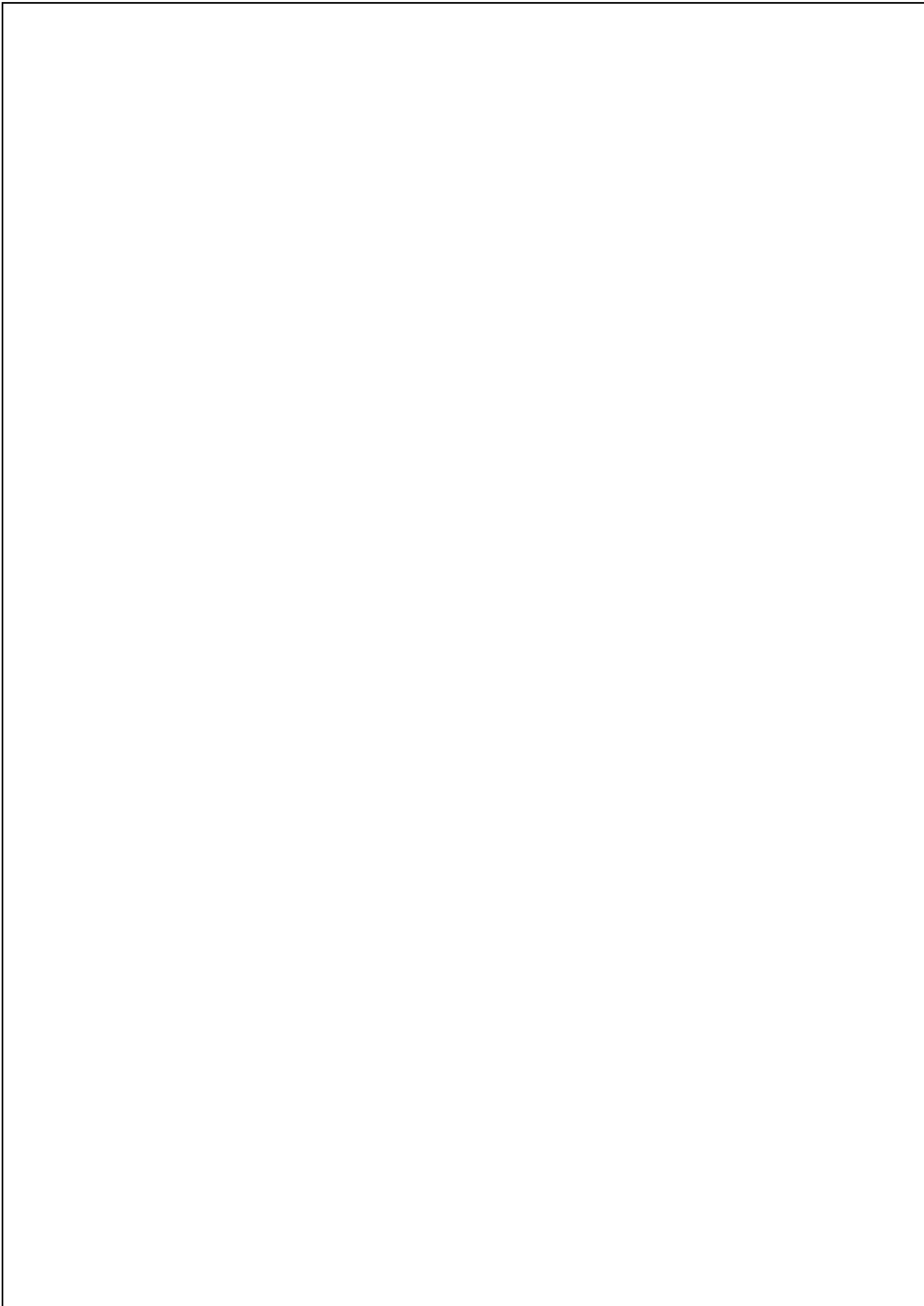

Fig. 4: FET characteristics of sample MO 752/2 2.2/2.2; $\boldsymbol{U_{BG}}$ **= –7 V**, length of gate: 2.4 mm, backgate: 0.75 mm, channel doping: $9.5 \times 10^{17} cm^{-3}$, channel thickness: 39.7 nm

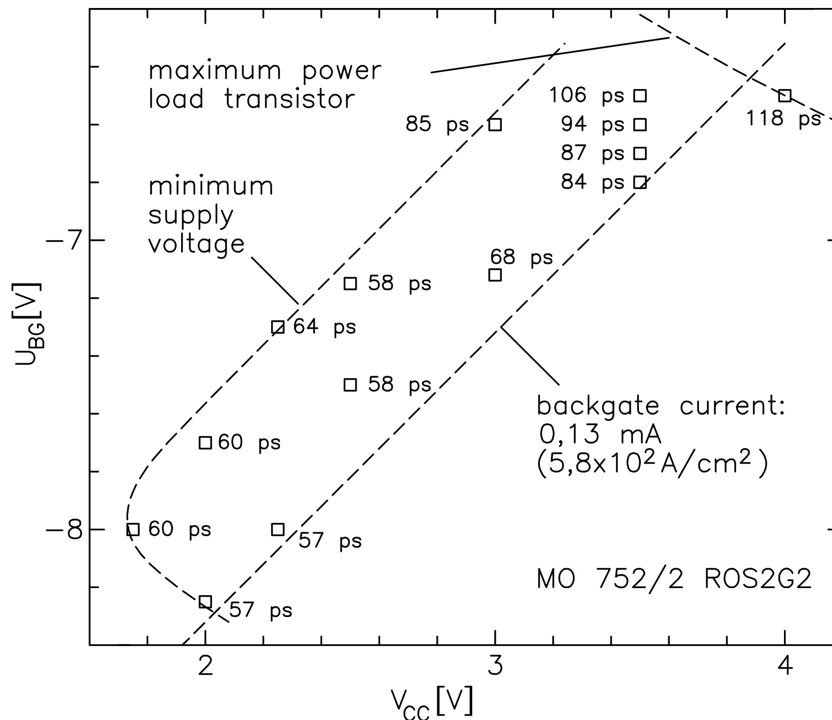

Fig. 5: Switching time of a ring-oscillator depending on the voltage supply. Oscillations are limited by a minimum supply voltage, maximum power and the backgate-current.

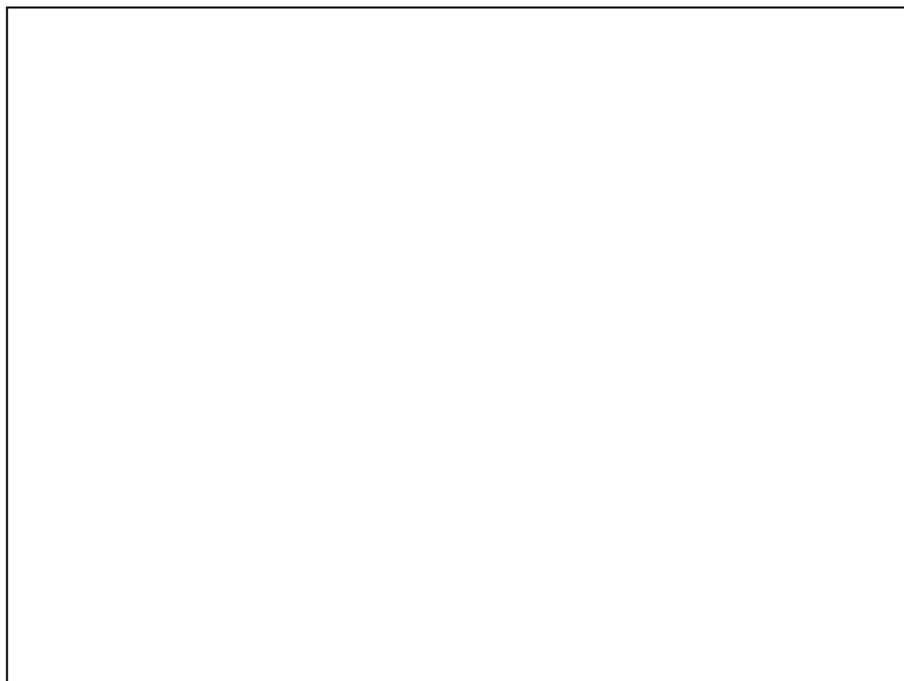

Fig. 6: 420MHz-output of a 1.2/0.75 µm 17-stage ringoscillator; Switching time 70 ps/stage

References:

[1] B. Kim et al., 'Microwave power GaAs MISFET's with Undoped AlGaAs as an Insulator', IEEE Trans., 1984, **EDL-5**(12), pp. 494-495.

[2] C.-L. Chen et al., 'High-Power-Density GaAs MISFET's with a Low-Temperature-Grown Epitaxial Layer as the Insulator', IEEE Trans., 1991, **EDL-12**(6), pp. 306-308.

[3] H. Hida et al., 'High-Speed and Large Noise Margin Tolerance E/D Logic Gates with LDD Structure DMT's Fabricated Using Selective RIE Technology', IEEE Trans., 1989, **ED-36**(10), pp. 2223-2230.

[4] C. G. Diskus et al., 'Threshold voltage adjustable GaAs FET for VLSI', Electron. Lett., 1991, **27**(5), pp. 418-420.