

# Point and Extended Defects in Ion Implanted Silicon

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## 1. Introduction

Ion implantation is central to almost all silicon device manufacture. It provides the capability of close control of the amount of dopant incorporated and the ability to create grossly non-equilibrium dopant profiles. Unfortunately, all ion implantation creates some damage in the silicon lattice, this can range from low concentrations of atomic displacements to total amorphisation dependent on the dose, energy and mass of the implanted species. In order to restore the electronic properties of the silicon, some form of annealing always follows the actual process of ion implantation. Consequently we have to consider the entire ion implantation thermal anneal cycle when examining the defect population which may effect subsequent device performance.

Taking silicon device manufacture in general, we are interested in three types of defect: point defects which can act as recombination centres, point defects which can act as generation centres and extended defects which have pronounced recombination/generation activity when decorated with impurity atoms. Extended defects can also provide the mechanisms for junction shorts and anomalous diffusion. Let us first consider the role of recombination/generation centres in the device environment.

## 2. Recombination-Generation Models

It is important to remember that the electrical activity of an impurity depends not only on its chemical nature but also on its exact siting in the lattice. Similarly, displaced silicon atoms contribute to the electrical activity as vacancies or interstitials, or as a result of complexes formed such as the oxygen-vacancy A-centre.

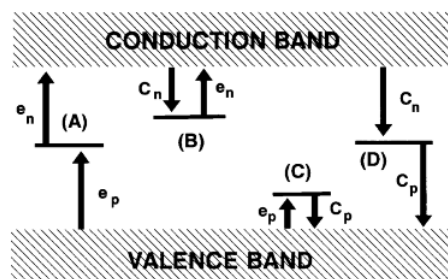


Fig. 1: The classic Shockley-Hall-Read representation of : A) a generation centre, B) an electron trap, C) a hole trap, D) a recombination centre. where arrows show the direction of electron transfer.

Process A) defines the generation lifetime in a material or a device region and technologically is by far the most important process in integrated circuits design for signal processing or data storage. For example, it is the key parameter in setting the refresh rate required for dynamic RAM. Although most text books emphasise process D), recombination, which is often the dominating factor in defining the minority carrier lifetime, it is of relatively little significance in signal processing devices. It is, however, of major significance in power semiconductors and in opto-electronic devices (solar cells, LEDs and opto detectors). The processes B) and C) can contribute to noise in devices but in the present context have more significance in our detection of the presence of deep states by techniques such as DLTS. It is important to note that a mid-gap defect can behave as a recombination centre, a generation centre or as a trapping state. Its role depends much more on the environment it finds itself in than on the physical characteristics of the defect. For example, the same state could well be a generation centre in the depletion region and a recombination centre in the bulk.

### 3. Annealing

The objective of annealing ion implanted silicon is to remove the implant damage. In many cases this needs to be done without redistributing the impurities and so there is always a conflict between total removal of defects (which may require a larger thermal budget) and restricting the movement of dopants. This is a particularly critical problem when very shallow junctions are required (as in ULSI) or where complex doping profiles need to be established (as in varactor diodes, for example). If the diffusion process and the defect removal process have very different activation energies, there will be advantages in using long low temperature anneals or short high temperature anneals (RTA) dependent on whether the defect removal activation energy is greater or less than the diffusion activation. The concept is illustrated in Fig. 2.

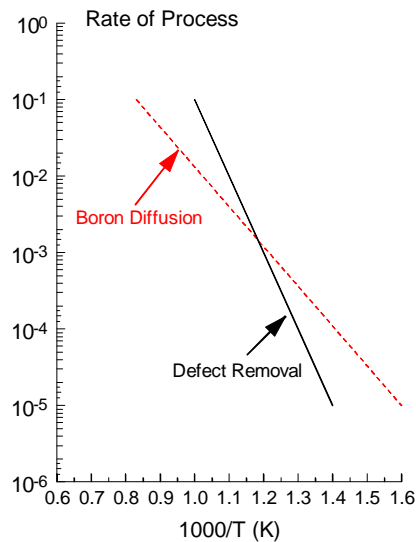


Fig. 2: Arrhenius plot of relative process rates occurring during annealing.

Unfortunately, the choice of annealing schedule is complicated by a number of factors among these is the simple observation that several defect species are important in optimum device operation. They have quite different annealing kinetics which include de-

fect reactions during annealing resulting in the formation of new species. The other major complication is that the diffusion rate of some dopant species, the classic example of which is boron, is dramatically affected by the presence of defects, particularly silicon self interstitials. These factors make generalisations difficult and indeed detailed anneal schedules tend to be process/device specific.

#### 4. Extended Defects

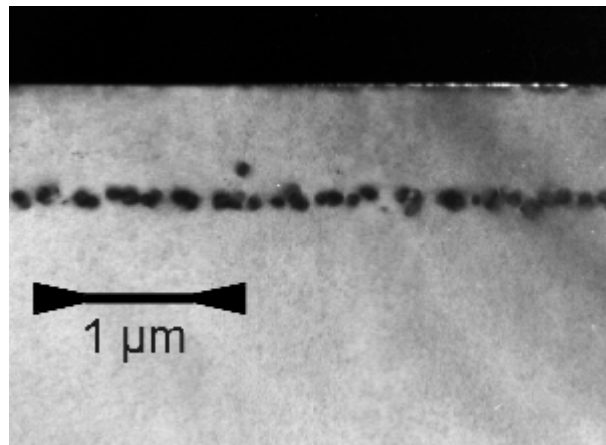


Fig. 3. Cross-sectional TEM image of end of range dislocation loops in amorphised/regrown silicon.

Heavy implants will, in general, produce a significant excess of silicon self-interstitials. The anneal process will tend to remove these to stable locations. Ideally this should be the surface of the semiconductor where they will simply form one or more additional atomic layers of silicon. If the dynamics of the anneal process are such that they cannot reach the surface, they will form dislocations. Figure 3 shows a silicon layer which has been amorphised by a germanium implantation and then slowly regrown at 650 °C in a slightly oxidising atmosphere. The growth of a few mono-layer of oxide at the surface creates additional interstitials which prevent the migration to the surface of the excess interstitials in the implanted region and so the self interstitials condense into dislocation loops at the original crystalline/amorphous boundary. If the same annealing schedule had taken place in a reducing atmosphere (hydrogen) no loops would be present. Many other factors influence the formation of dislocations including the abruptness of the transition from damage to crystalline silicon and the presence of inadvertent metallic species.

#### 5. Decoration of Extended Defects

Extended defects are very important in semiconductor device fabrication because of their electrical activity, distortion of the band gap, and because of the local enhancement of diffusion of dopant species (the long established process of so-called pipe diffusion). It is now generally accepted that only undecorated (clean) dislocations have little or no electrical activity. In semiconductors the term “decoration” has come to be used to describe a quite low concentration of atoms at the dislocation as distinct to the metallurgical sense where decoration would imply a visible precipitation of impurity

atom in the vicinity of the dislocation. The strain field of the dislocation enables mobile impurities to move against the concentration gradient and so accumulate an even precipitate in the vicinity of the dislocation. It is this accommodation of mobile impurities which make extended defects so important in semiconductor processing and ion implantation in particular. Ion implantation processing errors can produce extended defects but is also a potential source of metallic contamination which affects the electrical behaviour of the extended defect by low level decoration

Finding such defects is not easy using conventional methods such as TEM, there are simply not enough of them to occur in the average TEM sample volume and so other methods of detection are being explored.

## 6. Point Defects

As indicated previously, many defect species are produced by implantation and these react to form secondary defects and complexes during annealing. The highest concentration of defects occur in the tail of the implant. This is shown clearly in Fig. 4, which illustrates the evolution of deep states effecting the background doping. This results from a germanium implant into silicon with anneal schedules as shown. Deep Level Transient Spectroscopy (DLTS) and related techniques have been used to study the reactions of these defect species during annealing and in some cases it is possible to relate the electrical fingerprint to the molecular structure of the defects. It is becoming apparent that the presence of impurities in the silicon (oxygen, carbon, hydrogen and transition metals) can have a profound effect on the effectiveness of the annealing schedule.

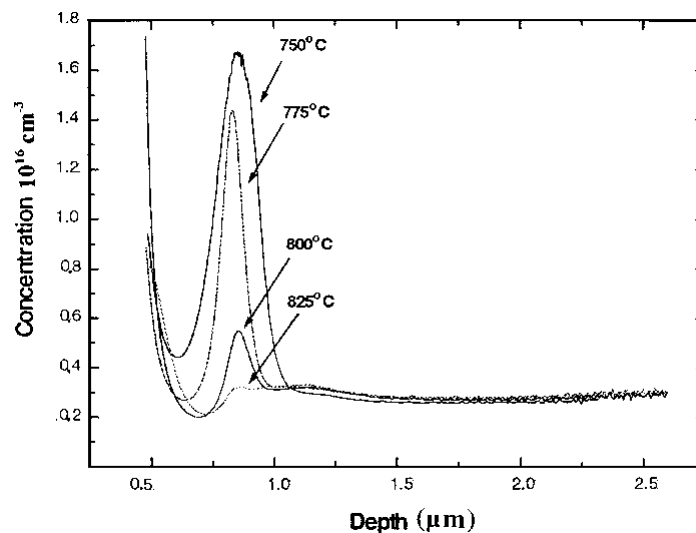


Fig. 4: Apparent electron concentration in n-type silicon ion-implanted with 400 keV germanium with a dose of  $10^{15} \text{ cm}^{-2}$ . The samples were annealed at the temperatures shown for 10 minutes.

## 7. The Future

It is only in the last few years that defect management in semiconductor processing has been put on a firm scientific basis. However, new issues can be perceived which have received very little consideration so far. In particular the statistical nature of defect distribution is evident when it is realised that a sub-micron DRAM cell will work well with three point defects in the active region but fail if six are present. These issues and possible diagnostic techniques will be discussed in the talk.