Si/SiGe Heterostructure Devices

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A review is given of the most recent developments in the field of strained Si/SiGe heterostructures for transistor applications. Main topics are the Si/SiGe heterobipolar transistor (HBT) and modulation-doped field effect transistors (MODFET) utilizing strain-adjusting SiGe buffer layers. Si/SiGe HBTs have recently demonstrated maximum oscillation frequencies (f_{max}) in excess of 100 GHz, which is an improvement of about a factor of two as compared to the best Si bipolar junction transistors (BJT). Si/SiGe HBTs are now on their way into the production lines, and integrated circuits have been announced to become commercially available in the very near future. n- and p-type MODFETs are another promising species of Si-based devices, which once could overcome the well-known matching problem of conventional CMOS circuits caused by the poor performance of the p-type transistors. For the realization of MODFETs tailoring of the band structure by controlled adjustment of the strain distribution in the active layers is required. Both n-type and p-type quantum well structures with — for Si-based systems — unprecedentedly high carrier mobilities could be demonstrated. Accordingly, test-MODFETs show superior transconductances, which is a prerequisite for high operation frequencies.

1. Introduction

In the world-wide electronic market, which is estimated to reach a volume of close to 200 billion $ by the year 2000, Silicon devices have an overwhelming market share of about 97%. The introduction of III-V heterostructures more than twenty years ago, and intense R&D activities in this field, have certainly produced superior devices in high-end areas such as millimeter wave and optoelectronic applications. However, being widely unsuited for large scale integration and lacking compatibility with Si VLSI technologies, the potential market segments for these heterosystems are restricted. On the other hand, the ubiquitous Si technology has in several areas been driven close to its physical limits, and new, fast growing markets, such as telecommunication at GHz frequencies, will require enormous efforts to be addressed by Si devices at all. Therefore, it appears attractive to introduce a heterosystem providing all means of modern band-structure engineering without sacrificing the preconditions for large scale integration, namely the basic compatibility with Si substrates and technologies. These conditions are widely fulfilled by the lattice mismatched $Si/Si_{1-x}Ge_x$ heterosystem.

The most important application of pseudomorphic SiGe layers is the HBT, which has shifted both the unity-gain cut-off frequency f_T and the maximum oscillation frequency f_{max} of Si-based three-terminal devices beyond the 100 GHz margin.

Another potential application of Si/SiGe heterostructures are MODFETs, a device type pioneered in the III-V heterosystems, where it is commercially used for low-noise, high-frequency applications. In contrast to the III-V materials, which are only suited for n-type devices, the Si/SiGe heterosystems can principally provide n- and p-type MODFETs with excellent, and even more important, closely matched, properties.

In the following the pseudomorphic Si/SiGe HBT and the complementary types of MODFETs will be reviewed.

2. Heterobipolar Transistor

Current amplification in an npn bipolar junction transistor (BJT) is mainly determined by the ratio between the density of electrons injected from the emitter into the base, and the density of holes re-injected from the base into the emitter:

$$\beta_{max} = J_c/J_b = (N_e w_e D_n)/(P_b w_b D_p), \quad (1)$$

where N_e and P_b denote the emitter and base doping concentrations, w_e and w_b are the respective thicknesses, and D_n, D_p are the diffusion constants of electrons in the base, and of holes in the emitter, respectively. The basic idea of the HBT [1], [2] is the introduction of a heterojunction at the emitter/base interface such that the bandgap of the base layer is smaller than that of the emitter. This leads to an enhancement of β by an exponential factor

$$\beta_{HBT} = \beta_{BJT} \cdot \exp[\Delta E_g/kT], \quad (2)$$

which depends only on the effective bandgap difference ΔE_g and thermal energy kT.

The base transit time τ_b of a transistor is a key element for high speed applications. It is directly proportional to the base width w_b, but so is the base sheet conductance, which should be as high as possible for high f_{max} values. Thus, it is necessary to scale up P_b as w_b is reduced, which, however, leads to a reduction of β unless N_e is also increased (eq. 1). This spiral ends as soon as tunneling currents dominate the base emitter diode, which restricts N_e to concentrations $\leq 2 \cdot 10^{18}$ cm^{-3}. In an HBT with its much higher β these overall limitations are much less stringent. For example, at room temperature (kT = 26 meV) and with a typical ΔE_g of 200 meV the exponential factor in eq. 2 will enhance β by a factor of 2200, which can be traded in for an increase of the ratio P_b/N_e by a comparable amount. Hence, while BJTs require N_e to be larger than P_b by typically a factor of the order of 100, the HBT permits base doping concentrations much higher than N_e, and thus provides the low base sheet resistances required for high f_{max} values.

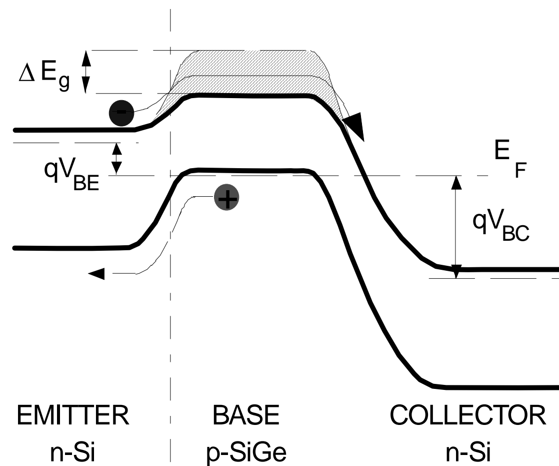

Fig. 1: Comparison of the potential variations across a Si BJT and an HBT with SiGe (narrow-gap) base.

The potential variation throughout a Si/SiGe HBT and a corresponding BJT is schematically depicted in Fig. 1. Since the narrow-gap material SiGe is only used for the base, the Si/SiGe HBT contains actually two heterointerfaces, with the base/collector junction being of limited relevance for device performance, as long as no additional potential barriers occur in the conduction band. It is worth noting that at a given emitter/base voltage the enhanced current gain is due to a reduction in the potential barrier for electrons, whereas the overall barrier for holes remains unaffected.

Rapid progress concerning the high-speed performance of the Si/SiGe HBT has been achieved during recent years. Early concerns about metastable layers, and high-temperature steps during post-epitaxial device processing, led some laboratories to designs with relatively low Ge content (on the order of, or even smaller than 10%) and built-in drift fields induced by a linear increase of x towards the collector layer [3]. Despite the relatively small band offset concomitant with a quite high base sheet resistance of around 17 $k\Omega_{\square}$ outstanding transit frequency of up to $f_T = 75$ GHz were reported by an IBM group in 1990 [4].

A different concept was followed by other labs [5], [6] including our group [7], [8], where a full exploitation of the metastable growth range was attempted in order to gain band offset. Since the demand for short base transit times requires thin base layers, Ge contents of up to 35% could be implemented without formation of misfit dislocations at typical growth temperatures below 600°C. Simultaneously, the base doping level was drastically increased (up to $8 \cdot 10^{20}$ cm^{-3}, typically in the high 10^{19} cm^{-3}), leading to very small base sheet resistances down to 300 $\Omega_{\square}$ (typically around 1 $k\Omega_{\square}$).

Highly doped base layers with Ge contents between 20 and 25% and thicknesses down to 20 nm or even less, the consequent reduction of parasitic effects, and carefully designed transistor layouts, led to Si-based HBTs with f_T [9], [10] values beyond 100 GHz. Recently, with f_{max} at 120 GHz a new record was also achieved for that figure of merit, which is for most applications even more important [11] (Fig. 2). This is a significant improvement as compared to Si BJTs (best f_T values reported at around 60 GHz).

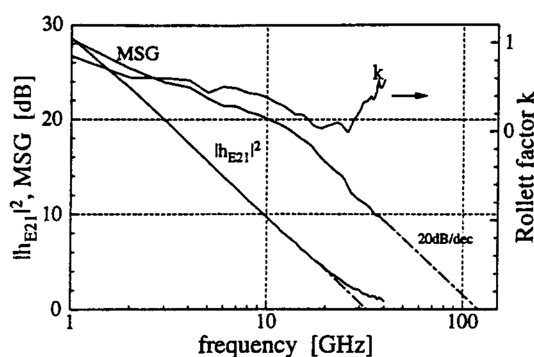

Fig. 2: RF measurements of an HBT in common base configuration at Ic = 40mA and Vcb = 4V (from [11]).

One of the most promising applications for Si/SiGe HBTs will be low-noise amplifiers at GHz frequencies. The high-frequency noise of bipolar transistors is mainly determined by the base resistance R_b, the base transit time τ_b and the emitter/base capacitance C_{eb} [12]. Since HBTs allow a reduction of all three parameters, they are very well

suited for that purpose. Experimental noise measurements are indeed very promising, with excellent noise figures of 0.9 dB at 10 GHz and 0.5 dB at 2 GHz [13].

Fast digital applications are another wide field were Si/SiGe HBTs can excel. For emitter coupled logic (ECL), for example, a low base resistance R_b is crucial, which is one of the strong points of the HBT. Simulations predict outstanding propagation delay times of $\tau_D = 10$ ps [14] for optimized HBTs.

3. Modulation-Doped Field Effect Transistors

The bandgap difference between Si and a pseudomorphic SiGe layer is completely adapted by the offset in the valence band [15], which is advantageous for the HBT, but would otherwise hamper the versatility of the Si/SiGe heterostructure. This restriction no longer applies, if the Si layer is also strained, which leads to a strain-induced splitting of the sixfold degenerate conduction bands in both layers. In 1985 Abstreiter and coworkers could show experimentally that with an in-plane tensile strain in the Si layer the conduction band minimum of the Si layer lies below that of the adjacent SiGe layer, whereas the valence band offset remains always in favor of the SiGe layer [16]. This way, a staggered, or Type-II, band alignment develops, which can be tailored within relatively wide margins by appropriate adjustment of the strain distribution across the heterolayers [3].

With adjustable band offsets in the conduction and valence bands, enhanced electron and hole mobilities can be achieved by spatial separation of the doping atoms and the respective carriers (frequently referred to as modulation doping) [17], [18]. The required strain adjustment for n-type modulation doped structures is achieved by introducing a partly or completely strain-relaxed $Si_{1-x}Ge_x$ interlayer between the mandatory Si substrate and the modulation doping structure [19]. p-type quantum wells (QW) can principally be implemented with pseudomorphic SiGe channels. However, the relatively low experimental hole mobilities in such layers, especially at room temperature [20], suggest the use of strained $Si_{1-x}Ge_x$ channels with x close to 1, which again require a relaxed SiGe buffer layer.

Initially, $Si_{1-x}Ge_x$ buffer layers with constant x were grown to a thickness somewhat above the (growth temperature dependent) critical thickness for strain relaxation by the formation of misfit dislocations. These were sufficient to demonstrate the strain-induced Type-II band ordering and the electron-mobility enhancement by modulation doping in a subsequently deposited Si/SiGe heterostructure with a Si quantum well [18]. Also, the first n-type MODFETs in this material system were based on such a buffer type [21]. Despite gradual improvements [22], however, the low-temperature mobilities remained behind expectations. One of the main reasons was seen in the strain-adjusting SiGe buffer layers then used, which were known to contain a high density ($>10^9$ cm^{-2}) of detrimental threading dislocations that penetrate through all active layers, finally ending at the free surface.

A major breakthrough with threading dislocation densities reduced by several orders of magnitude was achieved by introducing a linearly or step-wise increasing Ge content concomitant with relatively high growth temperatures [23] – [25]. Because of the gradual increase of the lattice mismatch in such a buffer, the misfit dislocation network is distributed over the graded layer rather than being concentrated at the interface to the Si substrate, which would be the case if a constant Ge content is used throughout (Fig. 3).

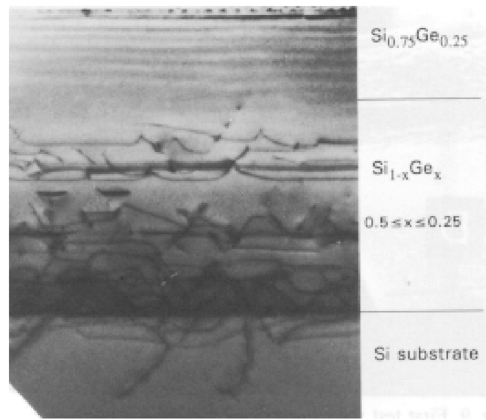

Fig. 3: TEM cross sectional view of a $Si_{1-x}Ge_x$ buffer layer with linear grading of the Ge content from 5% to 30%. Note the distribution of the misfit dislocation network over the thickness of the grading and the virtual dislocation-free upper part of the buffer grown at a constant x.

The greatly improved buffer quality soon led to low-temperature electron-mobilities in excess of 100000 cm^2/Vs [25] – [27] with the best values reaching now 500000 cm^2/Vs [28] in back-gated structures. This is the highest known mobility of a two-dimensional electron gas (2DEG) in Si, which is more than a factor of ten higher than the best values found in Si MOSFETs [29]. Moreover, room temperature Hall-mobilities of about 2500 cm^2/Vs were found in the MODFET samples, which not only exceed the values of commercial MOSFETs by a factor of 2.5, but also are higher than the bulk mobility of intrinsic Si.

The success of n-MODQW structures grown on graded SiGe buffers with an effective composition of up to x=30% suggested an extension to higher Ge contents (up to 100%), to allow p-type QW structures with channels consisting of pure Ge, which has the highest hole mobilities of conventional semiconductors. However, with increasing x_{eff} (and thus lattice mismatch), growth becomes more demanding. It requires a careful selection of growth parameters to maintain a low threading dislocation density without running into a three-dimensional growth mode. Based on this concept, p-MODQW structures with Ge channels grown on Si substrates became available recently. They show promising hole mobilities at room temperature (up to 1300 cm^2/Vs) [30] and 4.2 K (up to 55000 cm^2/Vs) [31], but a premature mobility saturation observed below about 40 K is indicative of relatively high defect or background doping concentrations within the Ge channel. Obviously, further refinements of the growth and doping conditions are required. Nonetheless, the basic superiority of a Ge channel and the compatibility with Si substrates has clearly been demonstrated.

One of the main attractions of the high-mobility Si/SiGe and Si/SiGe/Ge MODQW-structures is their potential in terms of high-speed device applications. Consequently, the availability of such samples almost immediately led to n-type MODFETs with impressive transconductances [32], [33]. The highest values reported so far are g_m=340 and 670 mS/mm at 300 and 77 K, respectively (Fig. 4). Recently, also p-type MODFETs with Ge-channels grown on Si substrates were fabricated successfully [30]. Although their performance has not yet reached the level of their n-type counterparts, transconductances of 125 and 290 mS/mm at 300 K and 77 K, respectively, are very promising for future developments (Fig. 5).

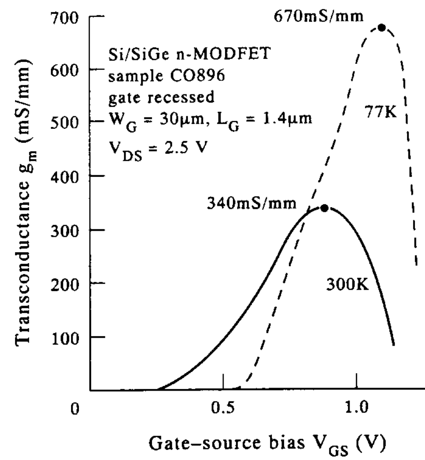

Fig. 4: Extrinsic transconductance g_{me} at room temperature and at 77 K of a gate-recessed n-type (Si channel) MODFET device utilizing a high-mobility Si/SiGe heterostructure grown on Si substrates (from [30]).

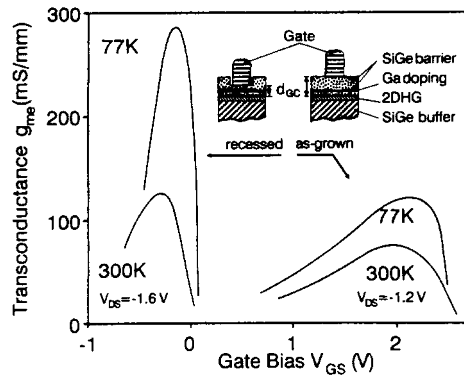

Fig. 5: Extrinsic transconductance g_{me} of Ge-channel (p-type) MODFETs with and without gate recessing at room temperature and at 77 K (from [29])

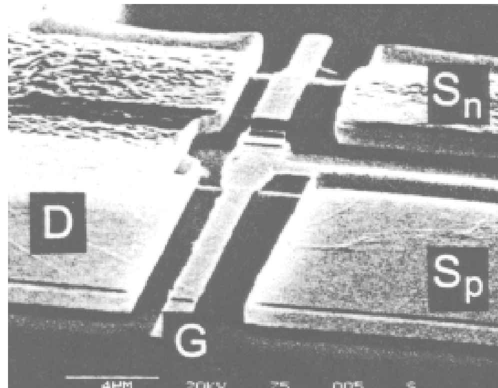

Fig. 6: First test vehicle of a CMODFET with stacked p- and n-FETs. The common Drain metallization is on the left, the separate Source contacts at the right. The common T-shaped gate connects the p-FET in the foreground with the stacked n-FET in the background.

The implementation of superior n- and p-MODFETs is a prerequisite for complementary transistors (CMODFETs) with matched characteristics, which cannot be realized in any of the established material systems because of the far inferior properties of the respective p-type devices. With almost identical mobilities of electrons in Si and holes in Ge, the Si/SiGe/Ge heterosystem could for the first time provide such matched transistor pairs, and moreover, remain widely compatible with Si very large scale integration (VLSI) technologies. Initial steps to implement such CMODFETs are already under way. This is demonstrated in Fig. 6, which shows a simplified double-mesa CMODFET with a layer sequence consisting of an n-MODFET structure grown on top of a p-MODFET without growth interruption. This development, which will certainly require more refined integration concepts and process steps, could once open the field of high-speed applications for complementary logic, which is in its contemporary CMOSFET implementation the most widespread concept in microelectronics.

4. Outlook

Thorough understanding of the basic material aspects and successful development of adequate growth techniques allow us now to exploit the benefits of lattice mismatched heterosystems, and to stay within their limits. Because of its principal compatibility with the highly developed Si technology the Si/SiGe system is of special interest. The recently developed Si/SiGe HBTs and MODFETs demonstrate that, with the aid of this heterojunction, Si-based electronics can significantly extend its high frequency properties well into the 100 GHz range.

Acknowledgments

The contributions and helpful comments of A. Gruhle, A. Schüppen, U. König, H. Kibbel, and H.-J. Herzog are gratefully acknowledged.

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