Lateral Quantum Dot in Si/SiGe Realized by a Schottky Split-Gate Technique

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Introduction

Single electron transistors (SET) in silicon/silicon-germanium heterostructures are of great current interest because of their envisaged use as elements for quantum computation [1]. Recently, several SETs in silicon/silicon-germanium have been reported [2] – [5]. However, none of these were achieved by the classical split-gate technique that is necessary for the coupling of quantum dots and for high integration. Furthermore, it was argued that a SET realized only with Schottky gates is not feasible because of excessive gate leakage currents which were attributed to threading dislocations. We report on the first Coulomb blockade measurements of a SET formed by the split gate technique on a modulation doped SiGe heterostructure.

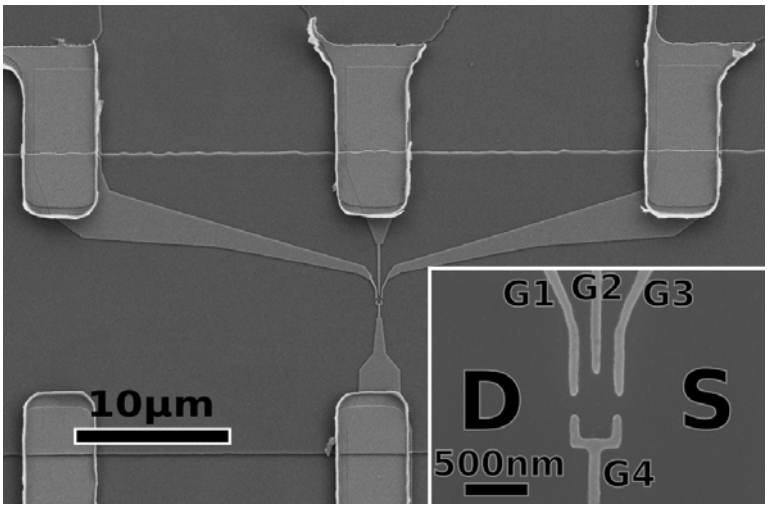

Fig. 1: Scanning electron micrographs of the palladium split gate arrangement on a mesa-etched Hall bar. The main image shows the complete area of the Pd gates including the leads to the bond pads. Insert shows the active SET region defined by the four split gates G1 – G4. The half-pitch of the upper gates is 90 nm.

Sample Preparation

The sample was grown in a Riber SIVA 45 Si molecular beam epitaxy (MBE) apparatus. The 2DEG is formed at the upper interface of a 150 Å thick strained Si channel grown on a 3 µm relaxed step graded buffer ($Si_{0.95}Ge_{0.05}$ to $Si_{0.75}Ge_{0.25}$). A 150 Å thick

$Si_{0.75}Ge_{0.25}$ spacer layer separates the channel from a 150 Å thick antimony doped $Si_{0.75}Ge_{0.25}$ layer. Finally a 450 Å thick layer $Si_{0.75}Ge_{0.25}$ and a 100 Å Si cap were grown. Electrical measurements at 1.5 K showed an electron mobility of 150000 cm^2/Vs at an electron density of 3.2 x 10^{11} cm^{-2}.

Ohmic contacts were formed by deposition of Au/Sb and subsequent annealing at 350 ºC for 60 sec. A Hall bar structure was prepared by reactive ion etching (RIE) with SF_6. Subsequently the split gate structures were written by e-beam lithography with a LEO Supra 35 SEM in PMMA. Finally the split gates were fabricated by using a lift-off technique after depositing a layer of Pd. The final structure is shown in Fig. 1. The pitch between the upper gates is 185 nm.

Experiments

As the feasibility of a Schottky-gate approach for SET applications on Si/SiGe heterostructures was generally questioned [2], [3], [6], we carefully characterized the I-V characteristics of the Schottky gates. For testing the worst-case condition, all four gates were connected in parallel to maximize possible leakage currents. The total gate area for the connected gates was about 150 μm^2. Down to a voltage of about –3 V the total leakage current is below 20 pA (Fig. 2), which is on the lower limit of our experimental setup [7]. Since the measurements we report below are observed at gate voltages between –1.6 V and –1.46 V, we stay safely within the non-conducting part of the diode characteristics.

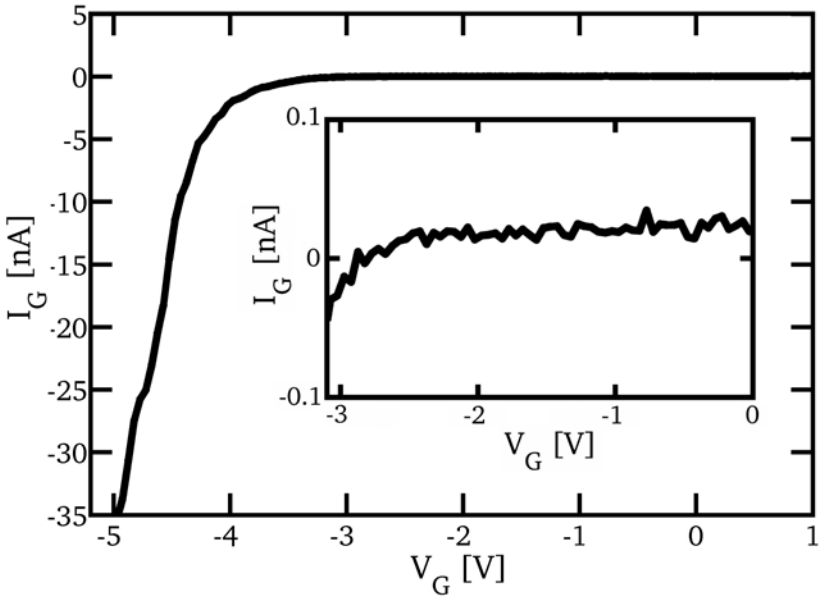

Fig. 2: I-V-characteristics of all gates connected in parallel to maximize possible leakage currents. Down to about –3 V the leaking currents are below the measurement accuracy. The insert shows a zoom-in of the non-conducting range of the diode characteristics.

By applying negative voltages to the gates the underlying 2DEG can be depleted and a quantum dot (QD) is formed. Negative voltages applied to gates G1 and G4, and G3 and G4 define the tunnel barriers, on the drain, and source side, respectively. The QD is controlled by the voltage applied to the plunger gate G2, and the voltage on G4. In the SET operation mode conductance between source and drain is measured as a function of the plunger gate voltage. For this purpose, we utilized a standard low fre-

quency lock-in technique [8]. The experiments were performed in a 3He/4He dilution refrigerator at a temperature of 30 mK. By scanning the voltage V_G, which was here applied to both gates G1 and G2 typical conductance oscillations where recorded (Fig. 3).

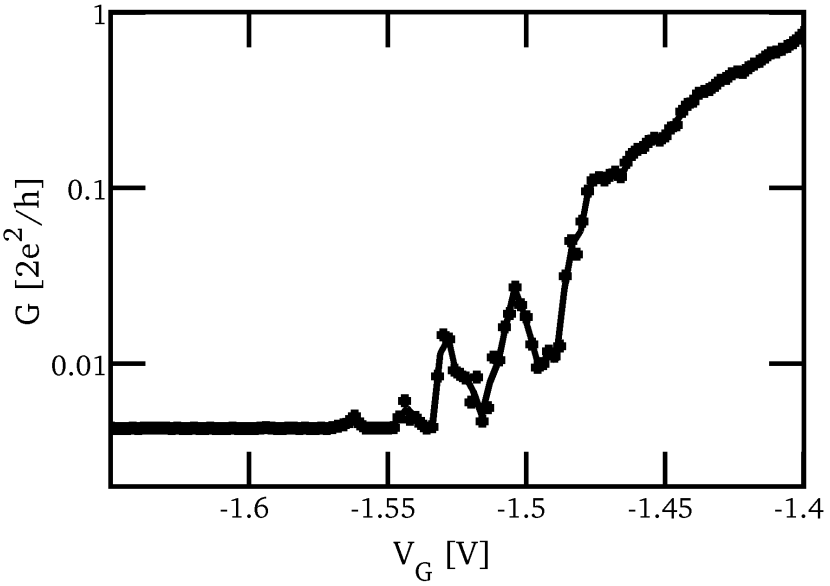

Fig. 3: Conductance oscillations measured at 30 mK by changing the gate voltages of gates G1 and G2 with fixed gate voltage at G3 and G4. One can distinguish different conductance peaks separated by vanishing conductance in the Coulomb-blockade regions. Lines are guides to the eye.

By measuring the conductance as a function of the plunger gate voltage and an additional DC voltage VDS applied between source and drain contacts, one can obtain the quantum dot spectrum, resulting in Coulomb blockade ''diamonds''. Figure 4 shows well resolved Coulomb blockade diamonds. Such experiments reveal the stability of the SET with regard to the number of electrons on the dot [8]. During the measurement time of about 70 h no indication for any transient in the number of electrons was found. Well-behaved Coulomb blockade diamonds were measured up to a temperature of 1.5 K, which was the maximum reachable temperature in the measurement apparatus.

By analyzing the distance between neighboring Coulomb diamonds and their confining slopes we estimated the gate and drain capacity to be C_G = 6.5 aF and C_D = 18 aF, respectively, and the total dot capacity to be C = 40 aF which results in a Coulomb charging energy of about 4 meV. Assuming the dot to be a metallic disc with radius R we estimated the dot radius to be about 50 nm, which corresponds to a maximum number of about 25 electrons on the dot and an estimated single particle energy spacing of 0.16 meV.

Conclusion

Our experiments demonstrate that Schottky-barrier reducing mechanisms can be overcome by adequately designed Si/SiGe heterostructures and that SET functionality can be achieved in modulation-doped Si/SiGe heterostructures with a standard split-gate approach that can easily be integrated into an array of coupled SETs as suggested in Ref. 1.

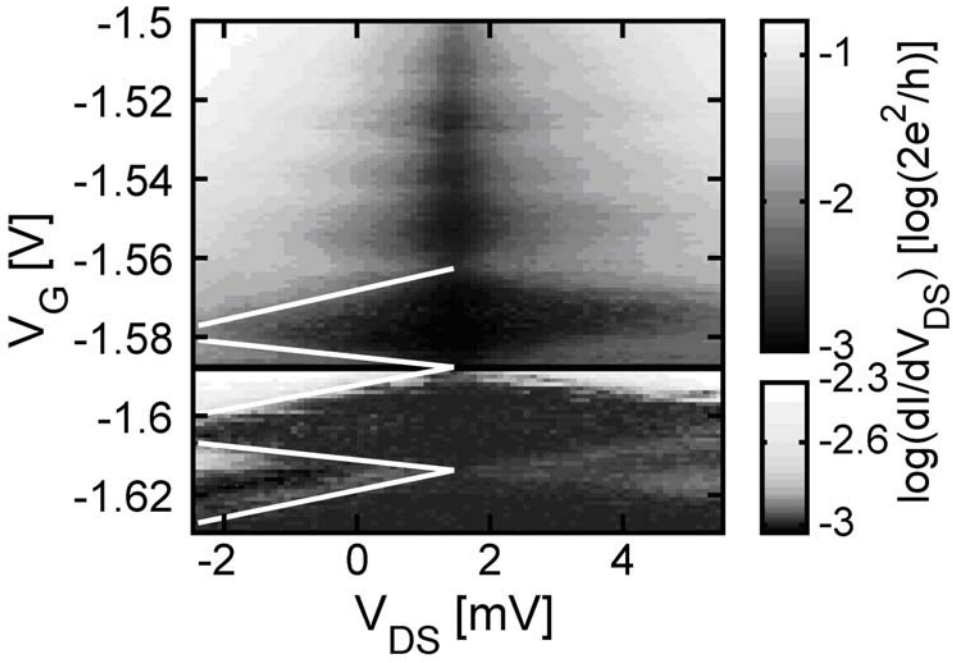

Fig. 4: Stability plot at 30 mK of the differential conductance through the dot as a function of the dc voltage V_{DS} between drain and source, and the gate voltage V_G applied to gates G1 and G2. Seven stability diamonds are clear visible.

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