

Fabrication of Silicon Vertical Taper Structures for Fiber to Chip Coupler by KOH Anisotropic Etching

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In order to exploit the full potential of silicon photonic devices we require an efficient way of coupling light from fibers to integrated photonic circuits. One of the most common solutions to this problem is the use of tapered silicon waveguides. We present a method of vertical silicon taper fabrication using KOH anisotropic etching. The main advantage of this method is the low roughness of the tilted surface, which should lead to a good optical transmission of the tapered waveguide. We successfully created vertical silicon tapers with heights more than sufficient for the use in fiber to chip light couplers.

Introduction

The use of high index contrast waveguides and devices is the key to successful development and fabrication of photonic integrated circuits. Considering the widespread use of silicon technologies and the suitable optical properties of silicon in the infrared range, this material is one of the best candidates for such devices [1]. In order to exploit the full potential of silicon photonic devices we require an efficient way of coupling light from fibers to integrated photonic circuits. One of the most common solutions to this problem is the use of tapered silicon waveguides [2]. However this approach is connected with the problem of creating a vertical taper. The efforts to fabricate such a taper are currently concentrated mainly on various lithography techniques used to create a taper shaped structure in photoresist. The pattern is then transferred to silicon by reactive ion etching. Although silicon taper structures have been already successfully fabricated using grayscale lithography methods [3], this approach introduces an additional non-standard lithography step and may also lead to the increase of the surface roughness, which is critical for the proper function of photonic devices [2].

One of the possibilities to fabricate a vertical taper structure is the use of a silicon substrate with a tilted $\langle 111 \rangle$ crystallographic orientation. Such wafers are produced by changing the cutting angle in the silicon wafer production process. In order to fabricate the desired vertical taper structure a very small angle (2 – 5 degrees) between the $\langle 111 \rangle$ orientation and the wafer surface is needed.

These substrates can then be used for the creation of a taper by means of anisotropic etching (i.e. etching along preferred crystallographic direction). One of the most suitable chemicals for anisotropic etching of silicon is potassium hydroxide (KOH) water solution. Under suitable process conditions (temperature, KOH concentration) we can achieve a big etching speed difference resulting in the uncovering of $\langle 111 \rangle$ planes.

Therefore using a substrate with tilted $\langle 111 \rangle$ plane should lead to the formation of vertically tilted surfaces which could be used for the fabrication of vertical taper structures.

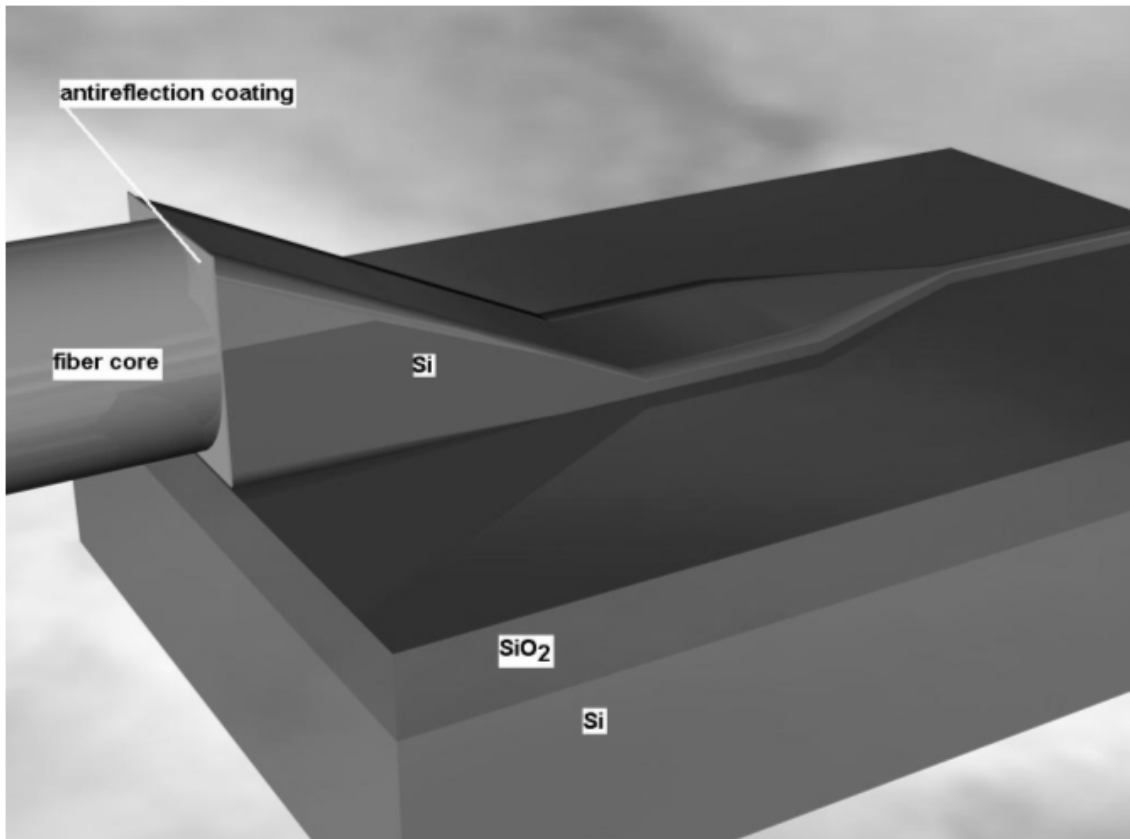


Fig. 1: Fiber to chip interface consisting of two silicon structures - one with vertical and one with horizontal tapering. The optical signal from a fiber core is led to the first taper via an antireflection coating to compensate the refractive index difference. The light propagates through both tapers and finally ends in a single mode silicon waveguide. Dimensions – Start: fiber core 6 μm in diameter; End: Si waveguide 300 x 300 nm; Length = 200 – 400 μm .

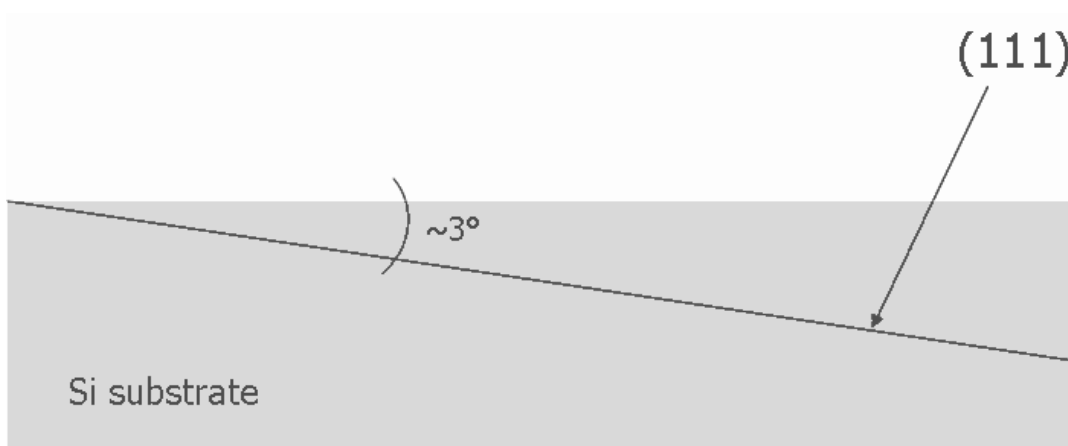


Fig. 2: Silicon substrate with tilted $\langle 111 \rangle$ plane.

The main advantages of this process are:

1. Simplicity (KOH wet chemical etching is well known and often used process)
2. Set tilt angle and shape (the angle only depends on the substrate and is not influenced by the process parameters and the shape is always linear)
3. Low roughness of the tilted surface

Experimental

The process of anisotropic silicon etching is influenced by several parameters. Besides etching solution parameters (KOH concentration, temperature), the etching process also depends on the roughness of the silicon substrate. This influence is becoming stronger with the decreasing angle between the $\langle 111 \rangle$ orientation and the wafer surface. The main reason for this behavior is the low etching speed of such substrate surfaces caused by the very small tilt angle – the surface plane orientation is very close to $\langle 111 \rangle$. The presence of the surface roughness increases the etching speed, because it offers a possibility of directly etching the silicon in directions much different from the $\langle 111 \rangle$ plane. However this process continues only until the $\langle 111 \rangle$ planes are revealed and the surface consists of triangle shapes of random sizes. The average size of these triangles is determined by the initial surface roughness of the silicon substrate. Further etching results only in low etching speeds because the surface consists of $\langle 111 \rangle$ planes. Because of these obstacles, the fabrication of larger taper structures by simple etching of an unstructured silicon substrate is very difficult.

In order to obtain a larger structure, we can no longer depend on the surface roughness influence or the low etching speed in the vertical direction. Instead of this, we have to take advantage of much faster etching in the direction parallel to the substrate. This can be achieved by structuring the surface before the actual anisotropic etching takes place. One of the possibilities how to do this is to etch trenches or steps to the substrate and thus reveal planes perpendicular to the surface – Fig. 3.

With the structured substrate, we are able to achieve high etching speeds and reveal the $\langle 111 \rangle$ planes much faster than in the case of unstructured substrate. The size of the tilted surface obtained from the structured surface is dependent on the structuring depth – the depth of the etched steps / trenches.

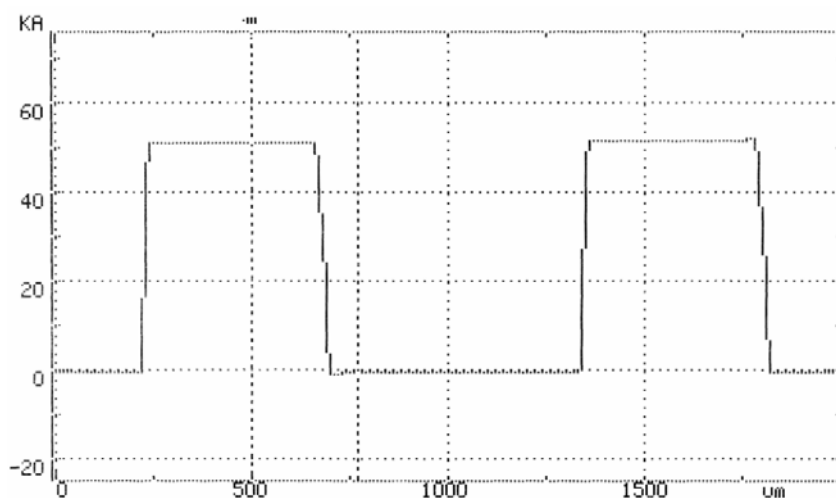


Fig. 3: Structured silicon profile – 5 μm deep trenches etched in silicon by reactive ion etching process.

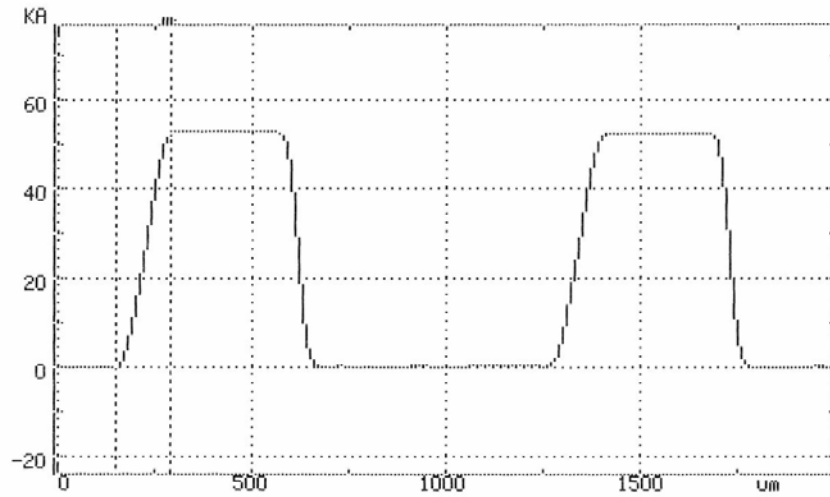


Fig. 4: The profile of the structured silicon after 30 min KOH etching, 47% KOH solution, 80°C.

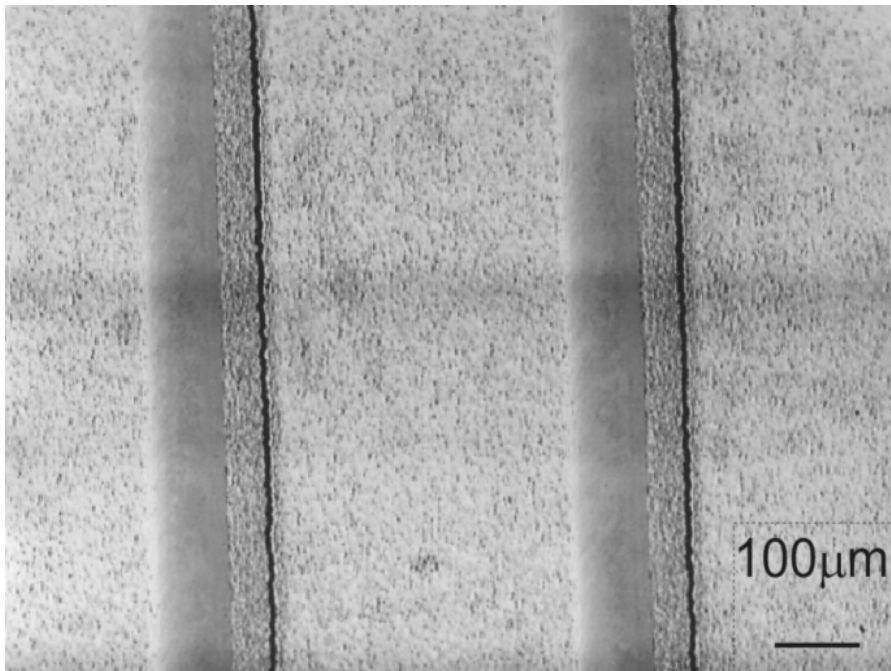


Fig. 5: Structured silicon surface after 30 min KOH etching, 47% KOH solution, 80°C.

The KOH etching of the Si trenches can be described by two processes:

1. Etching in the direction parallel to the surface. Taper structures are formed mainly by fast etching parallel to the surface ($\sim 100 \mu\text{m}/\text{hour}$). Taper height depends on the initial trench/edge depth or roughness – in the case of unstructured substrate. This process continues only until the $\langle 111 \rangle$ planes are revealed.
2. Etching in the direction perpendicular to the surface. This process is slow, results in further increase of the taper height but also increases the surface roughness.

In order to create a vertical taper structure with small surface roughness we need therefore to keep the KOH etching time as short as possible (the etching perpendicular to the surface will be in this case negligible).

Conclusions

Using the anisotropic etching of silicon with tilted $\langle 111 \rangle$ plane, we successfully created vertical silicon tapers with heights up to 35 μm and lengths up to 500 μm , which is more than sufficient for them to be used for fiber to chip light coupling.

We furthermore investigated the etching process of structured as well as unstructured silicon substrates and found out, that only the use of reactive ion etching prior to the KOH etching can ensure a well defined shape of the silicon vertical taper. Our experiments indicate a significant time dependence of the etched taper profile. In order to create a structure for the purpose of optical fiber to chip coupling, we need to keep the surface roughness minimal and therefore we have to reduce the time of the anisotropic etching to a minimum.

Basing on our experimental results, we are now able to design a fiber to chip optical interface with low scattering losses and high transmission.

References

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